

54LS/74LS374

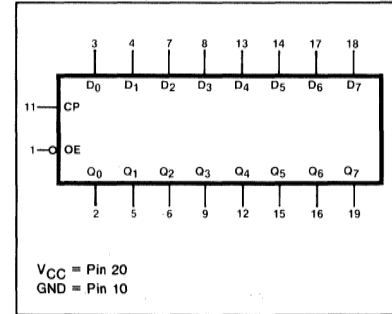
DESCRIPTION

The "374" is an Octal D Flip-Flop with 3-State buffered outputs. The device is used primarily as an 8-bit positive edge triggered storage register for interfacing with a 3-State bus. Data on the D inputs is transferred to storage during the LOW-to-HIGH transition of the Clock (CP) input. The 3-State output buffers are controlled by an active LOW Output Enable ( $\overline{OE}$ ) input. A HIGH on the  $\overline{OE}$  input forces the eight outputs to the high impedance "off" state. When  $\overline{OE}$  is LOW, the data in the register appears at the outputs.

FEATURES

- 8-Bit positive edge triggered register
- 3-State output buffers
- Common Clock input with hysteresis
- Common 3-State Output Enable control
- Independent register and 3-State buffer operation
- See "364" for MOS compatible output version

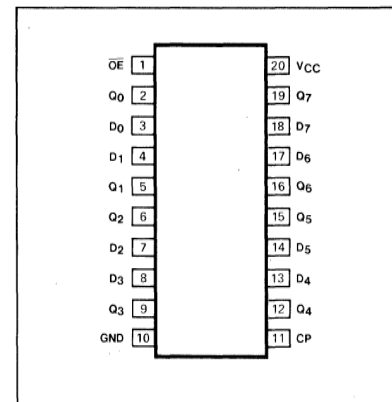
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$ ; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$ ; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS374N	
Ceramic DIP	N74LS374F	S54LS374F
Flatpak		

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	$I_{IH}$ ( $\mu A$ ) $I_{IL}$ (mA)			20 -0.4
D <sub>0</sub> -D <sub>7</sub>	Parallel Data inputs	$I_{IH}$ ( $\mu A$ ) $I_{IL}$ (mA)			20 -0.4
$\overline{OE}$	Output Enable (active LOW) input	$I_{IH}$ ( $\mu A$ ) $I_{IL}$ (mA)			20 -0.4
Q <sub>0</sub> -Q <sub>7</sub>	3-State outputs	$I_{OH}$ (mA) $I_{OL}$ (mA)			-1/-2.6(a) 12/24(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

**FUNCTIONAL DESCRIPTION**

The "374" is an 8-bit edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ( $\overline{OE}$ ) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

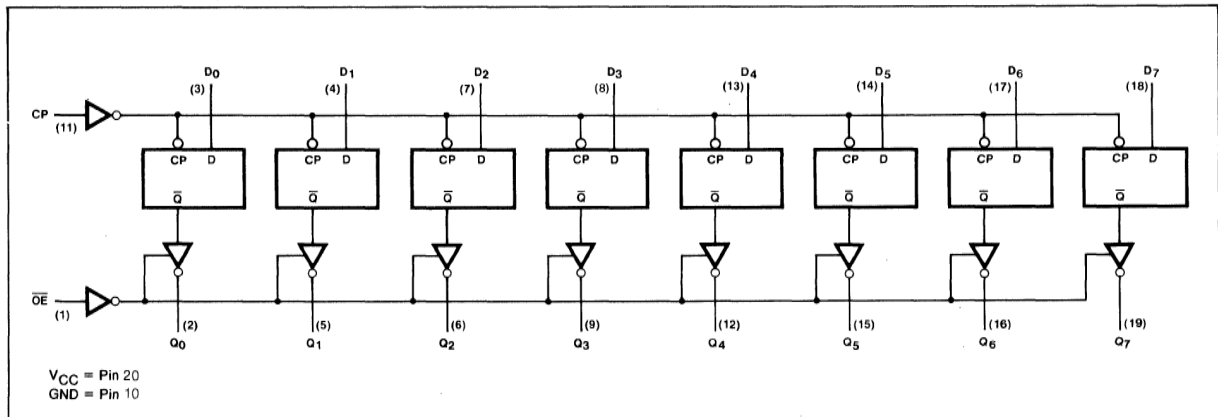
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ( $\overline{OE}$ ) controls all eight 3-State buffers independent of the register operation. When  $\overline{OE}$  is LOW, the data in the register appears at the outputs. When  $\overline{OE}$  is HIGH, the outputs are in the high impedance "off" state, which means they will neither drive nor load the bus.

**MODE SELECT—FUNCTION TABLE**

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS Q <sub>0</sub> -Q <sub>7</sub>
	$\overline{OE}$	CP	D <sub>n</sub>		
Load & read register	L	↑	l	L	L
	L	↑	h	H	H
Load register & disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = HIGH voltage level  
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition  
 L = LOW voltage level  
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition  
 (Z) = HIGH impedance "off" state  
 ↑ = LOW-to-HIGH clock transition

**LOGIC DIAGRAM**



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE<sup>(b)</sup>**

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V <sub>OL</sub> Output LOW voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 12mA						0.4	V
	V <sub>OE</sub> = V <sub>IL</sub> , I <sub>OL</sub> = 24mA						0.5 <sup>(c)</sup>	V
V <sub>OH</sub> Output HIGH voltage	V <sub>CC</sub> = Min, V <sub>OE</sub> = V <sub>IL</sub> I <sub>OH</sub> = See Fan Out Table					2.4		V
I <sub>OS</sub> Output short circuit current	V <sub>CC</sub> = Max, V <sub>OUT</sub> = 0V					-30	-100	mA
I <sub>CC</sub> Supply current	V <sub>CC</sub> = Max	Mil					49	mA
		Com					45	mA

**AC CHARACTERISTICS: T<sub>A</sub> = 25°C (See Section 4 for Test Circuits and Conditions)**

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
f <sub>MAX</sub> Maximum clock frequency	Figure 1					35		MHz
t <sub>PLH</sub> Propagation delay	Figure 1					28		ns
t <sub>PHL</sub> Clock to output						38		ns
t <sub>PZH</sub> Enable time to HIGH level	Figure 2					20		ns
t <sub>PZL</sub> Enable time to LOW level	Figure 3					28		ns
t <sub>PHZ</sub> Disable time from HIGH level	Figure 2					45		ns
	Figure 2, C <sub>L</sub> = 5pF <sup>(d)</sup>					22		ns
t <sub>PLZ</sub> Disable time from LOW level	Figure 3					24		ns
	Figure 3, C <sub>L</sub> = 5pF <sup>(d)</sup>					22		ns

**AC SETUP REQUIREMENTS: T<sub>A</sub> = 25°C (See Section 4 for Test Circuits and Conditions)**

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t <sub>W</sub> Clock pulse width	Figure 1					15		ns
t <sub>s</sub> Setup time Data to Clock	Figure 4					10		ns
t <sub>h</sub> Hold time Data to Clock	Figure 4					3.0		ns

**NOTES**

- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.
- c. This parameter for Commercial Range only.
- d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

AC WAVEFORMS

