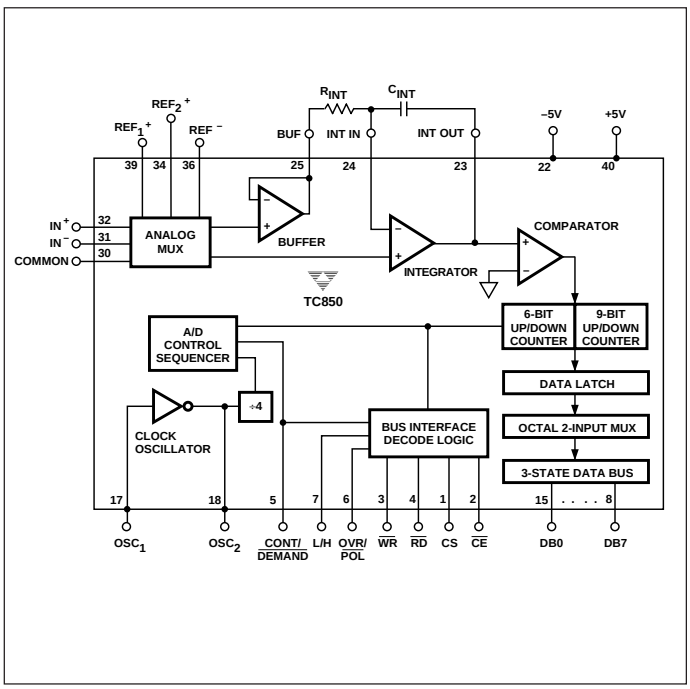
15-BIT, FAST-INTEGRATING CMOS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **15-bit Resolution Plus Sign Bit**
- **Up to 40 Conversions per Second**
- **12 Conversions per Second Guaranteed**
- **Integrating ADC Technique**
  - **— Monotonic**
  - **— High Noise Immunity**
  - **— Auto-Zeroed Amplifiers Eliminate Offset Trimming**
- **Wide Dynamic Range 96dB**
- **Low Input Bias Current 30pA**
- **Low Input Noise ..... 30μV_{P-P}**
- **Sensitivity 100μV**
- **Flexible Operational Control**
  - **— Continuous or On-Demand Conversions**
  - **— Data Valid Output**
- **Bus Compatible, 3-State Data Outputs**
  - **— 8-Bit Data Bus**
  - **— Simple μP Interface**
  - **— Two Chip Enables**
  - **— Read ADC Result Like Memory**
- **$\pm$5V Power Supply Operation 20mW**
- **40-Pin Dual-in-Line or 44-Pin PLCC Packages**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The TC850 is a monolithic CMOS analog-to-digital converter (ADC) with resolution of 15-bits plus sign. It combines a chopper-stabilized buffer and integrator with a unique multiple-slope integration technique that increases conversion speed. The result is 16 times improvement in speed over previous 15-bit, monolithic integrating ADCs (from 2.5 conversions per sec up to 40 per sec). Faster conversion speed is especially welcome in systems with human interface, such as digital scales.

The TC850 incorporates an ADC and a μP-compatible digital interface. Only a voltage reference and a few noncritical passive components are required to form a complete 15-bit plus sign ADC.

CMOS processing provides the TC850 with high-impedance differential inputs. Input bias current is typically only 30pA, permitting direct interface to sensors. Input sensitivity of 100μV per least significant bit (LSB) eliminates the need for precision external amplifiers. The internal amplifiers are auto-zeroed, guaranteeing a zero digital output with 0V analog input. Zero adjustment potentiometers or calibrations are not required.

The TC850 outputs data on an 8-bit, 3-state bus. Digital inputs are CMOS compatible; outputs are TTL/CMOS compatible. Chip-enable and byte-select inputs combined with an end-of-conversion output ensures easy interfacing to a wide variety of microprocessors. Conversions can be performed continuously or on command. In continuous mode, data is read as three consecutive bytes and manipulation of address lines is not required.

Operating from $\pm$5V supplies, the TC850 dissipates only 20mW. It is packaged in 40-pin plastic or ceramic dual-in-line packages (DIPs) and in a 44-pin plastic leaded chip carrier (PLCC), surface-mount package.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC850CLW	44-Pin PLCC	0°C to +70°C
TC850CPL	40-Pin Plastic DIP	0°C to +70°C
TC850IJL	40-Pin CerDIP	– 25°C to +85°C
TC850ILW	44-Pin PLCC	– 25°C to +85°C

TC850

ABSOLUTE MAXIMUM RATINGS*

Positive Supply Voltage (V_{DD} to GND) ..... +6V
Negative Supply Voltage (V_{SS} to GND) ..... – 9V
Analog Input voltage (IN^+ or IN^-) ..... V_{DD} to V_{SS}
Voltage Reference Input
(REF_1^+, REF_1^-, REF_2^+) ..... V_{DD} to V_{SS}
Logic Input Voltage ..... V_{DD} + 0.3V to GND – 0.3V
Current Into Any Pin 10mA
While Operating 100µA
Ambient Operating Temperature Range
C Device ..... 0°C to +70°C
I Device ..... – 25°C to +85°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ($T_A \le 70°C$)
CerDIP 2.29W
Plastic DIP 1.23W
Plastic PLCC 1.23W

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

$V_S = \pm5V$, f_{CLK} = 61.44 kHz, V_{FS} = 3.2768V, T_A = 25°C, Fig. 1 Test Circuit, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Zero-Scale Error	V_{IN} = 0V		±0.25	±0.5	LSB
	End Point Linearity Error	$-V_{FS} \le V_{IN} \le +V_{FS}$	—	±1	±2	LSB
	Differential Nonlinearity		—	±0.1	±0.5	LSB
I_{IN}	Input Leakage Current	V_{IN} = 0V, T_A = 25°C $0°C \le T_A \le +70°C$ $-25° \le T_A \le +85°C$	— — —	30 — 1.1	75 — 3	pA nA
V_{CMR}	Common-Mode Voltage Range	Over Operating Temperature Range	V_{SS} + 1.5	—	V_{DD} – 1.5	V
CMRR	Common-Mode Rejection Ratio	V_{IN} = 0V, $V_{CM} = \pm1V$	—	80	—	dB
	Full-Scale Gain Temperature Coefficient	External Ref Temperature Coefficient = 0 ppm/°C $0°C \le T_A \le +70°C$	—	2	5	ppm/°C
	Zero-Scale Error Temperature Coefficient	V_{IN} = 0V $0°C \le T_A \le +70°C$	—	0.3	2	µV/°C
	Full-Scale Magnitude Symmetry Error	$V_{IN} = \pm3.275V$	—	0.5	2	LSB
e_N	Input Noise	Not Exceeded 95% of Time	—	30	—	μV_{P-P}
I_S^+	Positive Supply Current		—	2	3.5	mA
I_S^-	Negative Supply Current		—	2	3.5	mA
V_{OH}	Output High Voltage	I_O = 500 µA	3.5	4.9	—	V
V_{OL}	Output Low Voltage	I_O = 1.6 mA	—	0.15	0.4	V
I_{OP}	Output Leakage Current	Pins 8 – 15, High-Impedance State	—	0.1	1	µA
V_{IH}	Input High Voltage	Note 3	3.5	2.3	—	V
IL	Input Low Voltage	Note 3	—	2.1	1	V
I_{PU}	Input Pull-Up Current	Pins 2, 3, 4, 6, 7; V_{IN} = 0V	—	4	—	µA
I_{PD}	Input Pull-Down Current	Pins 1, 5; V_{IN} = 5V	—	14	—	µA
I_{OSC}	Oscillator Output Current	Pin 18, V_{OUT} = 2.5V	—	140	—	µA
C_{IN}	Input Capacitance	Pins 1 – 7, 17	—	1	—	pF
C_{OUT}	Output Capacitance	Pins 8 – 15, High-Impedance State	—	15	—	pF
t_{CE}	Chip-Enable Access Time	CS or $\overline{CE}$, $\overline{RD}$ = LOW (Note 1)	—	230	450	nsec
t_{RE}	Read-Enable Access Time	CS = HIGH, $\overline{CE}$ = LOW (Note 1)	—	190	450	nsec
t_{DHC}	Data Hold From CS or $\overline{CE}$	$\overline{RD}$ = LOW (Note 1)	—	250	450	nsec
t_{DHR}	Data Hold From $\overline{RD}$	CS = HIGH, $\overline{CE}$ = LOW (Note 1)	—	210	450	nsec
t_{OP}	OVR/$\overline{POL}$ Data Access Time	CS = HIGH, $\overline{CE}$ = LOW, $\overline{RD}$ = LOW (Note 1)	—	140	300	nsec

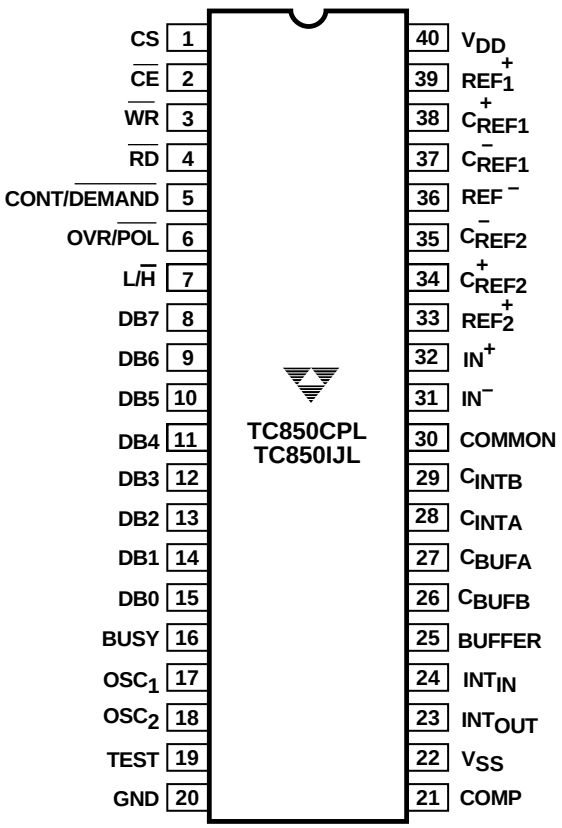
ELECTRICAL CHARACTERISTICS (Cont.)

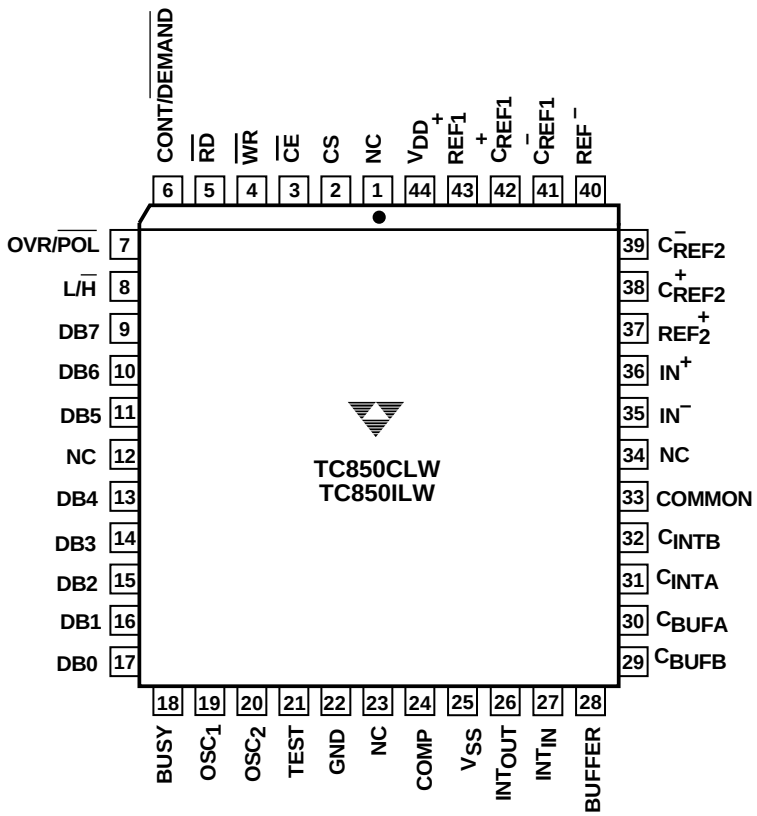
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{LH}	Low/High Byte Access Time	CS = HIGH, $\overline{CE}$ = LOW, $\overline{RD}$ = LOW (Note 1)	—	140	300	nsec
	Clock Setup Time	Positive or Negative Pulse Width	100	—	—	nsec
t_{WRE}	$\overline{RD}$ Minimum Pulse Width	CS = HIGH, $\overline{CE}$ = LOW (Note 2)	450	230	—	nsec
t_{WRD}	$\overline{RD}$ Minimum Delay Time	CS = HIGH, $\overline{CE}$ = LOW (Note 2)	150	50	—	nsec
t_{WWR}	$\overline{WR}$ Minimum Pulse Width	CS = HIGH, $\overline{CE}$ = LOW, Demand Mode	75	25	—	nsec
	Clock Setup Time	Positive or Negative Pulse Width	100	—	—	nsec

NOTES: 1. Demand mode, CONT/$\overline{DEMAND}$ = LOW. Figure 10 timing diagram. C_L = 100pF.
2. Continuous mode, CONT/$\overline{DEMAND}$ = HIGH. Figure 12 timing diagram.
3. Digital inputs have CMOS logic levels and internal pull-up/pull-down resistors. For TTL compatibility, external pull-up resistors to V_{CC} are recommended.

3

PIN CONFIGURATIONS





NC = NO INTERNAL CONNECTION

TC850

PIN DESCRIPTIONS

40-Pin DIP Pin No.	Symbol	Description
1	CS	Chip select, active HIGH. Logically ANDed with $\overline{CE}$ to enable read and write inputs. (See note 4.)
2	$\overline{CE}$	Chip enable, active LOW. (See note 5.)
3	$\overline{WR}$	Write input, active LOW. When chip is selected (CS = HIGH and CE = LOW) and in demand mode (CONT/$\overline{DEMAND}$ = LOW), a logic LOW on $\overline{WR}$ starts a conversion. (See note 4.)
4	$\overline{RD}$	Read input, active LOW. When CS = HIGH and $\overline{CE}$ = LOW, a logic LOW on $\overline{RD}$ enables the 3-state data outputs. (See note 5.)
5	CONT/$\overline{DEMAND}$	Conversion control input. When CONT/$\overline{DEMAND}$ = LOW, conversions are initiated by the $\overline{WR}$ input. When CONT/$\overline{DEMAND}$ = HIGH, conversions are performed continuously. (See note 4.)
6	OVR/$\overline{POL}$	Overrange/polarity data-select input. When making conversions in the demand mode (CONT/$\overline{DEMAND}$ = LOW), OVR/$\overline{POL}$ controls the data output on DB7 when the high-order byte is active. (See note 5.)
7	L/$\overline{H}$	Low/high byte-select input. When CONT/$\overline{DEMAND}$ = LOW, this input controls whether low-byte or high-byte data is enabled on DB0 through DB7. (See note 5.)
8	DB7	Most significant data bit output. When reading the A/D conversion result, the polarity, overrange, and DB7 data are output on this pin. (See text.)
9 – 15	DB6–DB0	Data outputs DB6–DB0. 3-state, bus compatible.
16	BUSY	A/D conversion status output. BUSY goes to a logic HIGH at the beginning of the deintegrate phase and goes LOW when conversion is complete. The falling edge of BUSY can be used to generate a µP interrupt.
17	OSC_1	Crystal oscillator connection or external oscillator input.
18	OSC_2	Crystal oscillator connection.
19	TEST	For factory testing purposes only. Do not make external connection to this pin.
20	DGND	Digital ground connection.
21	COMP	Connection for comparator auto-zero capacitor. Bypass to V_{SS} with 0.1 µF.
22	V_{SS}	Negative power supply connection, typically – 5V.
23	INT_{OUT}	Output of the integrator amplifier. Connect to C_{INT}.
24	INT_{IN}	Input to the integrator amplifier. Connect to summing node of R_{INT} and C_{INT}.
25	BUFFER	Output of the input buffer. Connect to R_{INT}.
26	C_{BUFB}	Connection for buffer auto-zero capacitor. Bypass to V_{SS} with 0.1 µF.
27	C_{BUFA}	Connection to buffer auto-zero capacitor. Bypass to V_{SS} with 0.1 µF.
28	C_{INTA}	Connection for integrator auto-zero capacitor. Bypass to V_{SS} with 0.1 µF.
29	C_{INTB}	Connection for integrator auto-zero capacitor. Bypass to V_{SS} with 0.1 µF.
30	COMMON	Analog common.
31	IN^-	Negative differential analog input.
30	COMMON	Analog common.
33	REF_2^+	Positive input for reference voltage V_{REF2}. ($V_{REF2} = V_{REF1}/64$)
34	C_{REF2}^+	Positive connection for V_{REF2} reference capacitor.
35	C_{REF2}^-	Negative connection for V_{REF2} reference capacitor.
36	REF^-	Negative input for reference voltages.
37	C_{REF1}^-	Negative connection for V_{REF1} reference capacitor.
38	C_{REF1}^+	Positive connection for V_{REF1} reference capacitor.
39	REF_1^+	Positive input for V_{REF1}.
40	V_{DD}	Positive power supply connection, typically +5V.

NOTES: 4. This pin incorporates a pull-down resistor to DGND.
5. This pin incorporates a pull-up resistor to V_{DD}.

THEORY OF OPERATION

The TC850 is a multiple-slope, integrating analog-to-digital converter (ADC). The multiple-slope conversion process, combined with chopper-stabilized amplifiers, results in a significant increase in ADC speed, while maintaining very high resolution and accuracy.

Dual-Slope Conversion Principles

The conventional dual-slope converter measurement cycle (shown in Figure 2A) has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period, measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual-slope converter, complete conversion requires the integrator output to "ramp-up" and "ramp-down." Most dual-slope converters add a third phase, auto-zero. During auto-zero, offset voltages of the input buffer, integrator, and comparator are nulled, thereby eliminating the need for zero-offset adjustments.

Dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. By converting the unknown analog input voltage into an easily-measured function of time, the dual-slope converter reduces the need for expensive, precision passive components.

Noise immunity is an inherent benefit of the integrating conversion method. Noise spikes are integrated, or averaged, to zero during the integration period. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments.

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\, t_{RI}}{RC},$$

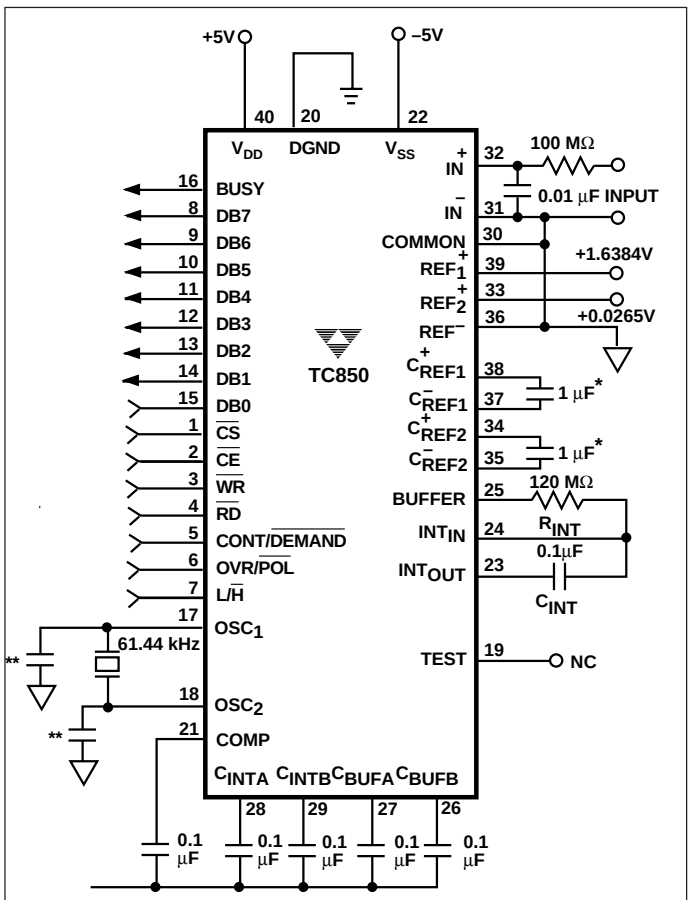
where: V_R = Reference voltage
t_{SI} = Signal integration time (fixed)
t_{RI} = Reference voltage integration time (variable).

Multiple-Slope Conversion Principles

One limitation of the dual-slope measurement technique is conversion speed. In a typical dual-slope method, the auto-zero and integrate times are each one-half of the deintegrate time. For a 15-bit conversion, $2^{14} + 2^{14} + 2^{15}$ (65,536) clock pulses are required for auto-zero, integrate, and deintegrate phases, respectively. The large number of clock cycles effectively limits the conversion rate to about 2.5 conversions per second, when a typical analog CMOS fabrication process is used.

The TC850 uses a multiple-slope conversion technique to increase conversion speed (Figure 2B). This technique makes use of a two-slope deintegration phase and permits 15-bit resolution up to 40 conversions per second.

During the TC850's deintegration phase, the integration capacitor is rapidly discharged to yield a resolution of 9 bits. At this point, some charge will remain on the capacitor. This remaining charge is then slowly deintegrated, producing an



NOTES: Unless otherwise specified, all 0.1µF capacitors are film dielectric.
Ceramic capacitors are not recommended.
NC = No internal capacitors
*Polypropylene capacitors.
** 100pF Mica capacitors.

Figure 1. Standard Circuit Configuration

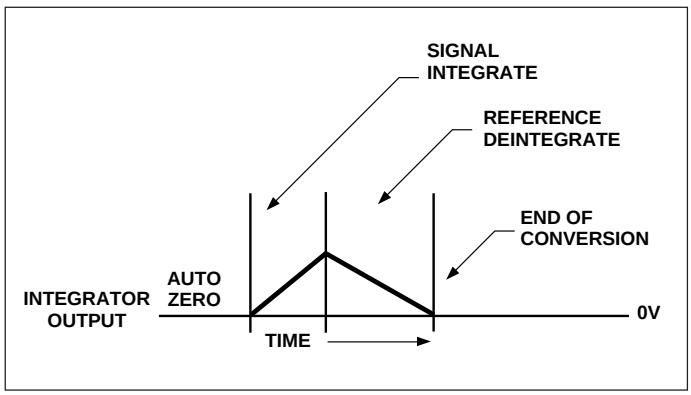


Figure 2A. Dual-Slope ADC Cycle

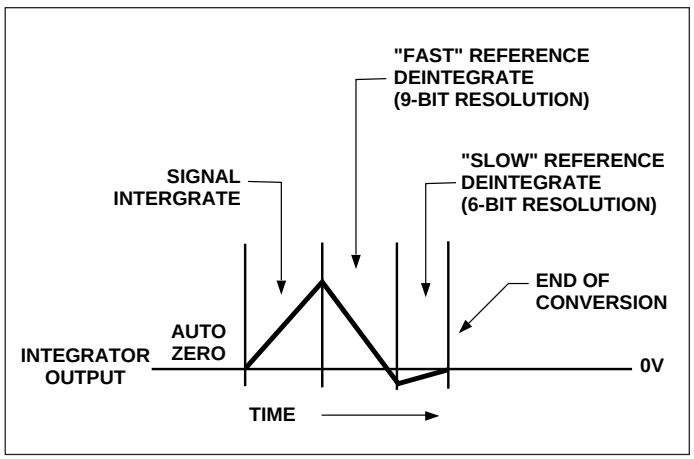


Figure 2B. "Fast-Slow" Reference Deintegrate Cycle

additional 6 bits of resolution. The result is 15 bits of resolution achieved with only $2^9 + 2^6$ (512 + 64, or 576) clock pulses for deintegration. A complete conversion cycle occupies only 1280 clock pulses.

In order to generate "fast-slow" integration phases, two voltage references are required. The primary reference (V_{REF1}) is set to one-half of the full-scale voltage (typically V_{REF1} = 1.6384V, and V_{FS} = 3.2768V). The secondary voltage reference (V_{REF2}) is set to $V_{REF1}/64$ (typically 25.6 mV). To maintain 15-bit linearity, a tolerance of 0.5% for V_{REF2} is recommended.

ANALOG SECTION DESCRIPTION

The TC850 analog section consists of an input buffer amplifier, integrator amplifier, comparator, and analog switches. A simplified block diagram is shown in Figure 3.

Conversion Timing

Each conversion consists of three phases: (1) Zero Integrator, (2) Signal Integrate, and (3) Reference Integrate (or Deintegrate). Each conversion cycle requires 1280 internal clock cycles (Figure 4).

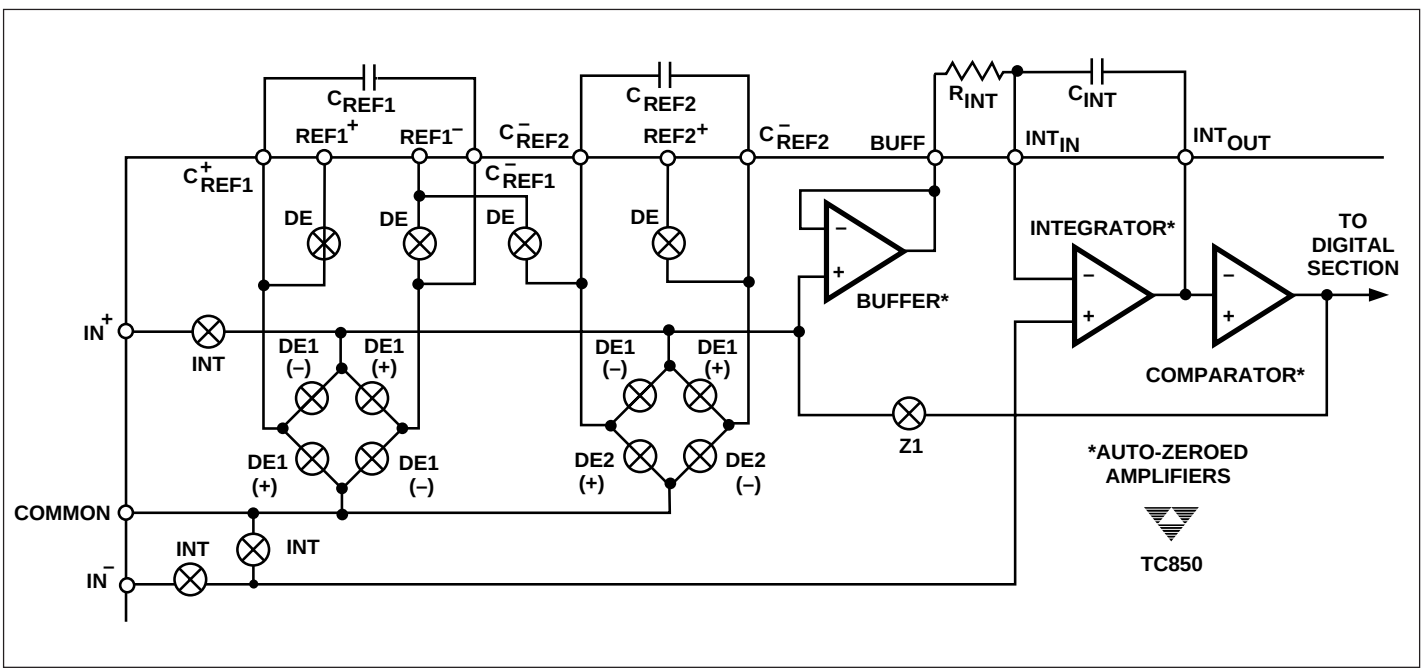


Figure 3. Analog Section Simplified Schematic

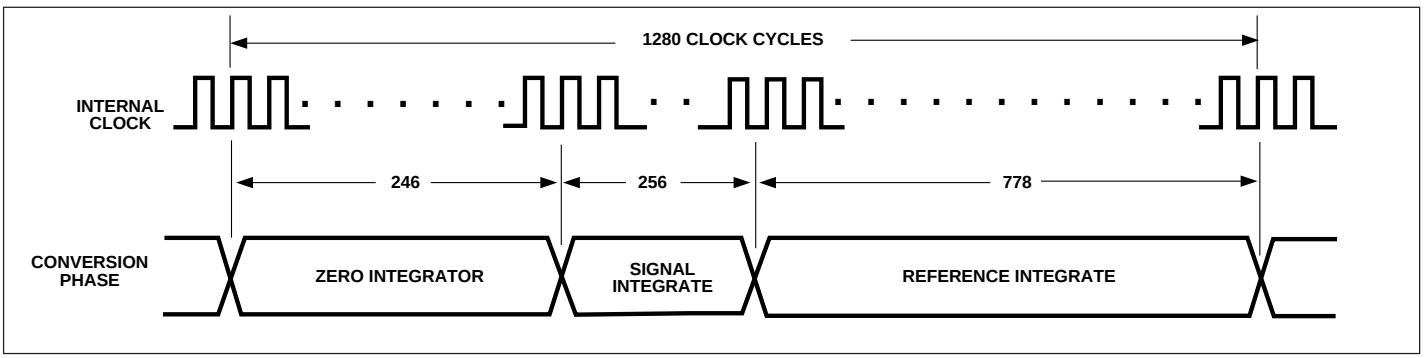


Figure 4. Conversion Timing

Zero-Integrator Phase

During the zero-integrator phase, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero-input condition. At the same time, a feedback loop is closed around the input buffer, integrator, and comparator. The feedback loop ensures the integrator output is near 0V before the signal-integrate phase begins.

During this phase, a chopper-stabilization technique is used to cancel offset errors in the input buffer, integrator, and comparator. Error voltages are stored on the C_{BUFF}, C_{INT}, and COMP capacitors. The zero-integrate phase requires 246 clock cycles.

Signal-Integrate Phase

The zero-integrator loop is opened and the internal differential inputs are connected to IN^+ and IN^-. The differential input signal is integrated for a fixed time period. The TC850 signal-integrate period is 256 clock periods, or counts. The crystal oscillator frequency is ÷4 before clocking the internal counters.

The integration time period is:

$$t_{SI} = \frac{4}{f_{OSC}} \times 256$$

Reference-Integrate Phase

During reference-integrate phase, the charge stored on the integrator capacitor is discharged. The time required to discharge the capacitor is proportional to the analog input voltage.

The reference integrate phase is divided into three subphases: (1) fast, (2) slow, and (3) overrange deintegrate.

During fast deintegrate, V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously-charged reference capacitor (C_{REF1}). The integrator capacitor is rapidly discharged for a maximum of 512 internal clock pulses, yielding 9 bits of resolution.

During the slow deintegrate phase, the internal V_{IN}^+ node is now connected to the C_{REF2} capacitor, and the residual charge on the integrator capacitor is further discharged a maximum of 64 clock pulses. At this point, the analog input voltage has been converted with 15 bits of resolution.

If the analog input is greater than full scale, the TC850 performs up to three overrange deintegrate subphases. Each subphase occupies a maximum of 64 clock pulses. The overrange feature permits analog inputs up to 192 LSBs greater than full scale to be correctly converted. This feature permits the user to digitally null up to 192 counts of input offset, while retaining full 15-bit resolution.

In addition to 512 counts of fast, 64 counts of slow, and 192 counts of overrange deintegrate, the reference-integrate phase uses 10 clock pulses to permit internal nodes to settle. Therefore, the reference integrate cycle occupies 778 clock pulses.

Pin Description (Analog)

Differential Inputs (IN^+ and IN^-)

The analog signal to be measured is applied at the IN^+ and IN^- inputs. The differential input voltage must be within the common-mode range of the converter. The input common-mode range extends from V_{DD} –1.5V to V_{SS} +1.5V. Within this common-mode voltage range, an 86 dB CMRR is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst-case condition exists, for example, when a large, positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its available swing has been used up by the positive common-mode voltage. For applications where maximum common-mode range is critical, integrator swing can be reduced. The integrator output can swing within 0.4V of either supply without loss of linearity.

Differential Reference (V_{REF})

The TC850 requires two reference voltage sources in order to generate the "fast-slow" deintegrate phases. The main voltage reference (V_{REF1}) is applied between the REF_1^+ and REF^- pins. The secondary reference (V_{REF2}) is applied between the REF_2^+ and REF^- pins.

The reference voltage inputs are fully differential, and the reference voltage can be generated anywhere within the power supply voltage of the converter. However, to minimize roll-over error, especially at high conversion rates, keep the reference common-mode voltage (i.e., REF^-) near or at the analog common potential. All voltage reference inputs are high impedance. Average reference input current is typically only 30pA.

Analog Common (COMMON)

Analog common is used as the IN^- return during the zero-integrator and deintegrate phases of each conversion. If IN^- is at a different potential than analog common, a common-mode voltage exists in the system. This signal is rejected by the 86 dB CMRR of the converter. However, in most applications, IN^- will be set at a fixed, known voltage (power supply common, for instance). In this case, analog common should be tied to the same point so that the common-mode voltage is eliminated.

DIGITAL SECTION DESCRIPTION

The TC850 digital section consists of two sets of conversion counters, control and sequencing logic, clock oscillator and divider, data latches, and an 8-bit, 3-state interface bus. A simplified schematic of the bus interface logic is shown in Figure 5.

Clock Oscillator

The TC850 includes a crystal oscillator on-chip. All that is required is to connect a crystal across OSC_1 and OSC_2 pins, and to add two inexpensive capacitors (Figure 1). The oscillator output is ÷ 4 prior to clocking the A/D internal counters. For example, a 100kHz crystal produces a system clock frequency of 25kHz. Since each conversion requires 1280 clock periods, in this case the conversion rate will be 25,000/1280, or 19.5 conversions per second.

In most applications, however, an external clock is divided down from the microprocessor clock. In this case, the OSC_1 pin is used as the external oscillator input and OSC_2 is left unconnected. The external clock driver should swing from digital ground to V_{DD}. The ÷4 function is active for both external clock and crystal oscillator operations.

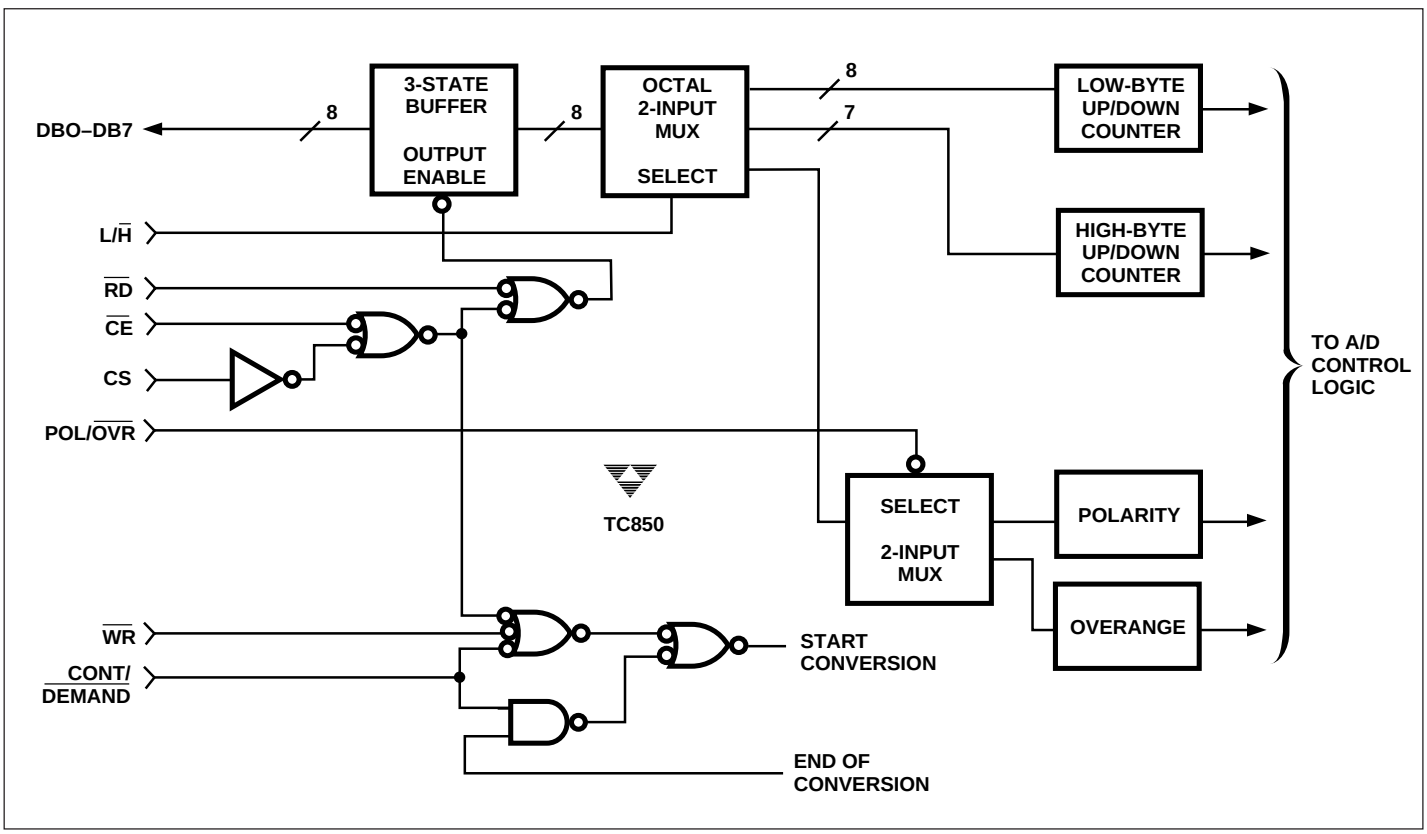


Figure 5. Bus Interface Simplified Schematic

Digital Operating Modes

Two modes of operation are available with the TC850, continuous conversions and on-demand. The operating mode is controlled by the CONT/$\overline{\text{DEMAND}}$ input. The bus interface method is different for continuous and demand modes of operation.

Demand Mode Operation

When CONT/$\overline{\text{DEMAND}}$ is low, the TC850 performs one conversion each time the chip is selected and the $\overline{\text{WR}}$ input is pulsed low. Data is valid on the falling edge of the BUSY output and can be accessed using the interface truth table (Table 1).

Continuous Mode Operation

When CONT/$\overline{\text{DEMAND}}$ is high, the TC850 continuously performs conversions. Data will be valid on the falling edge of the BUSY output, and remains valid for 443-1/2 clock cycles.

The low/high (L/$\overline{\text{H}}$) byte-select and overrange/polarity (OVR/$\overline{\text{POL}}$) inputs are disabled during continuous mode operation. Data must be read in three consecutive bytes, as shown in Table I.

NOTE: In continuous mode, the conversion result must be read within 443-1/2 clock cycles of the BUSY output falling edge. After this time (i.e., 1/2 clock cycle before BUSY goes high) the internal counters are reset and the data is lost.

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Table 1. Bus Interface Truth Table

$\overline{\text{CE}}$•CS	$\overline{\text{RD}}$	CONT/$\overline{\text{DEMAND}}$	L/$\overline{\text{H}}$	OVR/$\overline{\text{POL}}$	DB7	DB6–DB0
Pins 1 and 2	**Pin 4**	**Pin 5**	**Pin 7**	**Pin 6**	**Pin 8**	**Pin 9-Pin 15 (Note 1)**
0	0	0	0	0	"1" = Input Positive	Data Bits 14 – 8
0	0	0	0	1	"1" = Input Overrange (Note 2)	Data Bits 14 – 8
0	0	0	1	X	Data Bit 7	Data Bits 6 – 0
0	0	1	X	X	Note 3	
0	1	X	X	X	High-Impedance State	
1	X	X	X	X	High-Impedance State	

NOTES: 1. Pin numbers refer to 40-pin DIP.

2. Extended overrange operation: Although rated at 15 bits (±32,767 counts) of resolution, the TC850 provides an additional 191 counts above full scale. For example, with a full-scale input of 3.2768V, the maximum analog input voltage which will be properly converted is 3.2958V. The extended resolution is signified by the overrange bit being high and the low-order byte contents being between 0 and 190. For example, with a full-scale voltage of 3.2768V:

V_{IN}	Overrange Bit	Low Byte	Data Bits 14–8
3.2767V	Low	255_{10}	127_{10}
3.2768V	High	000_{10}	0_{10}
3.2769V	High	001_{10}	0_{10}
3.2867V	High	099_{10}	0_{10}

3. Continuous mode data transfer:
   a. In continuous mode, data MUST be read in three sequential bytes after the BUSY output goes low:
      (1) The first byte read will be the high-order byte, with DB7 = polarity.
      (2) The second byte read will contain the low-order byte.
      (3) The third byte read will again be the high-order byte, but with DB7 = overrange.
   b. All three data bytes must be read within 443-1/2 clock cycles after the falling edge of BUSY.
   c. The $\overline{\text{RD}}$ input must go high after each byte is read, so that the internal byte counter will be incremented. However, the CS and $\overline{\text{CE}}$ inputs can remain enabled through the entire data transfer sequence.

Pin Description (Digital)

Chip Select and Chip Enable (CS and $\overline{CE}$)

The CS and $\overline{CE}$ inputs permit easy interfacing to a variety of digital bus systems. $\overline{CE}$ is active LOW while CS is active HIGH. These inputs are logically ANDed internally and are used to enable the $\overline{RD}$ and $\overline{WR}$ inputs.

Write Enable Input ($\overline{WR}$)

The write input is used to initiate a conversion when the TC850 is in demand mode. CS and $\overline{CE}$ must be active for the $\overline{WR}$ input to be recognized. The status of the data bus is meaningless during the $\overline{WR}$ pulse, because no data is actually written into the TC850.

Read Enable Input ($\overline{RD}$)

The read input, combined with CS and $\overline{CE}$, enables the 3-state data bus outputs. Also, in continuous mode, the rising edge of the $\overline{RD}$ input activates an internal byte counter to sequentially read the three data bytes.

Low/High Byte Select (L/$\overline{H}$)

The L/$\overline{H}$ input determines whether the low (least significant) byte or high (most significant) byte of data is placed on the 3-state data bus. This input is meaningful only when the TC850 is in the demand mode. In the continuous mode, data must be read in three predetermined bytes, so the L/$\overline{H}$ input is ignored.

Overrange/Polarity Bit Select (OVR/$\overline{POL}$)

The TC850 provides 15 bits of resolution, plus polarity and overrange bits. Thus, 17 bits of information must be transferred on an 8-bit data bus. To accomplish this, the overrange and polarity bits are multiplexed onto data bit DB7 of the most significant byte. When OVR/$\overline{POL}$ is HIGH, DB7 of the high byte contains the overrange status (HIGH = analog input overrange, LOW = input within full scale). When OVR/$\overline{POL}$ is LOW, DB7 is HIGH for positive analog input polarity and LOW for negative polarity. The OVR/$\overline{POL}$ input is meaningful only when CS, $\overline{CE}$, and $\overline{RD}$ are active, and L/$\overline{H}$ is LOW (i.e., the most significant byte is selected). OVR/$\overline{POL}$ is ignored when the TC850 is in continuous mode.

Continuous/Demand Mode Input (CONT/$\overline{DEMAND}$)

This input controls the TC850 operating mode. When CONT/$\overline{DEMAND}$ is HIGH, the TC850 performs conversions continuously. In continuous mode, data must be read in the prescribed sequence shown in Table I. Also, all three data bytes must be read within 443-1/2 internal clock cycles after the BUSY output goes low. After 443-1/2 clock cycles data will be lost.

When CONT/$\overline{DEMAND}$ is LOW, the TC850 begins a conversion each time CS and $\overline{CE}$ are active and $\overline{WR}$ is pulsed LOW. The conversion is complete and data can be read after the falling edge of the BUSY output. In demand mode, data can be read in any sequence, and remains valid until WR is again pulsed LOW.

Busy Output (BUSY)

The BUSY output is used to convey an end-of-conversion to external logic. BUSY goes HIGH at the beginning of the deintegrate phase and goes LOW at the end of the conversion cycle. Data is valid on the falling edge of BUSY. The output-high period is fixed at 836 clock periods, regardless of the analog input value. BUSY is active during continuous and demand mode operation.

This output can also be used to generate an end-of-conversion interrupt in µP-based systems. Noninterrupt-driven systems can poll BUSY to determine when data is valid.

ANALOG SECTION APPLICATIONS

Component Selection

Reference Voltage

The typical value for reference voltage V_{REF1} is 1.6384V. This value yields a full-scale voltage of 3.2768V and resolution of 100µV per step. The V_{REF2} value is derived by dividing V_{REF1} by 64. Thus, typical V_{REF2} value is 1.6384V/64, or 25.6mV. The V_{REF2} value should be adjusted within ±1% to maintain 15-bit accuracy for the total conversion process; i.e.,

$$V_{REF2} = \frac{V_{REF1}}{64} \pm 1\%.$$

The reference voltage is not limited to exactly 1.6384V, however, because the TC850 performs a ratiometric conversion. Therefore, the conversion result will be:

$$\text{Digital counts} = \frac{V_{IN}}{V_{REF1}} \bullet 16384.$$

The full-scale voltage can range from 3.2V to 3.5V. Full-scale voltages of less than 3.2V will result in increased noise in the least significant bits, while a full-scale above 3.5V will exceed the input common-mode range.

Integration Resistor

The TC850 buffer supplies 25µA of integrator charging current with minimal linearity error. R_{INT} is easily calculated:

$$R_{INT} = \frac{V_{FULL\ SCALE}}{25\ \mu A}.$$

For a full-scale voltage of 3.2768V, values of R_{INT} between 120kΩ and 150kΩ are acceptable.

Integration Capacitor

The integration capacitor should be selected to produce an integrator swing of ≈4V at full scale. The capacitor value is easily calculated:

$$C = \frac{V_{FS}}{R_{INT}} \bullet \frac{4 \bullet 256}{4V \bullet f_{CLOCK}},$$

where f_{CLOCK} is the crystal or external oscillator frequency and V_{FS} is the maximum input voltage.

The integration capacitor should be selected for low dielectric absorption to prevent roll-over errors. A polypropylene, polyester or polycarbonate dielectric capacitor is recommended.

Reference Capacitors

The reference capacitors require a low leakage dielectric, such as polypropylene, polyester or polycarbonate. A value of 1µF is recommended for operation over the temperature range. If high-temperature operation is not required, the C_{REF} values can be reduced.

Auto-Zero Capacitors

Five capacitors are required to auto-zero the input buffer, integrator amplifier, and comparator. Recommended capacitors are 0.1µF film dielectric (such as polyester or polypropylene). Ceramic capacitors are not recommended.

DIGITAL SECTION APPLICATION

Oscillator

The TC850 may operate with a crystal oscillator. The crystal selected should be designed for a Pierce oscillator, such as an AT-cut quartz crystal. The crystal oscillator schematic is shown in Figure 6.

Since low frequency crystals are very large and ceramic resonators are too lossy, the TC850 clock should be derived from an external source, such as a microprocessor clock. The clock should be input on the OSC_1 pin and no connection should be made to the OSC_2 pin. The external clock should swing between DGND and V_{DD}.

Since oscillator frequency is ÷ 4 internally and each conversion requires 1280 internal clock cycles, the conversion time will be:

$$\text{Conversion time} = f_{CLOCK} \times 4 \times 1280.$$

An important advantage of the integrating ADC is the ability to reject periodic noise. This feature is most often used to reject line frequency (50Hz or 60Hz) noise. Noise rejection is accomplished by selecting the integration period equal to one or more line frequency cycles. The desired clock frequency is selected as follows:

$$f_{CLOCK} = f_{NOISE} \times 4 \times 256,$$

where f_{NOISE} is the noise frequency to be rejected, 4 represents the clock divider, and 256 is the number of integrate cycles.

For example, 60Hz noise will be rejected with a clock frequency of 61.44kHz, giving a conversion rate of 12 conversions/sec. Integer submultiples of 61.44kHz (such as 30.72kHz, etc.) will also reject 60Hz noise. For 50Hz noise rejection, a 51.2kHz frequency is recommended.

If noise rejection is not important, other clock frequencies can be used. The TC850 will typically operate at conversion rates ranging from 3 to 40 conversions/sec, corresponding to oscillator frequencies from 15.36kHz to 204.8kHz.

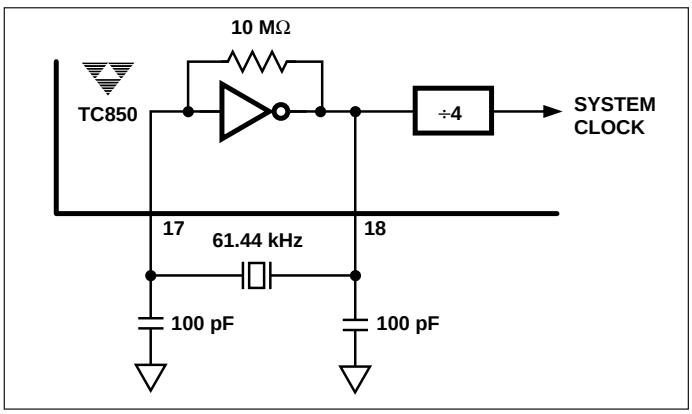


Figure 6. Crystal Oscillator Schematic

Data Bus Interfacing

The TC850 provides an easy and flexible digital interface. A 3-state data bus and six control inputs permit the TC850 to be treated as a memory device, in most applications. The conversion result can be accessed over an 8-bit bus or via a µP I/O port.

A typical µP bus interface for the TC850 is shown in Figure 7. In this example, the TC850 operates in the demand mode, and conversion begins when a write operation is performed to any decoded address space. The BUSY output interrupts the µP at the end-of-conversion.

The A/D conversion result is read as three memory bytes. The two LSBs of the address bus select high/low byte and overrange/polarity bit data, while high-order address lines enable the $\overline{CE}$ input.

Figure 8 shows a typical interface to a µP I/O port or single-chip µC. The TC850 operates in the continuous mode, and can either interrupt the µC/µP or be polled with an input pin.

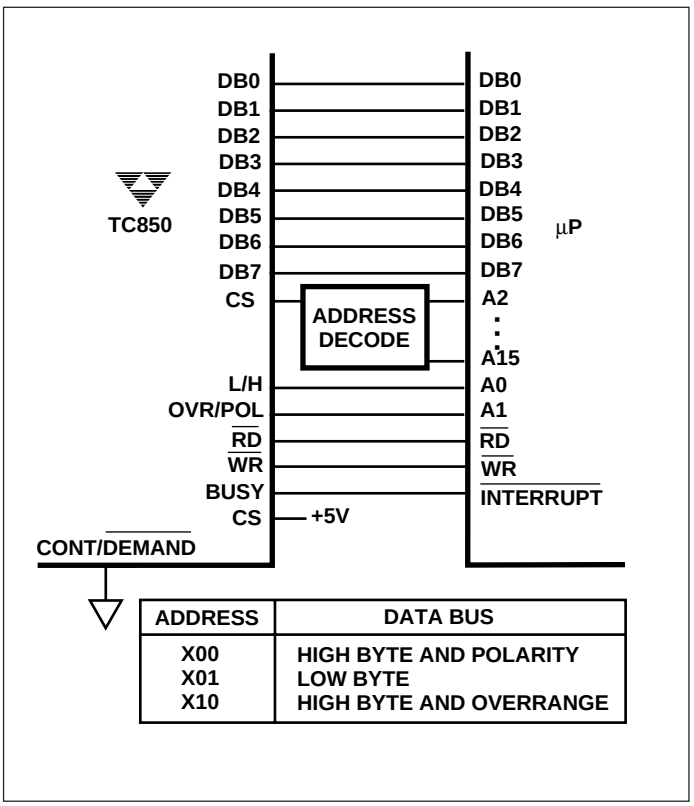


Figure 7. Interface to Typical µP Data Bus

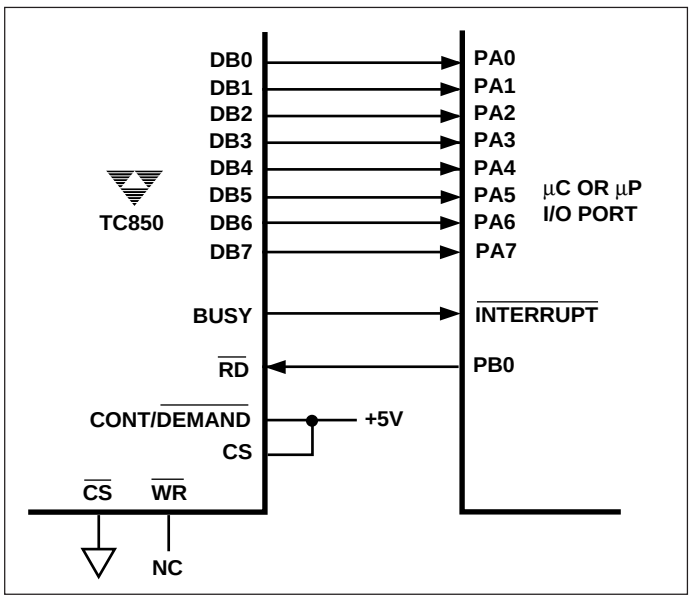


Figure 8. Interface to Typical µP I/O Port or Single-Chip µC

Since the PA0–PA7 inputs are dedicated to reading A/D data, the A/D CS/CE inputs can be enabled continuously. In continuous mode, data must be read in 3 bytes, as shown in Table I. The required RD pulses are provided by a µC/µP output pin.

The circuit of Figure 8 can also operate in the demand mode, with the start-up conversion strobe generated by a µC/µP output pin. In this case, the L/H and CONT/DEMAND inputs can be controlled by I/O pins and the RD input connected to digital ground.

Demand Mode Interface Timing

When CONT/DEMAND input is LOW, the TC850 performs a conversion each time CE and CS are active and WR is strobed LOW.

The demand mode conversion timing is shown in Figure 9. BUSY goes LOW and data is valid 1155 clock pulses after WR goes LOW. After BUSY goes low, 125 additional clock cycles are required before the next conversion cycle will begin.

Once conversion is started, WR is ignored for 1100 internal clock cycles. After 1100 clock cycles, another WR pulse is recognized and initiates a new conversion when the present conversion is complete. A negative edge on WR is required to begin conversion. If WR is held LOW, conversions will not occur continuously.

The A/D conversion data is valid on the falling edge of BUSY, and remains valid until one-half internal clock cycle before BUSY goes HIGH on the succeeding conversion. BUSY can be monitored with an I/O pin to determine end of conversion, or to generate a µP interrupt.

In demand mode, the three data bytes can be read in any desired order. The TC850 is simply regarded as three bytes of memory and accessed accordingly. The bus output timing is shown in Figure 10.

Continuous Mode Interface Timing

When the CONT/DEMAND input is HIGH, the TC850 performs conversions continuously. Data will be valid on the falling edge of BUSY, and all three bytes must be read within 443-1/2 internal clock cycles of BUSY going LOW. The timing diagram is shown in Figure 11.

In continuous mode, OVR/POL and L/H byte-select inputs are ignored. The TC850 automatically cycles through three data bytes, as shown in Table I. Bus output timing in the continuous mode is shown in Figure 12.

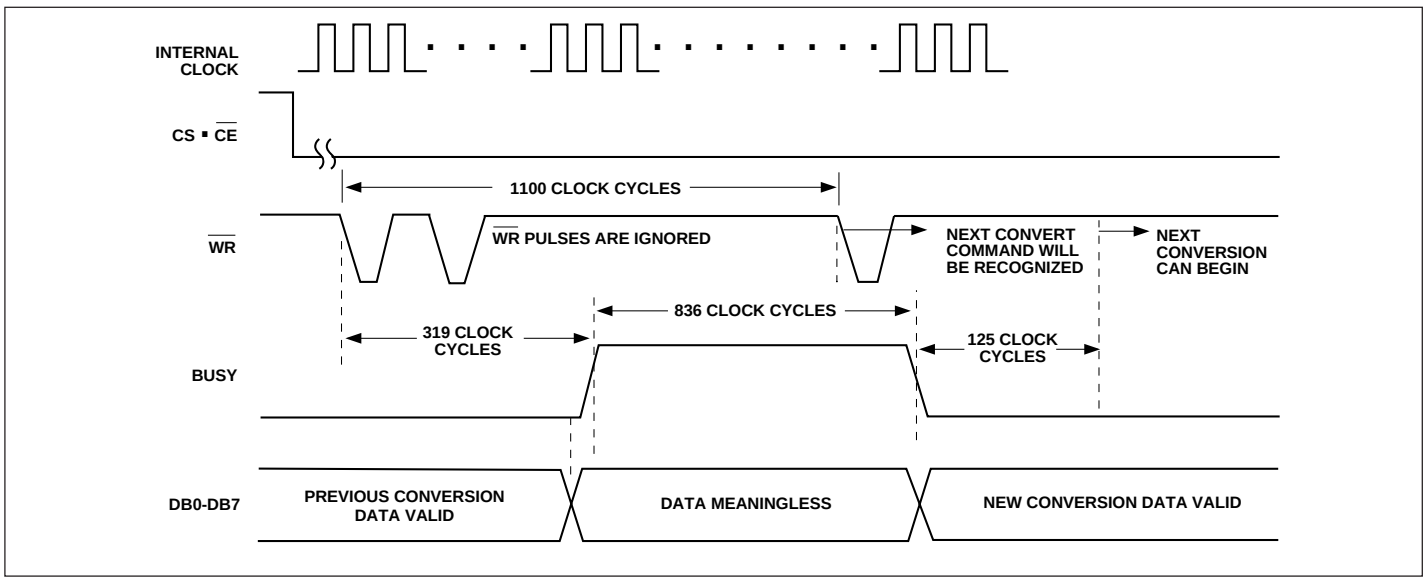
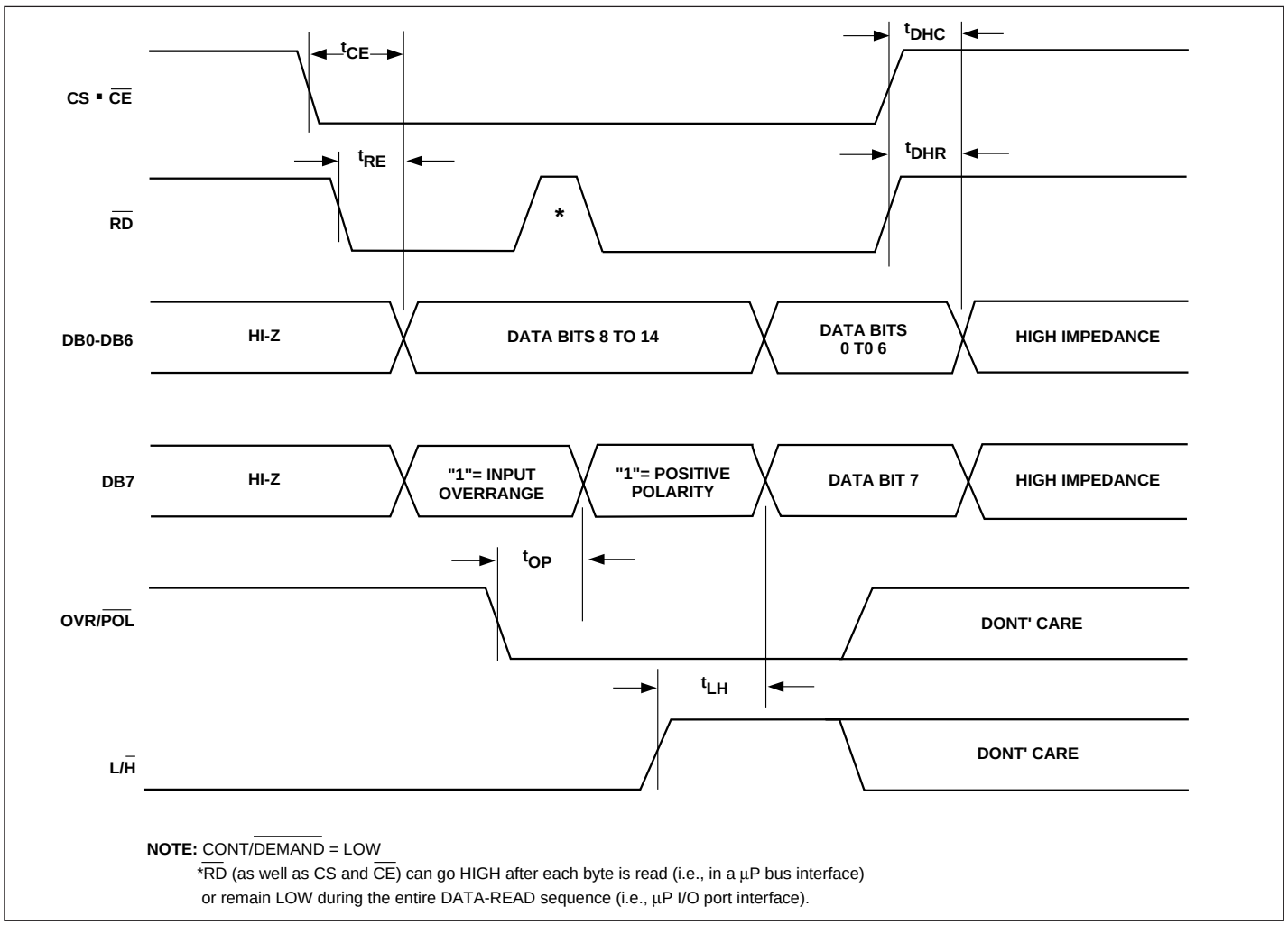


Figure 9. Conversion Timing, Demand Mode



NOTE: CONT/DEMAND = LOW
*RD (as well as CS and CE) can go HIGH after each byte is read (i.e., in a µP bus interface)
or remain LOW during the entire DATA-READ sequence (i.e., µP I/O port interface).

Figure 10. Bus Output Timing, Demand Mode

TC850

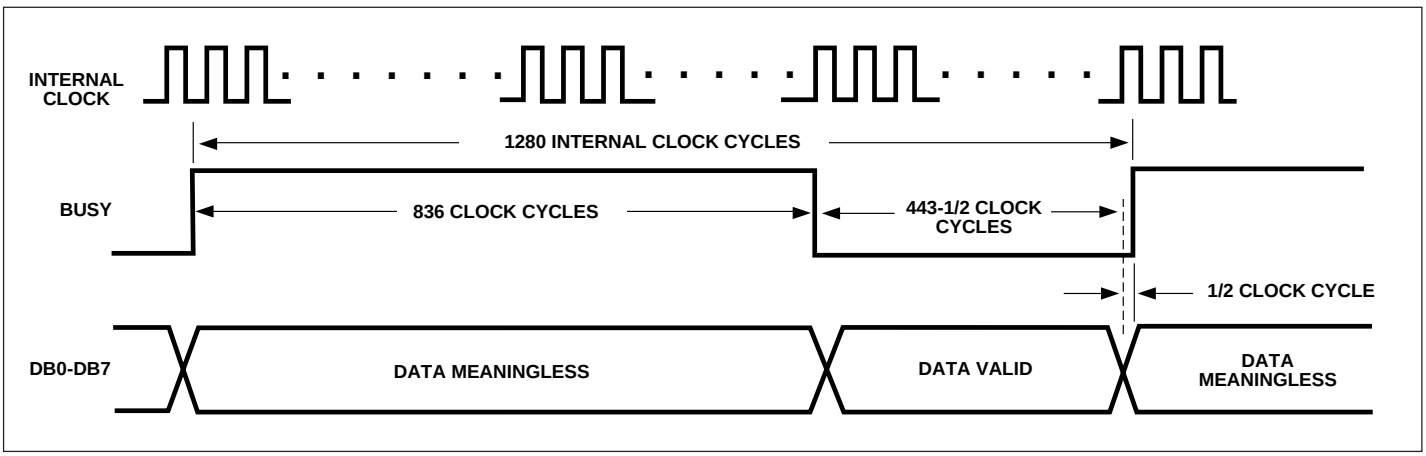


Figure 11. Conversion Timing, Continuous Mode

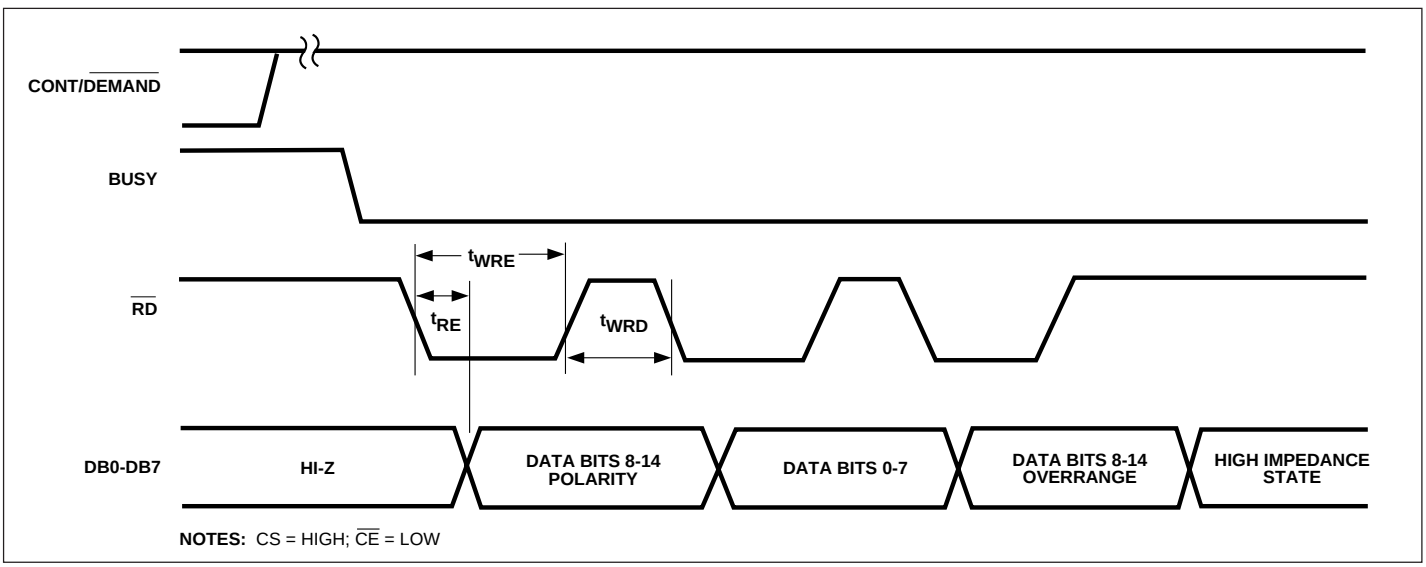


Figure 12. Bus Output Timing, Continuous Mode