64K BIT (8K WORD X 8 BIT) MASK PROGRAMMABLE ROM

N CHANNEL SILICON GATE

TMM2364P

DESCRIPTION

The TMM2364P is a 65536 bit read only memory organized as 8192 words by 8 bits with a low bit cost, thus being most suitable for use in programming of production apparatus using micro-processor.

Consisting of static memory cells and clocked peripheral circuitry, the TMM2364P provides a high speed and low power dissipation (access time 250ns, operating current 40mA).

The TMM2364P also features an automatic stand-by power mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced from 40mA to 15mA. Output Enable ($\overline{OE}$) is effective in preventing data confliction on a common bus line.

The TMM2364P uses the address latch system that the falling edge of $\overline{CE}$ latches all inputs except for $\overline{OE}$, thus can be easily connected to a system where address and data buses are commonly used.

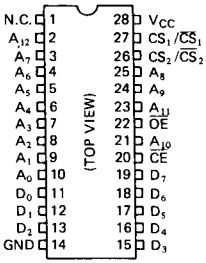
The TMM2364P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production of high performance.

The TMM2364P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

FEATURES

- Single 5V ± 10% power Supply
- Access Time: 250ns max.
- Low Power Dissipation
  - Average Current: 40mA max.
  - Standby Current: 15mA max.
- Input and Output: TTL Compatible
- Three State Outputs: Wired OR Capability
- Edge Enabled Operation: $\overline{CE}$
- Output Buffer Control: $\overline{OE}$
- Programmable Chip Select: CS_1, CS_2
  - Easy Memory Expansion
- Pin Compatible with i2364
- Inputs protected: All inputs have protection against static charge.

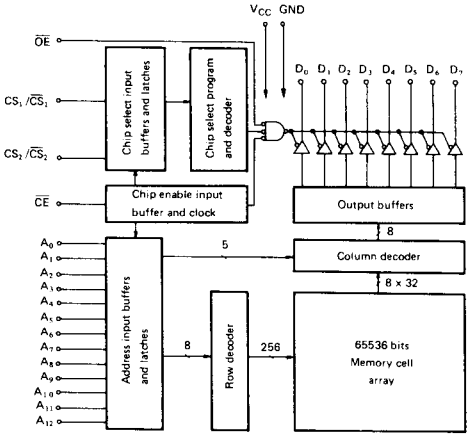
PIN CONNECTION



PIN NAMES

$A_0 \sim A_{12}$	Address inputs
$D_0 \sim D_7$	Data outputs
CS/$\overline{CS}$	Chip select inputs
$\overline{OE}$	Output enable inpu
$\overline{CE}$	Chip enable input
N.C.	No connection
V_{CC}	Power supply terminal
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input and Output Voltage	−0.5 ~ 7.0	V
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STRG}	Storage Temperature	−55 ~ 150	°C
T_{SD}	Soldering Temperature · Time	260 · 10	°C · sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	–	2.2	–	V_{CC} + 1	V
V_{IL}	Input Low Voltage	–	−0.5	–	0.8	V
V_{CC}	Power Supply Voltage	–	4.5	5.0	5.5	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_{IH}	Input High Current	V_{IN} = 5.5V		–	0.05	10	μA
I_{IL}	Input Low Current	V_{IN} = GND		–	−0.05	−10	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA		2.4	3.3	–	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA		–	0.3	0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 5.5V	$\overline{CE}$ = 2.2V or	–	0.05	10	μA
I_{LOL}		V_{OUT} = 0.4V	$\overline{OE}$ = 2.2V	–	−0.1	−20	μA
I_{CC1}	Standby Current	$\overline{CE}$ = 2.2V		–	8	15	mA
I_{CC2}	Average Current	t_{CYC} = 350ns, I_{OUT} = 0mA		–	20	40	mA

* Typical values are at Ta = 25°C and V_{CC} = 5V.

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{CE}	$\overline{CE}$ pulse width	–	250	–	–	ns
t_{AS}	Address Setup Time	–	0	–	–	ns
t_{AH}	Address Hold Time	–	50	–	–	ns
t_{ACC}	Access Time	–	–	150	250	ns
t_{OO}	Output Delay Time from $\overline{OE}$	–	–	50	120	ns
t_{OD}	Output Turn off Delay	–	–	40	70	ns
t_{CC}	$\overline{CE}$ off Time	–	90	–	–	ns
t_{CYC}	Cycle Time	t_{AS} = 0ns, t_r, t_f = 5ns	350	–	–	ns

* Typical values are at Ta = 25°C and V_{CC} = 5V.

A.C. TEST CONDITIONS

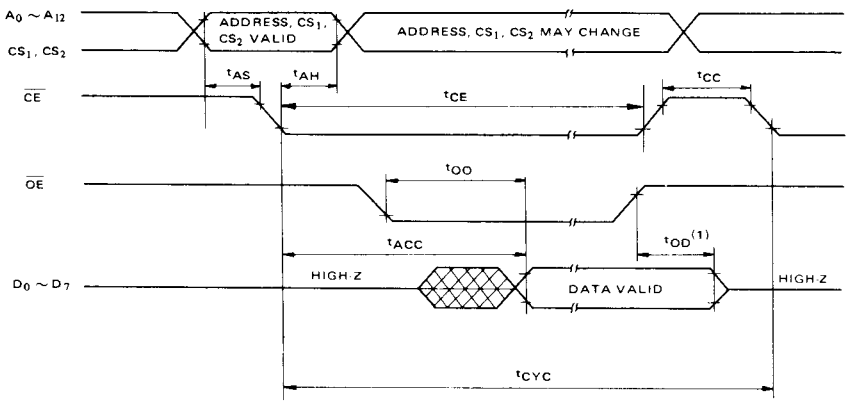
- Output Load: 1TTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%): 5ns
- Input Pulse Levels: 0.8 ~ 2.4V
- Timing Measurement Reference Levels: Input; 1V and 2.2V
  Output; 0.8V and 2.0V

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = A.C. GND	–	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = A.C. GND	–	8	15	pF

Note: This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



Note (1) t_{OD} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

OPERATION MODE

$\overline{CE}$	CS_1, CS_2, Address	$\overline{OE}$	OUTPUT	MODE
H	(1)	(1)	High Z	Standby
↑	Valid	(1)	High Z	Latch
L	(2)	L	Data out	Read

Note (1) Don't care
(2) CS_1, CS_2, Address may change after t_{AH}.

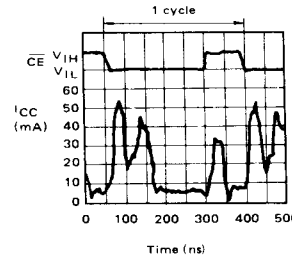
APPLICATION INFORMATION

1. POWER SUPPLY DECOUPLING

The operating current I_{CC} waveforms for TMM2364P are shown in Fig. 1, 2.

The TMM2364P is a clocked device, so the transient current peaks are produced on the $\overline{CE}$ transition and $\overline{CE}$ active level.

The I_{CC} current transients require adequate decoupling of V_{CC} power supply.



Fgi. 1 I_{CC} vs time (CS: Select)

2. POWER ON

The TMM2364P requires initialization prior to normal operation. Two initialization methods are as follows:

(1) A minimum 100 μs time delay is required after the application of V_{CC} (+5V) before proper device operation is achieved. And during this period, $\overline{CE}$ must be at V_{IH} level.

(2) A minimum 100 μs time delay is required after the application of V_{CC} (5V), and then a minimum of one initialization cycle must be performed before proper device operation is acheived.

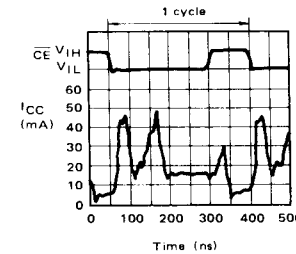


Fig. 2 I_{CC} vs time (CS: Deselect)

Initialization cycle: An initialization cycle is one Chip Enable clock cycle from the first down edge of the $\overline{CE}$ till the next down edge.