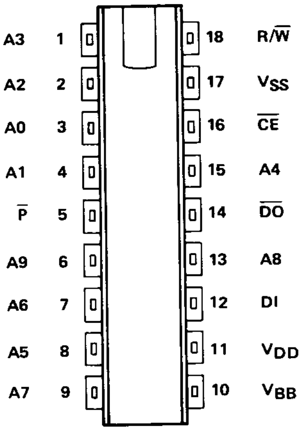
MOS LSI

TMS 1103 JL, NL; TMS 1103-1 JL, NL 1024-BIT DYNAMIC RANDOM-ACCESS MEMORIES

BULLETIN NO. DL-S 7512234, JANUARY 1975

- 1024 x 1-Bit Organization
- Low Power Dissipation
- Input Interface
  - Fully Decoded, On-Chip Address Decode
  - Static Charge Protection
- Output Interface
  - OR-Tie Capability
- Address Access Time
  - TMS 1103 JL, NL . . . 300 ns
  - TMS 1103-1 JL, NL . . . 150 ns
- P-Channel Silicon-Gate Technology
- 18-Pin 300-Mil Dual-In-Line Packages

18-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)



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description

The TMS 1103 JL, NL and TMS 1103-1 JL, NL are monolithic random-access memory devices organized as 1024 one-bit words. Outputs may be OR-tied for simple memory expansion since a particular device can be activated by a chip-enable signal. Stored information is read nondestructively and all cells in any row are refreshed by addressing that row at least once every 2-milliseconds for the TMS 1103, 1-millisecond for the TMS 1103-1. These RAMs are fabricated with P-channel silicon-gate enhancement-type technology. Two power supplies and three control clock signals are required with address inputs decoded on the chip. The TMS 1103-1 is a faster-access version of the TMS 1103 with improved cycle times. The TMS 1103 and TMS 1103-1 are offered in both 18-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages.

operation

addresses (A0-A9)

Address terminals are used to activate a particular cell in a 32 x 32 array. Each row address (A0—A4) and each column address (A5—A9) of 5 bits uniquely specify a 10-bit address for a single memory cell. All address signals must be stable during transitions of the chip-enable, read/write, or data-in control signals.

chip enable ($\overline{CE}$)

The chip-enable terminal enables one particular device of an array whose outputs are connected to a common data bus. Chip enable must be low during any read or write interval to allow data to enter or exit.

precharge ($\overline{P}$)

The precharge terminal must be low at the start of any read or write cycle and remain low for a specified time interval after chip enable drops to a low. This overlap interval must be maintained between a specified minimum and maximum time in order to maintain the integrity of stored data.

read/write ($R/\overline{W}$)

The read/write input terminal gates data out of or into the addressed memory cell. Read/write is low when data is written and high during a read interval.

data in (DI)

The data-in terminal connects the incoming data bus to the addressed cell for a write operation.

data out ($\overline{DO}$)

Stored data appears at the data-out terminal as the complement of the data-in logic level. Information on the data-out terminal is sensed just prior to the rise of chip enable in a read-only cycle and prior to the fall of read/write in a read, modify write cycle.

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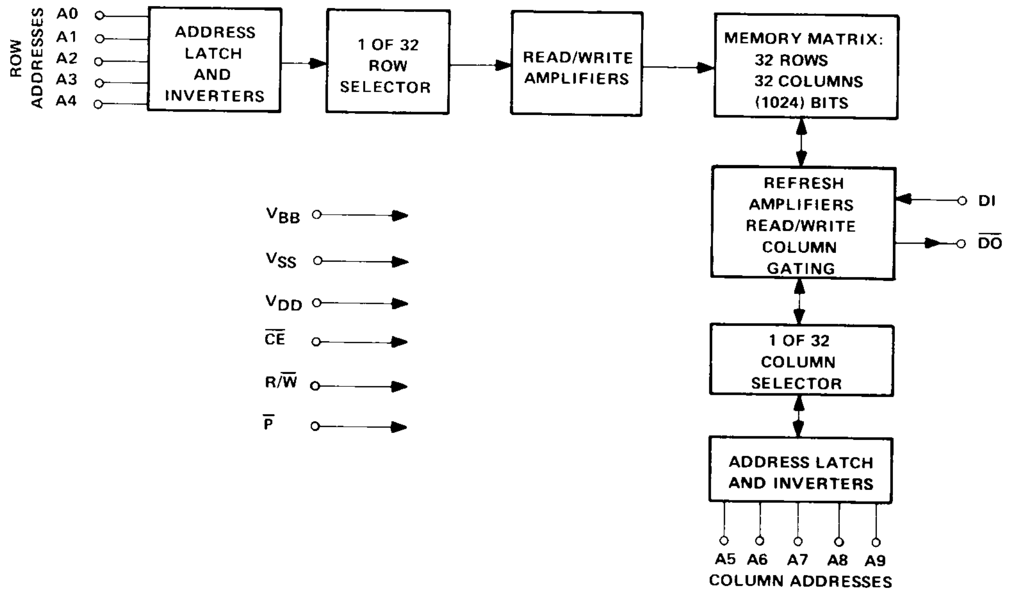
functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)		−25 to 0.3 V
Supply voltage, V_{SS} (see Note 1)		−25 to 0.3 V
Input voltage (any input)		−25 to 0.3 V
Continuous power dissipation		1 W
Operating free-air temperature range:	TMS 1103	0°C to 70°C
	TMS 1103-1	0°C to 55°C
Storage temperature range		−65°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-positive supply voltage, V_{BB} (substrate). Throughout the remainder of this data sheet, voltage values are with respect to V_{DD}.

recommended operating conditions

PARAMETER	TMS 1103			TMS 1103-1			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		0			0		V
Supply voltage, V_{SS}	15.2	16	16.8	18	19	20	V
Supply voltage, $V_{BB}-V_{SS}$ (see Note 2)	3		4	3		4	V
Operating free-air temperature, T_A	0		70	0		55	°C

NOTE 2. $V_{BB}-V_{SS}$ supply should be applied at the same time as or before V_{SS}.

electrical characteristics at specified free-air temperatures
V_{SS} = 16.8 V, ($V_{BB}-V_{SS}$) = 3 V, V_{DD} = 0 V (TMS 1103 JL, NL)
V_{SS} = 20 V, ($V_{BB}-V_{SS}$) = 3 V, V_{DD} = 0 V (TMS 1103-1 JL, NL)

PARAMETER		TEST CONDITIONS†	TMS 1103 MIN	TMS 1103 TYP‡	TMS 1103 MAX	TMS 1103-1 MIN	TMS 1103-1 TYP‡	TMS 1103-1 MAX	UNIT
V_{IH}	High-level input voltage	T_A = MIN	V_{SS} −1		V_{SS} +1	V_{SS} −1		V_{SS} +1	V
		T_A = MAX	V_{SS} −0.7		V_{SS} +1	V_{SS} −1		V_{SS} +1	
V_{IL}	Low-level input voltage (all addresses and data-in lines)	T_A = MIN	V_{SS} −17		V_{SS} −14.2	V_{SS} −20		V_{SS} −18	V
		T_A = MAX	V_{SS} −17		V_{SS} −14.5	V_{SS} −20		V_{SS} −18	
V_{IL}	Low-level input voltage (precharge, chip-enable, and read/write inputs) (see Note 3)	T_A = MIN	V_{SS} −17		V_{SS} −14.7	V_{SS} −20		V_{SS} −18	V
		T_A = MAX	V_{SS} −17		V_{SS} −15	V_{SS} −20		V_{SS} −18	
V_{OH}	High-level output voltage	R_L = 100 Ω, T_A = 25°C	60	90	500	115	130	900	mV
		R_L = 100 Ω, T_A = MAX	50	80	500	90	115	900	
I_I	Input current	V_I = 0 V, T_A = MIN to MAX			1			10	μA
I_{OH}	High-level output current	R_L = 100 Ω, T_A = 25°C	600	900	5000	1150	1130	9000	μA
		R_L = 100 Ω, T_A = MAX	500	800	5000	900	1150	9000	
$I_{O(off)}$	Off-state output current	V_O = 0 V, T_A = MIN to MAX			1			10	μA
I_{BB}	Supply current from V_{BB}	T_A = MIN to MAX			100			100	μA
$I_{DD(1)}$	Supply current from V_{DD} during precharge pulse width	All addresses = 0 V, $\overline{CE}$ at V_{SS}, V_I = V_{SS} Precharge = 0 V, T_A = 25°C		37	56		45	60	mA
$I_{DD(2)}$	Supply current from V_{DD} during precharge and chip-enable overlap	All addresses = 0 V, $\overline{CE}$ at 0 V, V_I = V_{SS} Precharge = 0 V, T_A = 25°C		38	59		50	68	mA
$I_{DD(3)}$	Supply current from V_{DD} during precharge to end of chip enable	Precharge = V_{SS}, $\overline{CE}$ at 0 V, V_I = V_{SS} T_A = 25°C		5.5	11		8.5	11	μA
$I_{DD(4)}$	Supply current from V_{DD} during chip enable to precharge delay	Precharge = V_{SS}, $\overline{CE}$ at V_{SS}, V_I = V_{SS} T_A = 25°C		3	4		3	4	mA
$I_{DD(av)}$	Average supply current from V_{DD} — TMS 1103	$t_{w(\overline{P})}$ = 190 ns, t_c = 580 ns, T_A = 25°C		17	25		20	23	mA
	Average supply current from V_{DD} — TMS 1103-1	$t_{w(\overline{P})}$ = 105 ns, t_c = 340 ns T_A = 25°C							

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at T_A = 25°C.

NOTE 3. The maximum values for V_{IL} for precharge, chip-enable, and read/write of the TMS 1103 may be increased to V_{SS} − 14.2 V at 0°C and V_{SS} − 14.5 V at 70°C (same values as those specified for the address and data-in lines) with a 40-ns degradation (worst case) in $t_{su(ad\,\overline{CE})}$, $t_{d(PL\,\overline{CE}L)}$, $t_{c(rd)}$, $t_{c(RW)}$, $t_{a(ad)}$, and $t_{a(\overline{P})}$.

dynamic electrical characteristics over operating free-air temperature range (unless otherwise noted)
T_A = 0°C to 70°C, V_{SS} = 16 V ± 5%, (V_{BB} – V_{SS}) = 3 V to 4 V, V_{DD} = 0 V (TMS 1103 JL, NL)
T_A = 0°C to 55°C, V_{SS} = 19 V ± 5%, (V_{BB} – V_{SS}) = 3 V to 4 V, V_{DD} = 0 V (TMS 1103-1 JL, NL)

capacitance at 25°C free-air temperature

CHARACTERISTICS		TEST CONDITIONS†	PLASTIC PKG		CERAMIC PKG		UNIT
			TYP	MAX	TYP	MAX	
$C_{i(ad)}$	Address input capacitance	$V_I = V_{SS}$	5	7	10	12	pF
$C_{i(\overline{P})}$	Precharge input capacitance	$V_I = V_{SS}$	15	18	16.5	19.5	pF
$C_{i(\overline{CE})}$	Chip-enable input capacitance	$V_I = V_{SS}$	15	18	18	21	pF
$C_{i(R/\overline{W})}$	Read/write input capacitance	$V_I = V_{SS}$	11	15	15.5	19.5	pF
$C_{i(da)}$	Data input capacitance	$\overline{CE}$ at 0 V, $V_I = V_{SS}$	4	5	6.5	7.5	pF
		$\overline{CE}$ at V_{SS}, $V_I = V_{SS}$	2	4	5.6	6.5	
C_o	Data output capacitance	V_O = 0 V	2	3	6	7	pF

†f = 1 MHz, and all unused pins are at ac ground.

read, write, and read, modify write cycle

PARAMETER		TEST CONDITIONS	TMS 1103		TMS 1103-1		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rfsh)}$	Refresh cycle time	$t_r = t_f$ = 20 ns, C_L = 100 pF (1103), C_L = 50 pF (1103-1), R_L = 100 Ω, v_{ref} = 40 mV (1103), v_{ref} = 80 mV (1103-1)		2		1	ms
$t_{su(ad\text{-}\overline{CE})}$	Address-to-chip-enable setup time		115		30		ns
$t_{h(\overline{CE}\text{-}ad)}$	Chip-enable-to-address hold time		20		10		ns
$t_{d(\overline{P}L\text{-}\overline{CE}L)}$	Precharge low to chip-enable low delay time		125		60		ns
$t_{d(\overline{CE}H\text{-}\overline{P}L)}$	Chip-enable high to precharge low delay time		85		40		ns
$t_{d(\overline{CE}L\text{-}\overline{P}H)1}$	Chip-enable low to precharge high delay time between low reference points		25	75	5	30	ns
$t_{d(\overline{CE}L\text{-}\overline{P}H)2}$	Chip-enable low to precharge high delay time between high reference points			140		85	ns

read cycle

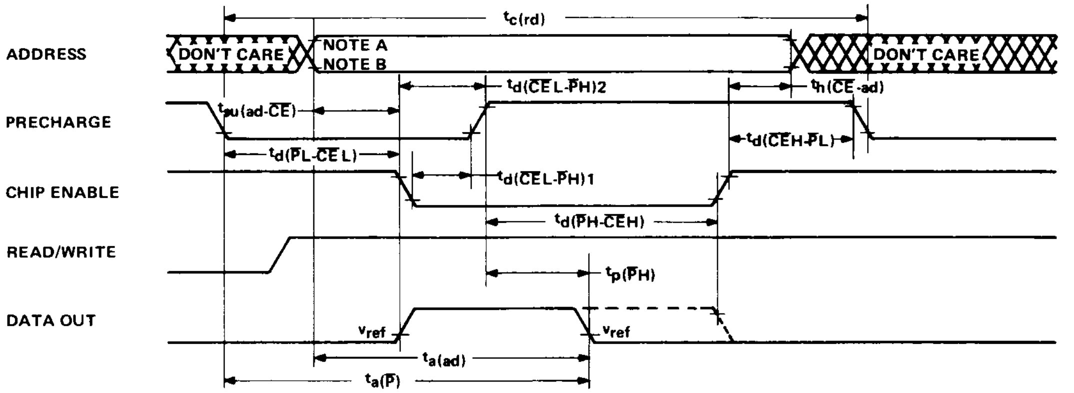
PARAMETER		TEST CONDITIONS	TMS 1103		TMS 1103-1		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	$t_r = t_f$ = 20 ns, C_L = 100 pF (1103), C_L = 50 pF (1103-1), R_L = 100 Ω, v_{ref} = 40 mV (1103), v_{ref} = 80 mV (1103-1)	480		300		ns
$t_{d(\overline{P}H\text{-}\overline{CE}H)}$	Precharge high to chip-enable high delay time		165	500	115	500	ns
$t_{p(\overline{P}H)}$	Precharge high to output propagation delay time			120		75	ns
$t_{a(ad)}$	Access time from address (see Note 4)		300		150		ns
$t_{a(\overline{P})}$	Access time from precharge (see Note 5)		310		180		ns

NOTES:
4. $t_{a(ad)} = t_{su(ad\text{-}\overline{CE})} + t_{f(\overline{CE})} + t_{d(\overline{CE}L\text{-}\overline{P}H)1} + t_{r(\overline{P})} + t_{p(\overline{P}H)}$.
5. $t_{a(\overline{P})} = t_{d(\overline{P}L\text{-}\overline{CE}L)} + t_{f(\overline{CE})} + t_{d(\overline{CE}L\text{-}\overline{P}H)1} + t_{r(\overline{P})} + t_{p(\overline{P}H)}$.

write or read, modify write cycle

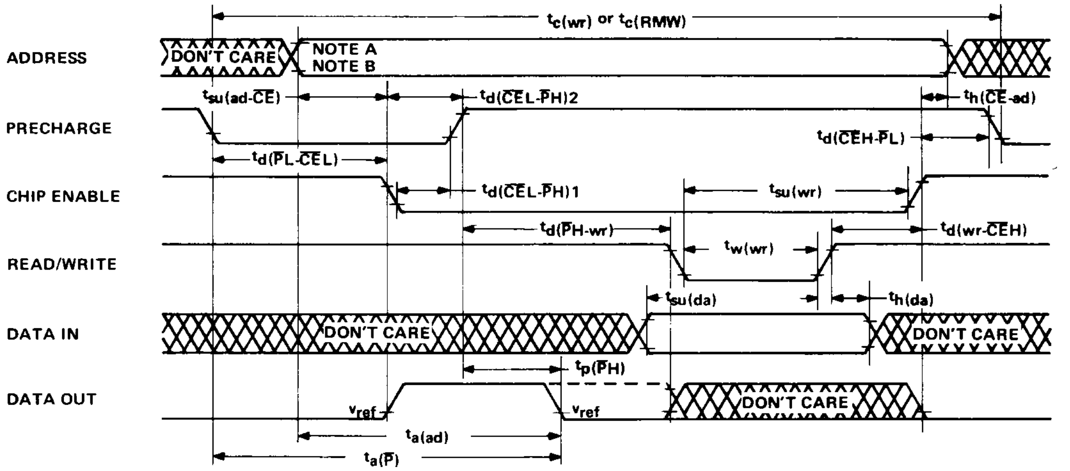
PARAMETER		TEST CONDITIONS	TMS 1103		TMS 1103-1		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	$t_r = t_f$ = 20 ns, C_L = 100 pF (1103), C_L = 50 pF (1103-1), R_L = 100 Ω, v_{ref} = 40 mV (1103), v_{ref} = 80 mV (1103-1)	580		340		ns
$t_{c(RMW)}$	Read, modify write cycle time		580		340		ns
$t_{d(\overline{P}H\text{-}wr)}$	Precharge high to write delay time		165	500	115	500	ns
$t_{w(wr)}$	Write pulse width		50		20		ns
$t_{su(wr)}$	Write setup time		80		20		ns
$t_{su(da)}$	Data setup time		105		40		ns
$t_{h(da)}$	Data hold time		10		10		ns
$t_{p(\overline{P}H)}$	Precharge high to output propagation delay time			120		75	ns
$t_{d(wr\text{-}\overline{CE}H)}$	Write to chip-enable high delay time		0		0		ns

PARAMETER MEASUREMENT INFORMATION



NOTES:
A. The high-level time reference on each waveform except data out is V_{SS} −2 V.
B. The low-level time reference on each waveform except data out is V_{DD} +2 V.

FIGURE 1—READ CYCLE



NOTES:
A. The high-level time reference on each waveform except data out is V_{SS} −2 V.
B. The low-level time reference on each waveform except data out is V_{DD} +2 V.

FIGURE 2 – WRITE OR READ, MODIFY WRITE CYCLE

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