National Semiconductor

TP5088 DTMF Generator for Binary Data

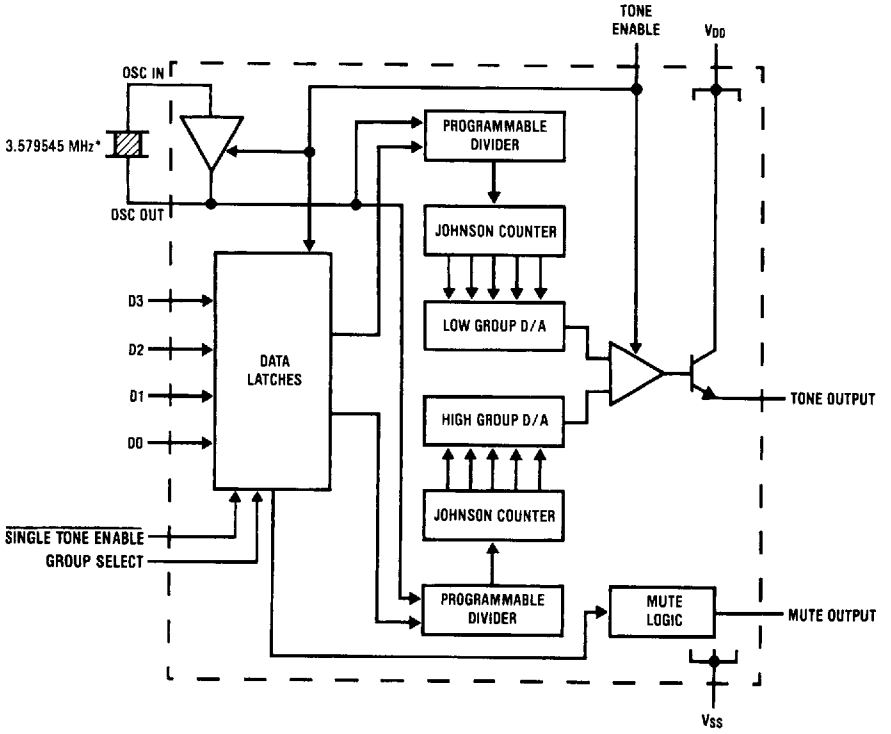
General Description

This CMOS device provides low cost tone-dialing capability in microprocessor-controlled telephone applications. 4-bit binary data is decoded directly, without the need for conversion to simulated keyboard inputs required by standard DTMF generators. With the TONE ENABLE input low, the oscillator is inhibited and the device is in a low power idle mode. On the low-to-high transition of TONE ENABLE, data is latched into the device and the selected tone pair from the standard DTMF frequencies is generated. An open-drain N-channel transistor provides a MUTE output during tone generation.

Features

- Direct microprocessor interface
- Binary data inputs with latches
- Generates 16 standard tone pairs
- On-chip 3.579545 MHz crystal-controlled oscillator
- Better than 0.64% frequency accuracy
- High group pre-emphasis
- Low harmonic distortion
- MUTE output interfaces to speech network
- Low power idle mode
- 3.5V–8V operation

Block Diagram



TL/H/5004–1

*Crystal Specification: Parallel Resonant 3.579545 MHz, $R_S \leq 150\Omega$, L = 100 mH, C_0 = 5 pF, C_1 = 0.02 pF.

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_{DD} - V_{SS}$)	12V
$\overline{MUTE}$ Voltage	12V
Maximum Voltage at Any Other Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Operating Temperature, T_A	−30°C to +70°C
Storage Temperature	−55°C to +150°C
Maximum Power Dissipation	500 mW

Electrical Characteristics

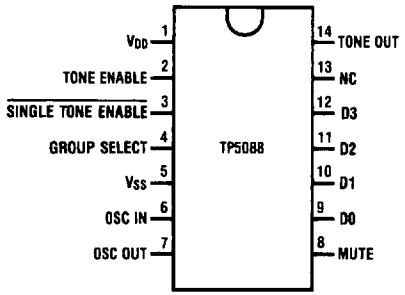
Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{DD} = 3.5V to 8V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Parameter	Conditions	Min	Typ	Max	Units
Minimum Supply Voltage, V_{DD} (min)	Generating Tones	**3.5**			V
Minimum Supply Voltage for Data Input, TONE ENABLE and MUTE Logic Functions		2			V
Operating Current Idle Generating Tones	 R_L = ∞, D0–D3 Open V_{DD} = 3.5V, Mute Open		 55 1.5	 **350** **2.5**	 μA mA
Input Pull-Up Resistance D0–D3 TONE ENABLE			 100 50		 kΩ kΩ
Input Low Level TONE ENABLE, D0–D3				**0.2 V_{DD}**	V
Input High Level TONE ENABLE, D0–D3		**0.8 V_{DD}**			V
MUTE OUT Sink Current (TONE ENABLE LOW)	V_{DD} = 3.5V V_o = 0.5V	**0.4**			mA
MUTE OUT Leakage Current (TONE ENABLE HIGH)	V_{DD} = 3.5V V_o = V_{DD}		1		μA
Output Amplitudes Low Group High Group	R_L = 240 Ω V_{DD} = 3.5V T_A = 25°C	 **130** **180**	 170 230	 **220** **310**	 mVrms mVrms
Mean Output DC Offset	V_{DD} = 3.5V V_{DD} = 8V		 1.2 3.6		 V V
High Group Pre-Emphasis		**2.2**	2.7	**3.2**	dB
Dual Tone/Total Harmonic Distortion Ratio	1 MHz Bandwidth, V_{DD} = 5V R_L = 240Ω	**−20**			dB
Start-Up Time (to 90% Amplitude), t_{OSC}			4		ms
Data Set-Up Time, t_S (*Figure 2*)	V_{DD} = 5V	100			ns
Data Hold Time, t_H	V_{DD} = 5V	280			ns
Data Duration t_W	V_{DD} = 5V	600			ns

Note 1: R_L is the external load resistor connected from TONE OUT to V_{SS}.

Connection Diagram

Dual-In-Line Package



TL/H/5004–2

Top View

Order Number TP5088WM or TP5088N
See NS Package M14B or N14A

Functional Description

With the TONE ENABLE pin pulled low, the device is in a low power idle mode, with the oscillator inhibited and the output transistor turned off. Data on inputs D0–D3 is ignored until a rising transition on TONE ENABLE. Data meeting the timing specifications is latched in, the oscillator and output stage are enabled, and tone generation begins. The decoded data sets the high group and low group programmable counters to the appropriate divide ratios. These counters sequence two ratioed-capacitor D/A converters through a series of 28 equal duration steps per sine wave cycle. On-chip regulators ensure good stability of tone amplitudes with variations in supply voltage and temperature. The two tones are summed by a mixer amplifier, with preemphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}.

Table I shows the accuracies of the tone output frequencies and Table II is the Functional Truth Table.

TABLE I. Output Frequency Accuracy

Tone Group	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low Group f_L	697	694.8	−0.32
	770	770.1	+0.02
	852	852.4	+0.03
	941	940.0	−0.11
High Group f_H	1209	1206.0	−0.24
	1336	1331.7	−0.32
	1477	1486.5	+0.64
	1633	1639.0	+0.37

Pin Descriptions

V_{DD} (Pin 1): This is the positive supply to the device, referenced to V_{SS}. The collector of the TONE OUT transistor is also connected to this pin.

V_{SS} (Pin 5): This is the negative voltage supply. All voltages are referenced to this pin.

OSC IN, OSC OUT (Pins 6 and 7): All tone generation timing is derived from the on-chip oscillator circuit. A low-cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) is needed between pins 6 and 7. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator is stopped when the TONE ENABLE input is pulled to logic low.

TONE ENABLE Input (Pin 2): This input has an internal pull-up resistor. When TONE ENABLE is pulled to logic low, the oscillator is inhibited and the tone generators and output transistor are turned off. A low to high transition on TONE ENABLE latches in data from D0–D3. The oscillator starts, and tone generation continues until TONE ENABLE is pulled low again.

MUTE (Pin 8): This output is an open-drain N-channel device that sinks current to V_{SS} when TONE ENABLE is low and no tones are being generated. The device turns off when TONE ENABLE is high.

D0, D1, D2, D3 (Pins 9, 10, 11, 12): These are the inputs for binary-coded data, which is latched in on the rising edge of TONE ENABLE. Data must meet the timing specifications of *Figure 2*. At all other times these inputs are ignored and may be multiplexed with other system functions.

TONE OUT (Pin 14): This output is the open emitter of an NPN transistor, the collector of which is connected internally to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group tones superimposed on a DC offset. When not generating tones, this output transistor is turned off to minimize the device idle current.

$\overline{\text{SINGLE TONE ENABLE}}$ (Pin 3): This input has an internal pull-up resistor. When pulled to V_{SS}, the device is in single tone mode and only a single tone will be generated at pin 14 (for testing purposes). For normal operation, leave this pin open-circuit or pull to V_{DD}.

GROUP SELECT (Pin 4): This pin is used to select the high group or low group frequency when the device is in single tone mode. It has an internal pull-up resistor. Leaving this pin open-circuit or pulling it to V_{DD} will generate the high group, while pulling to V_{SS} will generate the low group frequency at the TONE OUT pin.

TABLE II. Functional Truth Table

Keyboard Equivalent	Data Inputs				TONE ENABLE	TONES OUT		MUTE
	D3	D2	D1	D0		f_L (Hz)	f_H(Hz)	
X	X	X	X	X	0	0V	0V	0V
1	0	0	0	1	⎍	697	1209	O/C
2	0	0	1	0	⎍	697	1336	O/C
3	0	0	1	1	⎍	697	1477	O/C
4	0	1	0	0	⎍	770	1209	O/C
5	0	1	0	1	⎍	770	1336	O/C
6	0	1	1	0	⎍	770	1477	O/C
7	0	1	1	1	⎍	852	1209	O/C
8	1	0	0	0	⎍	852	1336	O/C
9	1	0	0	1	⎍	852	1477	O/C
0	1	0	1	0	⎍	941	1336	O/C
*	1	0	1	1	⎍	941	1209	O/C
#	1	1	0	0	⎍	941	1477	O/C
A	1	1	0	1	⎍	697	1633	O/C
B	1	1	1	0	⎍	770	1633	O/C
C	1	1	1	1	⎍	852	1633	O/C
D	0	0	0	0	⎍	941	1633	O/C

Timing Diagram

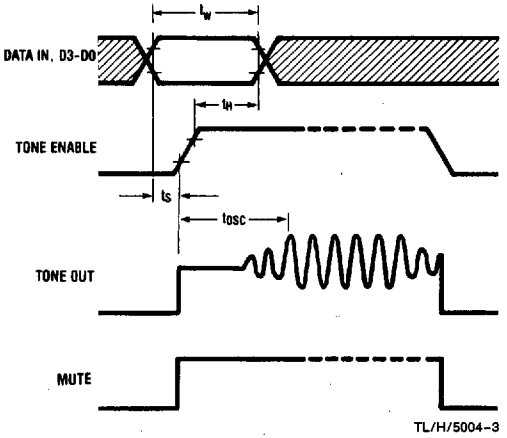
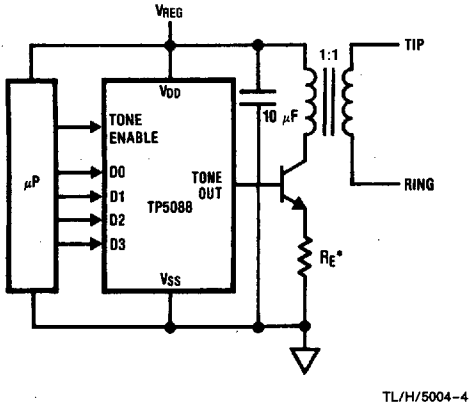


FIGURE 2

Typical Application



*Adjust R_E for desired tone amplitude.

FIGURE 3

Application Information

A block diagram of the basic phase locked loop is shown in *Figure 1*.

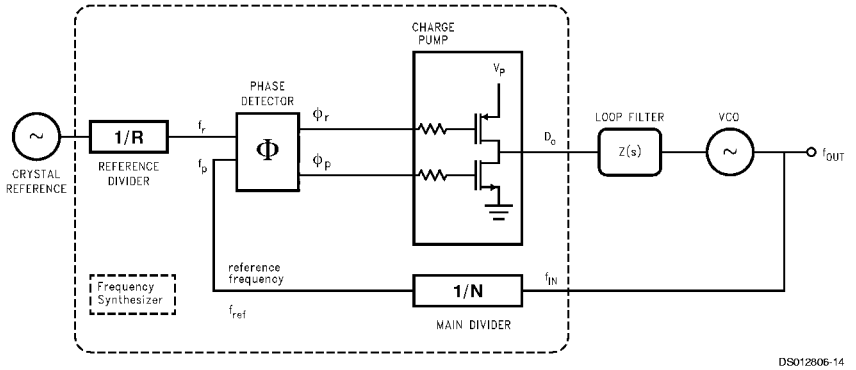


FIGURE 1. Basic Charge Pump Phase Locked Loop

LOOP GAIN EQUATIONS

A linear control system model of the phase feedback for a PLL in the locked state is shown in *Figure 2*. The open loop gain is the product of the phase comparator gain (Kϕ), the VCO gain (K_{VCO}/s), and the loop filter gain Z(s) divided by the gain of the feedback counter modulus (N). The passive loop filter configuration used is displayed in *Figure 3*, while the complex impedance of the filter is given in *Equation (1)*.

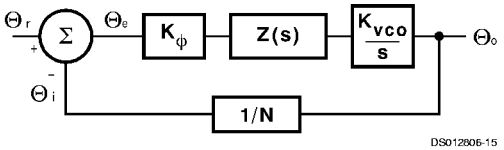


FIGURE 2. PLL Linear Model

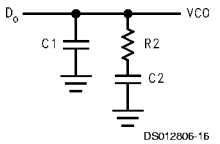


FIGURE 3. Passive Loop Filter

$$\text{Open loop gain} = H(s)\,G(s) = \Theta i/\Theta e = K_\phi Z(s)\,K_{VCO}/Ns$$

$$Z(s) = \frac{s(C1 \bullet R2) + 1}{s^2(C1 \bullet C2 \bullet R2) + sC1 + sC2} \quad (1)$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad (2)$$

and

$$T2 = R2 \bullet C2 \quad (3)$$

The 3rd order PLL Open Loop Gain can be calculated in terms of frequency, ω, the filter time constants T1 and T2, and the design constants K_ϕ, K_{VCO}, and N.

$$G(s) \bullet H(s)\big|_{s = j \bullet \omega} = \frac{-K_\phi \bullet K_{VCO}(1 + j\omega \bullet T2)}{\omega^2 C1 \bullet N(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \quad (4)$$

From *Equations (2), (3)* we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in *Equation (5)*.

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180^\circ \quad (5)$$

A plot of the magnitude and phase of G(s)H(s) for a stable loop, is shown in *Figure 4* with a solid trace. The parameter ϕ_p shows the amount of phase margin that exists at the point the gain drops below zero (the cutoff frequency wp of the loop). In a critically damped system, the amount of phase margin would be approximately 45 degrees.

If we were now to redefine the cut off frequency, wp', as double the frequency which gave us our original loop bandwidth, wp, the loop response time would be approximately halved. Because the filter attenuation at the comparison frequency also diminishes, the spurs would have increased by approximately 6 dB. In the proposed Fastlock scheme, the higher spur levels and wider loop filter conditions would exist only during the initial lock-on phase—just long enough to reap the benefits of locking faster. The objective would be to open up the loop bandwidth but not introduce any additional complications or compromises related to our original design criteria. We would ideally like to momentarily shift the curve of *Figure 4* over to a different cutoff frequency, illustrated by the dotted line, without affecting the relative open loop gain and phase relationships. To maintain the same gain/phase relationship at twice the original cutoff frequency, other terms in the gain and phase *Equation (4)* and *Equation (5)* will have to compensate by the corresponding "1/w" or "1/w^2" factor. Examination of equations *Equations (2), (3)* and *Equation (5)* indicates the damping resistor variable R2 could be chosen to compensate the "w"' terms for the phase margin. This implies that another resistor of equal value to R2 will need to be switched in parallel with R2 during the initial lock period. We must also insure that the magnitude of the open loop gain, H(s)G(s) is equal to zero at wp' = 2wp. K_{vco}, Kϕ, N, or the net product of these terms can be changed by a factor of 4, to counteract the w^2 term present in the denominator of *Equation (2)* and *Equation (3)*. The Kϕ term was chosen to complete the transformation because it can readily be

Application Information (Continued)

switched between 1X and 4X values. This is accomplished by increasing the charge pump output current from 1 mA in the standard mode to 4 mA in Fastlock.

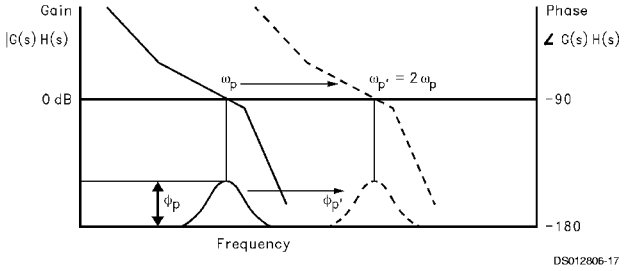


FIGURE 4. Open Loop Response Bode Plot

FASTLOCK CIRCUIT IMPLEMENTATION

A diagram of the Fastlock scheme as implemented in National Semiconductors LMX233XL PLL is shown in *Figure 5*. When a new frequency is loaded, and the RF Icp_o bit is set high the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error while an open drain NMOS on chip device switches in a second R2 resistor element to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second identical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations to account for. Once locked on the correct frequency, the user can return the PLL to standard low noise operation by sending a MICROWIRE instruction with the RF Icp_o bit set low. This transition does not affect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless change between Fastlock and standard mode.

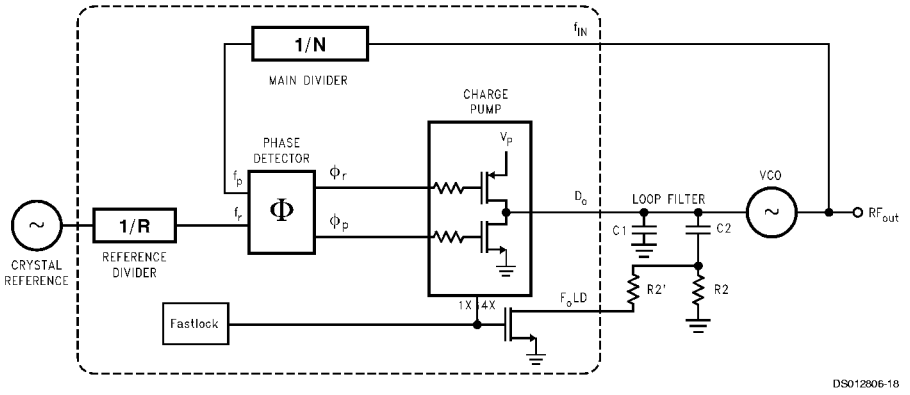
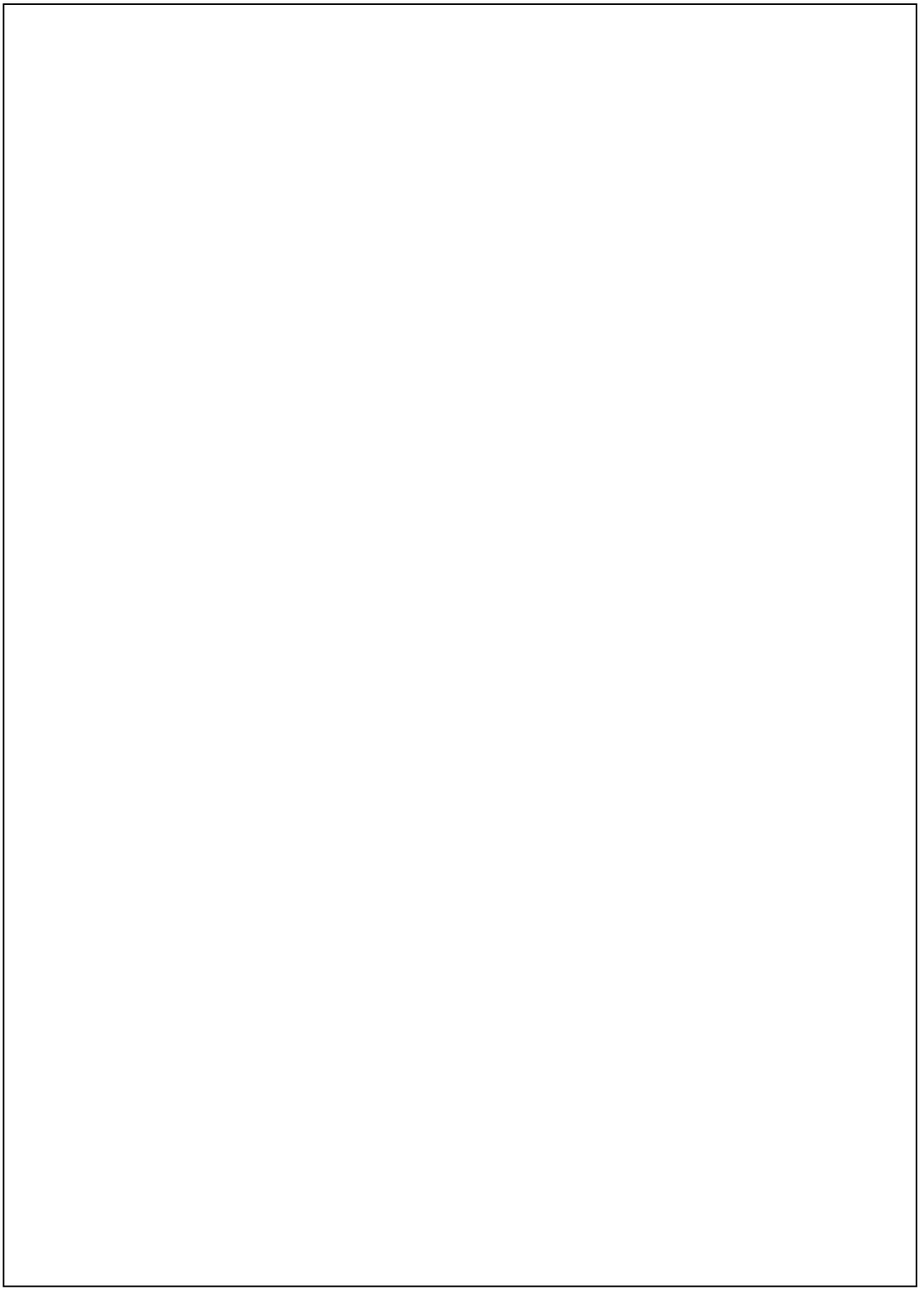
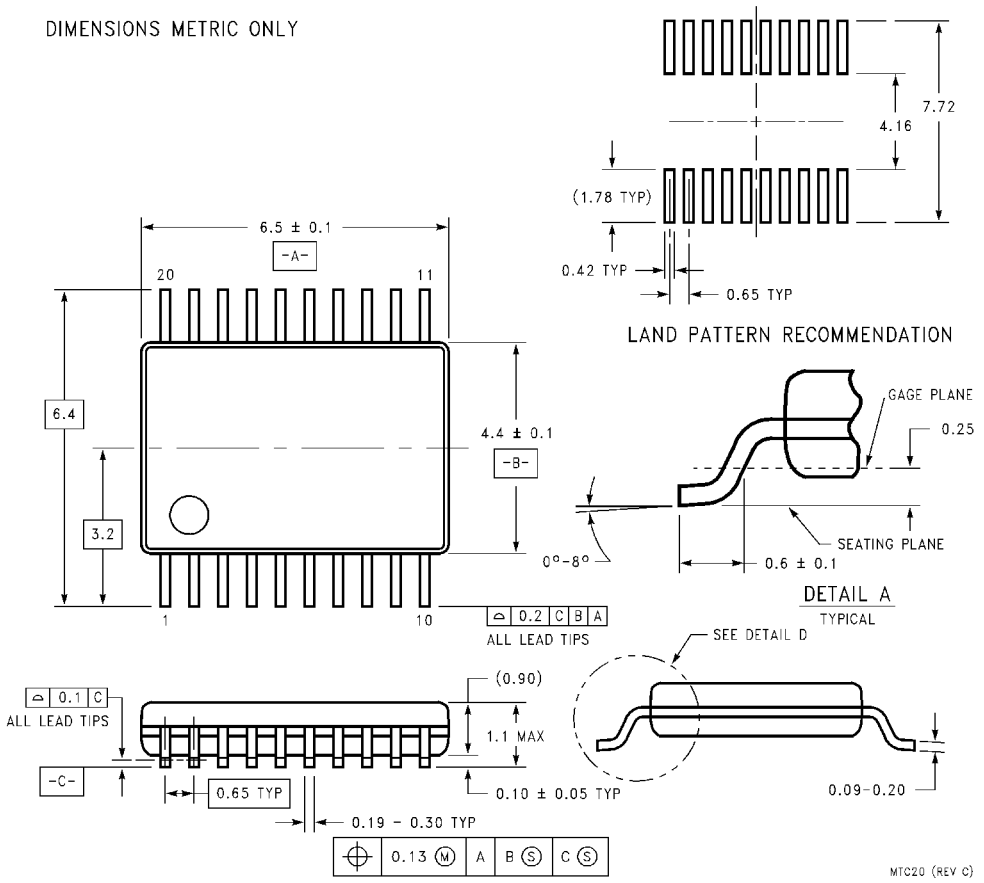


FIGURE 5. Fastlock PLL Architecture



Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead (0.173" Wide) Thin Shrink Small Outline Package (TM)
Order Number LMX2330LTM, LMX2331LTM or LMX2332LTM
*** For Tape and Reel (2500 units per reel)**
Order Number LMX2330LTMX, LMX2331LTMX or LMX2332LTMX
NS Package Number MTC20

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National Semiconductor

ADVANCE INFORMATION
July 1998

LMX2350/LMX2352
PLLatinum™ Fractional N RF / Integer N IF Dual Low Power Frequency Synthesizer

LMX2350 2.5 GHz/550 MHz
LMX2352 1.2 GHz/550 MHz

General Description

The LMX2350/2352 is part of a family of monolithic integrated fractional N/ Integer N frequency synthesizers designed to be used in a local oscillator subsystem for a radio transceiver. It is fabricated using National's 0.5µ ABiC V silicon BiCMOS process. The LMX2350/2352 contains dual modulus prescalers along with modulo 15 or 16 fractional compensation circuitry in the RF divider. A 16/17 or 32/33 prescale ratio can be selected for the LMX2350, and the LMX2352 provides 8/9 or 16/17 prescale ratios. The IF circuitry for both the LMX2350 and LMX2352 contains an 8/9 prescaler, and is fully programmable. Using a fractional N phase locked loop technique, the LMX2350 /52 can generate very stable low noise control signals for UHF and VHF voltage controlled oscillators (VCO's).

For the RF PLL, a highly flexible 16 level programmable charge pump supplies output current magnitudes from 100µA to 1.6mA. Two uncommitted CMOS outputs can be used to provide external control signals, or configured to FastLock™ mode. Serial data is transferred into the LMX2350/2352 via a three wire interface (Data, LE, Clock). Supply voltage can range from 2.7 V to 5.5 V. The LMX2350/2352 family features very low current consumption; typically LMX2350 (2.5 GHz) 7.0 mA, LMX2352 (1.2 GHz) 5.5 mA at 3.0V. The LMX2350/2352 are available in a 24-pin TSSOP surface mount plastic package.

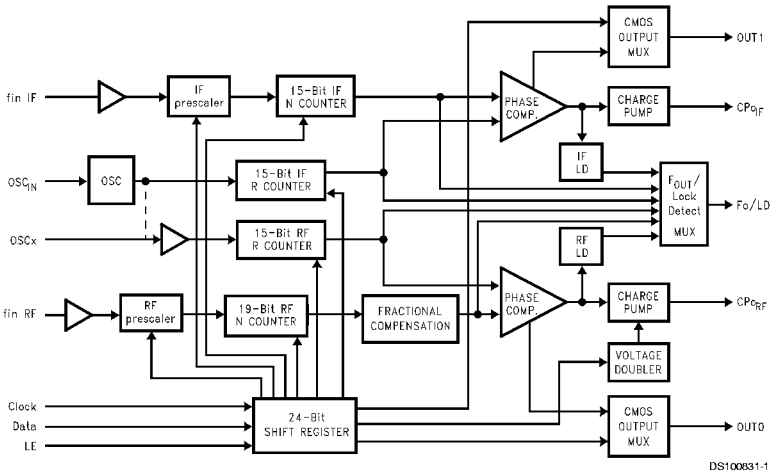
Features

- 2.7 V to 5.5 V operation
- Low current consumption
  LMX2350: Icc = 7mA typ at 3v
  LMX2352: Icc = 5.5mA typ at 3v
- Programmable or logical power down mode
  Icc = 5 µA typ at 3v
- Modulo 15 or 16 fractional RF N divider supports ratios of 1, 2, 3, 4, 5, 8, 15, or 16
- Programmable charge pump current levels
  RF 100µA to 1.6mA in 100µA steps
  IF 100µA or 800 µA
- Digital filtered lock detect

Applications

- Portable wireless communications (PCS/PCN, cordless)
- Dual mode cellular telephone systems
- Zero blind slot TDMA systems
- Spread spectrum communication systems (CDMA)
- Cable TV Tuners (CATV)

Block Diagram



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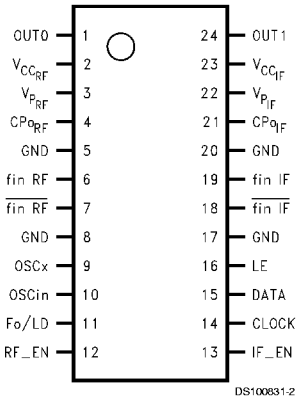
Connection Diagram



Order Number LMX2350TM or LMX2352TM
NS Package Number MTC24

Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	OUT0	O	Programmable CMOS output. Level of the output is controlled by IF_N [17] bit.
2	Vcc_{RF}	-	RF PLL power supply voltage input. Must be equal to Vcc_{IF}. May range from 2.7 V to 5.5 V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
3	V_{PRF}	-	Power supply for RF charge pump. Must be $\geq V_{CC_{RF}}$ and $V_{CC_{IF}}$.
4	CP_{oRF}	O	RF charge pump output. Connected to a loop filter for driving the control input of an external VCO.
5	GND	-	Ground for RF PLL digital circuitry.
6	fin RF	I	RF prescaler input. Small signal input from the VCO.
7	$\overline{\text{fin RF}}$	I	RF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
8	GND	-	Ground for RF PLL analog circuitry.
9	OSCx	I/O	Dual mode oscillator output or RF R counter input. Has a Vcc/2 input threshold when configured as an input and can be driven from an external CMOS or TTL logic gate. Can also be configured as an output to work in conjunction with OSCin to form a crystal oscillator. (See functional description 1.1 and programming description 3.1.)
10	OSCin	I	Oscillator input which can be configured to drive both the IF and RF R counter inputs or only the IF R counter depending on the state of the OSC programming bit. (See functional description 1.1 and programming description 3.1.)
11	FoLD	O	Multiplexed output of N or R divider and RF/IF lock detect. Active High/Low CMOS output except in analog lock detect mode. (See programming description 3.1.5.)
12	RF_EN	I	RF PLL Enable. Powers down RF N and R counters, prescaler, and will TRI-STATE the charge pump output when LOW. Bringing RF_EN high powers up RF PLL depending on the state of RF_CTL_WORD. (See functional description 1.9.)
13	IF_EN	I	IF PLL Enable. Powers down IF N and R counters, prescaler, and will TRI-STATE the charge pump output when LOW. Bringing IF_EN high powers up IF PLL depending on the state of IF_CTL_WORD. (See functional description 1.9.)
14	CLOCK	I	High impedance CMOS Clock input. Data for the various counters is clocked into the 24 - bit shift register on the rising edge.
15	DATA	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.