



**Absolute Maximum Rating\***

D.C. Supply Voltage $V_{DD}$ .....	-0.5V to 7V (With respect to $V_{SS}$ )
Operating Temperature .....	0°C – 70°C
Storage Temperature .....	-65°C – 150°C

**Comments\***

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D. C. Characteristics**

( $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5V \pm 5\%$  unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$V_{IHx}$	Clock Input High-Level Voltage	2.0	—	$V_{DD}$	V	
$V_{ILx}$	Clock Input Low-Level Voltage	-0.5	—	0.8	V	
$V_{IH}$	Input High-Level Voltage	2.0	—	$V_{DD}$	V	
$V_{IL}$	Input Low-Level Voltage	-0.5	—	0.8	V	
$V_{OH}$	Output High-Level Voltage	2.4	—	—	V	$I_{OL} = 1.6\text{ ma}$ on all outputs
$V_{OL}$	Output Low-Level Voltage	—	—	0.4	V	$I_{OH} = -100\text{ ua}$ on all outputs
$I_{IN}$	Input Leakage	—	—	$\pm 10$	ua	$V_{IN} = 5V - 0V$
$I_{CIN}$	Input Leakage	—	—	$\pm 10$	ua	Clock input
$I_{CC}(\text{AVG})$	AVG Power Supply Current	—	—	90	ma	$V_{IN} = V_{DD}$ or 0V, No load
$I_{OZ}$	OFF-State Output Current	—	—	20	ns	$V_o = V_{DD} - 0V$

**Capacitance**

( $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{SS} = 0V$ )

Symbol	Parameter	Min.	Max.	Unit	Condition
$C_{x\text{ IN}}$	Clock Input Capacitance	—	20	pF	$f_c = 1\text{ MHz}$ Unmeasured Pins Returned to $V_{SS}$
$C_{x\text{ OUT}}$	Clock Output Capacitance	—	25	pF	
$C_{IN}$	Input Capacitance	—	10	pF	
$C_{OUT}$	Output Capacitance	—	20	pF	

**A. C. Characteristics**
**Timing Requirements**

Symbol	Parameter	Min.	Max.	Unit	Condition
$t_{AW}$	Address Strobe Width	120	—	ns	
$t_{AS}$	Address Setup Time	110	—	ns	

(Cont.)

Symbol	Parameter	Min.	Max.	Unit	Condition
t <sub>AH</sub>	Address Hold Time	60	—	ns	
t <sub>CS</sub>	Chip Select Setup Time	110	—	ns	
t <sub>CH</sub>	Chip Select Hold Time	60	—	ns	
t <sub>DID</sub>	$\overline{\text{DISTR}}/\text{DISTR}$ Strobe Delay from Latch	20	—	ns	
t <sub>DIW</sub>	$\overline{\text{DISTR}}/\text{DISTR}$ Strobe Width	350	—	ns	
t <sub>RC</sub>	Read Cycle Delay	1,780	—	ns	
RC	Read Cycle = t <sub>AW</sub> + t <sub>DID</sub> + t <sub>DIW</sub> + t <sub>RC</sub>	2,300	—	ns	
t <sub>DOD</sub>	$\overline{\text{DOSTR}}/\text{DOSTR}$ Strobe Delay from Latch	10	—	ns	
t <sub>DOW</sub>	$\overline{\text{DOSTR}}/\text{DOSTR}$ Strobe Width	350	—	ns	
t <sub>WC</sub>	Write Cycle Delay	1,780	—	ns	
WC	Write Cycle = t <sub>AW</sub> + t <sub>DOD</sub> + t <sub>DOW</sub> + t <sub>WC</sub>	2,300	—	ns	
t <sub>DS</sub>	Data Setup Time	350	—	ns	
t <sub>DH</sub>	Data Hold Time	100	—	ns	
t <sub>RA</sub> *	Address Hold Time from $\overline{\text{DISTR}}/\text{DISTR}$	50	—	ns	
t <sub>RCS</sub> *	Chip Select Hold Time from $\overline{\text{DISTR}}/\text{DISTR}$	50	—	ns	
t <sub>AR</sub> *	$\overline{\text{DISTR}}/\text{DISTR}$ Delay from Address	110	—	ns	
t <sub>CSR</sub> *	$\overline{\text{DISTR}}/\text{DISTR}$ Delay from Chip Select	110	—	ns	
t <sub>WA</sub> *	Address Hold Time from $\overline{\text{DOSTR}}/\text{DOSTR}$	50	—	ns	
t <sub>WCS</sub> *	Chip Select Hold Time from $\overline{\text{DOSTR}}/\text{DOSTR}$	50	—	ns	
t <sub>AW</sub> *	$\overline{\text{DOSTR}}/\text{DOSTR}$ Delay from Address	160	—	ns	
t <sub>CSW</sub> *	$\overline{\text{DOSTR}}/\text{DOSTR}$ Delay from Chip Select	160	—	ns	
t <sub>MRM</sub>	Master Reset Pulse Width	25	—	ns	

**Timing Response**

Symbol	Parameter	Min.	Max.	Unit	Condition
t <sub>CSS</sub>	CSOUT Delay from Latch	—	90	ns	All Outputs Loading 40 pF
t <sub>DD</sub>	$\overline{\text{DISTR}}/\text{DISTR}$ to Driver Disable Time	—	250	ns	
t <sub>DDD</sub>	Delay from $\overline{\text{DISTR}}/\text{DISTR}$ to DATA	—	300	ns	
t <sub>HZ</sub>	$\overline{\text{DISTR}}/\text{DISTR}$ to Floating Data Delay	50	300	ns	
t <sub>CSC</sub> *	CSOUT Delay from Select	—	200	ns	

\*Only applies when  $\overline{\text{ADS}}$  is tied Low.

**Other Timing**
**Baud Generator**

Symbol	Parameter	Min.	Max.	Unit	Condition
N	Baud Rate Divisor	1	$2^{16} - 1$		
$t_{BLD}$	Baud Output Negative Edge Delay	—	250	ns	40 pF loading
$t_{BHD}$	Baud Output Positive Edge Delay	—	250	ns	40 pF loading
$t_{LW}$	Baud Output Down Time	425	—	ns	40 pF loading
$t_{HW}$	Baud Output Up Time	330	—	ns	40 pF loading

**Receiver**

Symbol	Parameter	Min.	Max.	Unit	Condition
$t_{SCD}$	Delay from RCLK to Sample Time	—	2	us	
$t_{SINT}$	Delay from Stop Bit to Set Interrupt	—	3	RCLK Cycle	40 pF loading
$t_{RINT}$	Delay from $\overline{DISTR}/DISTR$ (RD RBR/RDLSR) to Reset Interrupt	—	890	ns	40 pF loading

**Transmitter**

Symbol	Parameter	Min.	Max.	Unit	Condition
$t_{HR}$	Delay from $\overline{DOSTR}/DOSTR$ (WR INT) to Reset Interrupt	—	890	ns	40 pF loading
$t_{IRS}$	Delay from Initial INTR Reset to Transmit Start	—	16	BAUDOUT Cycle	
$t_{SI}$	Delay from Initial Write to Interrupt	—	24	BAUDOUT Cycle	
$t_{SS}$	Delay from Stop to Next Start	—	1	us	40 pF loading
$t_{STI}$	Delay from Stop to Interrupt (THRE)	—	8	BAUDOUT Cycle	
$t_{IR}$	Delay from $\overline{DISTR}/DISTR$ (RD IIR) to Reset Interrupt (THRE)	—	890	ns	40 pF loading

**Modem Control**

Symbol	Parameter	Min.	Max.	Unit	Condition
$t_{WDO}$	Delay from DOSTR/DOSTR (WR MCR) to Output	—	730	ns	40pF loading
$t_{SIM}$	Delay to Set Interrupt from MODEM Input	—	1,000	ns	40 pF loading
$t_{RIM}$	Delay to Reset Interrupt from DISTR/DISTR (RD MSR)	—	730	ns	40 pF loading

**Pin Description**
**Input Signal**

**Chip Select (CS0, CS1,  $\overline{CS2}$ ), Pins 12–14:** When CS0 and CS1 are high and  $\overline{CS2}$  is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ( $\overline{ADS}$ ) input.

**Data Input Strobe (DISTR,  $\overline{DISTR}$ ), Pins 21 and 22:** When DISTR is high or when  $\overline{DISTR}$  is low, the chip is selected; it allows the CPU to read status information or data from a selected register of the UM8250B.

**Data Output Strobe (DOSTR,  $\overline{DOSTR}$ ), Pins 18 and 19:** The chip is selected when DOSTR is high or  $\overline{DOSTR}$  is low and allows the CPU to write data or control words into a selected register of the UM8250B.

\*Note that only one of these two inputs, DISTR and  $\overline{DISTR}$  (DOSTR and  $\overline{DOSTR}$ ) is needed to activate the CPU read (Write). Tie either DISTR (DOSTR) low or  $\overline{DISTR}$  ( $\overline{DOSTR}$ ) high if not needed.

**Address Strobe ( $\overline{ADS}$ ), Pin 25:** When low, provides latching for the Register Select (A0, A1, A2) and Chip Select (CS0, CS1,  $\overline{CS2}$ ) signals. An active  $\overline{ADS}$  input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the  $\overline{ADS}$  input permanently low.

**Register Select (A0, A1, A2), Pins 26–28:** These three inputs are used during a read or write operation to select a UM8250B register to read from or write into as indicated in Table 1. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain UM8250B registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

**Receiver Clock (RCLK), Pin 9:** This input is the 16X baud rate clock for the receiver section of the chip.

**Serial Input (SIN), Pin 10:** Serial data input from the communications link (peripheral device, MODEM, or data set).

**Clear to Send ( $\overline{CTS}$ ), Pin 36:** The  $\overline{CTS}$  signal is a MODEM control function input whose conditions can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the  $\overline{CTS}$  input has changed state since the previous reading of the MODEM Status Register. CTS has no effect on the Transmitter. Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

**Data Set Ready ( $\overline{DSR}$ ), Pin 37:** When low, this indicates that the MODEM or data set is ready to establish the communications link and transfer data with the ACE. The DSR signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the  $\overline{DSR}$  input has changed state since the previous reading of the MODEM Status Register. Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

**Received Line Signal Detect Pin 38:** When low, indicates that the data carrier has been detected by MODEM or data set.

The  $\overline{RLSD}$  Signal is a MODEM Control function input and can be tested by reading bit 7 (RLSD) of the MSR. Bit 3 (DRLSD) of MSR indicates whether the  $\overline{RLSD}$  input has changed state since the previous reading of MSR. Whenever the RLSD bit of MSR changes state, an interrupt is generated if the MODEM Status Interrupt is enable.

**Table 1**

DLAB	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write).
0	0	0	1	Interrupt Enable.
X	0	1	0	Interrupt Identification (read only).
X	0	1	1	Line Control.
X	1	0	0	MODEM Control.
X	1	0	1	Line Status.
X	1	1	0	MODEM Status.
X	1	1	1	None.
1	0	0	0	Divisor Latch (least significant byte).
1	0	0	1	Divisor Latch (most significant byte).

**Ring Indicator ( $\overline{RI}$ ), Pin 39:** When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The  $\overline{RI}$  signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the RI input has changed from a low to a high state since the previous reading of the MODEM Status Register. Whenever the  $\overline{RI}$  bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM

Status Register is enabled.

**Master Reset (MR), Pin 35:** This input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis. When high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches) and the control logic of the UM8250B. Also, the state of various output signals (SOUT, INTRPT,  $\overline{OUT 1}$ ,  $\overline{OUT 2}$ ,  $\overline{RTS}$ , DTR) are affected by an active MR input. (Refer to Table 2).

**Table 2 Reset Function**

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All bits Low (0–3 forced and 4–7 permanent).
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low, Bits 3–7 are Permanently Low.
Line Control Register	Master Reset	All Bits Low.
MODEM Control Register	Master Reset	All Bits Low.
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 which are High.
MODEM Status Register	Master Reset	Bits 0–3 Low, Bits 4–7 – Input Signal.
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
DTR	Master Reset	High
$\overline{OUT 1}$	Master Reset	High

## Output Signals

**Request to Send ( $\overline{\text{RTS}}$ ), Pin 32:** When low, informs the MODEM or data set that the UM8250B is ready to transmit data. The  $\overline{\text{RTS}}$  output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The  $\overline{\text{RTS}}$  signal is set high in a Master Reset operation.

**Data Terminal Ready ( $\overline{\text{DTR}}$ ), Pin 33:** When low, informs the MODEM or data set that the UM8250B is ready to communicate. The  $\overline{\text{DTR}}$  output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The  $\overline{\text{DTR}}$  signal is set high in a Master Reset operation.

**Output 1 ( $\overline{\text{OUT 1}}$ ), Pin 34:** User-designated output can be set to an active low by programming bit 2 ( $\overline{\text{OUT 1}}$ ) of the MODEM Control Register to a high level. The  $\overline{\text{OUT 1}}$  signal is set high in a Master Reset Operation.

**Output 2 ( $\overline{\text{OUT 2}}$ ), Pin 31:** User-designated output can be set to an active low by programming bit 3 ( $\overline{\text{OUT 2}}$ ) of the MODEM Control Register to a high level. The  $\overline{\text{OUT 2}}$  signal is set high in a Master Reset Operation.

\*Note that the  $\overline{\text{RTS}}$ ,  $\overline{\text{DTR}}$ ,  $\overline{\text{OUT 1}}$  and  $\overline{\text{OUT 2}}$  are forced to inactive state (high) during loop mode operation.

**Chip Select Out (CSOUT), Pin 24:** When high, indicates that the chip has been selected by active, CS0, CS1, and  $\overline{\text{CS2}}$  inputs. No data transfer can be initiated until the CSOUT signal is a logic 1. When chip is not selected, CSOUT remains low.

**Driver Disable (DDIS), Pin 23:** This pin remains low whenever the CPU is reading data from UM8250B. A high-level output can be used to disable an external transceiver if the CPU is not reading.

**Baud Out ( $\overline{\text{BAUDOUT}}$ ), Pin 15:** 16X clock signal for the transmitter section of the UM8250B. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches.

The  $\overline{\text{BAUDOUT}}$  may also be used for the receiver section by tying this output to the RCLK input of the chip.

**Interrupt (INTRPT), Pin 30:** Goes high whenever any

of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset to low at the appropriate interrupt service or in a Master Reset operation.

**Serial Output (SOUT), Pin 11:** Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state in a Master Reset operation.

## Input/Output Signals

**Data ( $\text{D}_7\text{--}\text{D}_0$ ) Bus, Pins 1–8:** This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the UM8250 and the CPU. Data, control words, and status information are transferred via the  $\text{D}_7\text{--}\text{D}_0$  Data Bus.

**External Clock Input/Output (XTAL 1, XTAL 2), Pins 16 and 17:** These two pins connect the main timing reference (crystal or clock signal) to the UM8250B.

## Accessible Registers

There are 10 registers, as shown in Table 3, which may be accessed or controlled by the programmer via the CPU. These registers are used to control operations and to transmit and receive data.

### Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in Table 3 and are described below:

**Bits 0 and 1:** These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

**Table 3 Summary of UM8250B Programmable Registers**

Bit No.	Register Address									
	0DLAB=0	0DLAB=0	1DLAB=0	2	3	4	5	6	0DLAB=1	1DLAB=1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER		LCR	MCR	LSR	MSR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBF1)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

\*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.



Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

**Bit 2:** This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 and a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 and a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

**Bit 3:** This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are added.)

**Bit 4:** This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s are transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s are transmitted or checked.

**Bit 5:** This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.

**Bit 6:** This bit is the Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there regardless of other transmitter activities. The set break is disabled by setting bit 6 to a logic 0. This feature enables the CPU to alert a terminal in a computer communications system.

**Bit 7:** This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

### Programmable Baud Rate Generator

The UM8250B contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to  $(2^{16}-1)$ . The output frequency of the Baud Generator is  $16X$  the Baud rate [divisor  $\# = (\text{frequency input}) \div (\text{baud rate} \times 16)$ ]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Table 4 and 5 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the baud rate be greater than 56K Baud.

**Table 4 Baud Rates Using 1.8432 MHz Crystal**

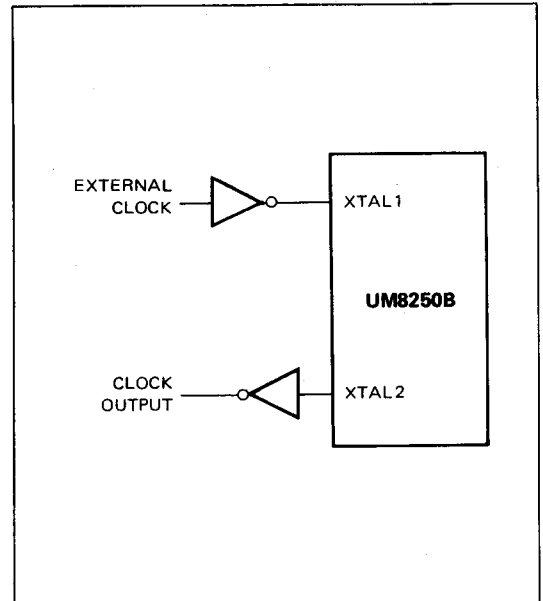
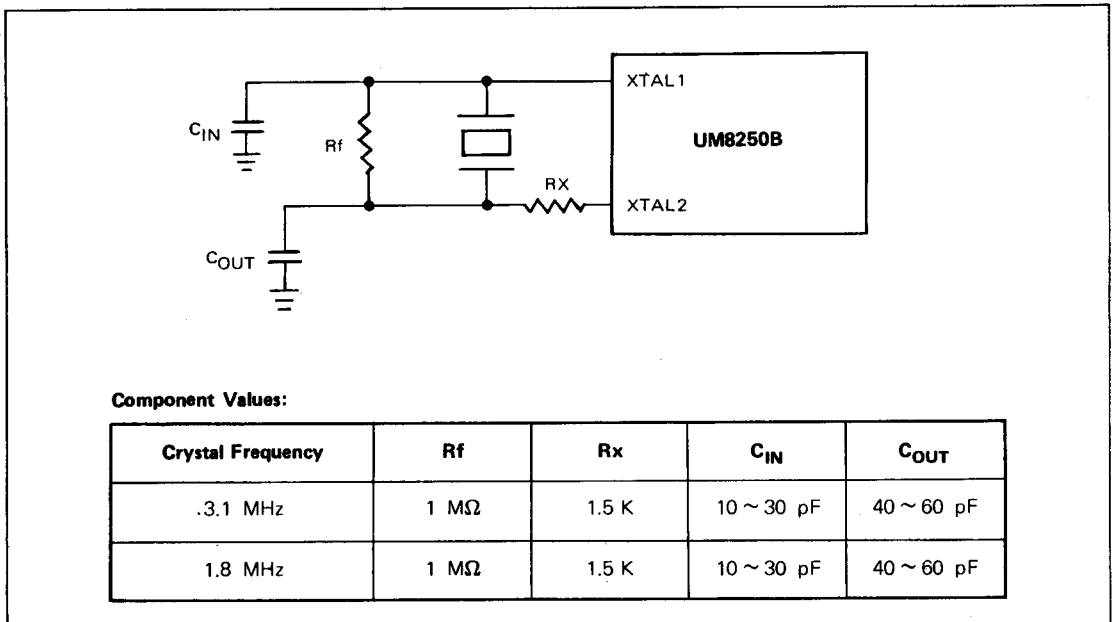
Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
133.5	857	0.0258
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

**Note:** 1.8432 MHz is the standard 8080 frequency divided by 10.

**Table 5 Baud Rates Using 3.072 MHz Crystal**

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	0.312
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—

Fig 1 and 2 show the typical application circuits of the UM8250B's clock generation.


**Figure 1 Clock Circuit with External Clock Signal.**

**Figure 2 Clock Circuit with Crystal Oscillator.**

### Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 3 and are described below.

**Bit 0:** This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

**Bit 1:** This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

**Bit 2:** This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

**Bit 3:** This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

**Bit 4:** This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

\*Note: BI and FE are reset whenever the CPU reads the contents of the Line State indicator.

\*Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

**Bit 5:** This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UM8250B is

ready to accept a new character for transmission. In addition, this bit causes the UM8250B to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is concurrently reset to logic 0 with the loading of the Transmitter Holding Register by the CPU.

**Bit 6:** This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon transfer of data from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

**Bit 7:** This bit is permanently set to logic 0.

### Interrupt Identification Register

The UM8250B has an on-chip interrupt capability that allows flexibility in interfacing popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the UM8250B prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and Modem Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt is stored in the Interrupt Identification Register (refer to Table 6). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 3 and are described below.

**Bit 0:** This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

**Bits 1 and 2:** These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 5.

**Table 6 Interrupt Control Functions**

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

**Bits 3 through 7:** These five bits of the IIR are always set at logic 0.

#### Interrupt Enable Register

This 8-bit register enables the four types of interrupts of the UM8250B to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table 3 and are described below.

**Bit 0:** This bit enables the Received Data Available Interrupt when set to logic 1.

**Bit 1:** This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

**Bit 2:** This bit enables the Receiver Line Status Interrupt when set to logic 1.

**Bit 3:** This bit enables the MODEM Status Interrupt when set to logic 1.

**Bits 4 through 7:** These four bits are always set at logic 0.

#### MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 3 and are described below.

**Bit 0:** This bit controls the Data Terminal Ready ( $\overline{DTR}$ ) output. When bit 0 is set to logic 1, the  $\overline{DTR}$  output

is forced to a logic 0. When bit 0 is reset to a logic 0, the  $\overline{DTR}$  output is forced to a logic 1. The  $\overline{DTR}$  output of the UM8250B may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

**Bit 1:** This bit controls the Request to Send ( $\overline{RTS}$ ) output. Bit 1 affects the  $\overline{RTS}$  output in a manner identical to that described above for bit 0.

**Bit 2:** This bit controls the Output 1 ( $\overline{OUT1}$ ) signal, which is an auxiliary user-designated output. Bit 2 affects the  $\overline{OUT1}$  output in a manner identical to that described above for bit 0.

**Bit 3:** This bit controls the Output 2 ( $\overline{OUT2}$ ) signal, which is an auxiliary user-designated output. Bit 3 affects the  $\overline{OUT2}$  output in a manner identical to that described above for bit 0.

**Bit 4:** This bit provides a local loopback feature for diagnostic testing of the UM8250B. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ( $\overline{CTS}$ ,  $\overline{DSR}$ ,  $\overline{DCD}$ , and  $\overline{RI}$ ) are disconnected; and the four MODEM Control outputs ( $\overline{DTR}$ ,  $\overline{RTS}$ ,  $\overline{OUT1}$ , and  $\overline{OUT2}$ ) are internally connected to the four MODEM Control inputs, and the MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UM8250B.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The UM8250B interrupt system can be tested by writing into the lower six bits of the Line Status Register and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal UM8250B operation. To return to normal operation, the registers must be reprogrammed for normal operation and then bit 4 of the MODEM control Register must be reset to logic 0.

**Bits 5 through 7:** These bits are permanently set to logic 0.

### MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 3 and are described below.

**Bit 0:** This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the  $\overline{CTS}$  input to the chip has changed state since the last time it was read by the CPU.

**Bit 1:** This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the  $\overline{DSR}$  input to the Chip has changed states since the last time it was read by the CPU.

**Bit 2:** This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the  $\overline{RI}$  input to the chip has changed from a low state to a high state.

**Bit 3:** This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates the  $\overline{RLSD}$  input to the chip has changed states.

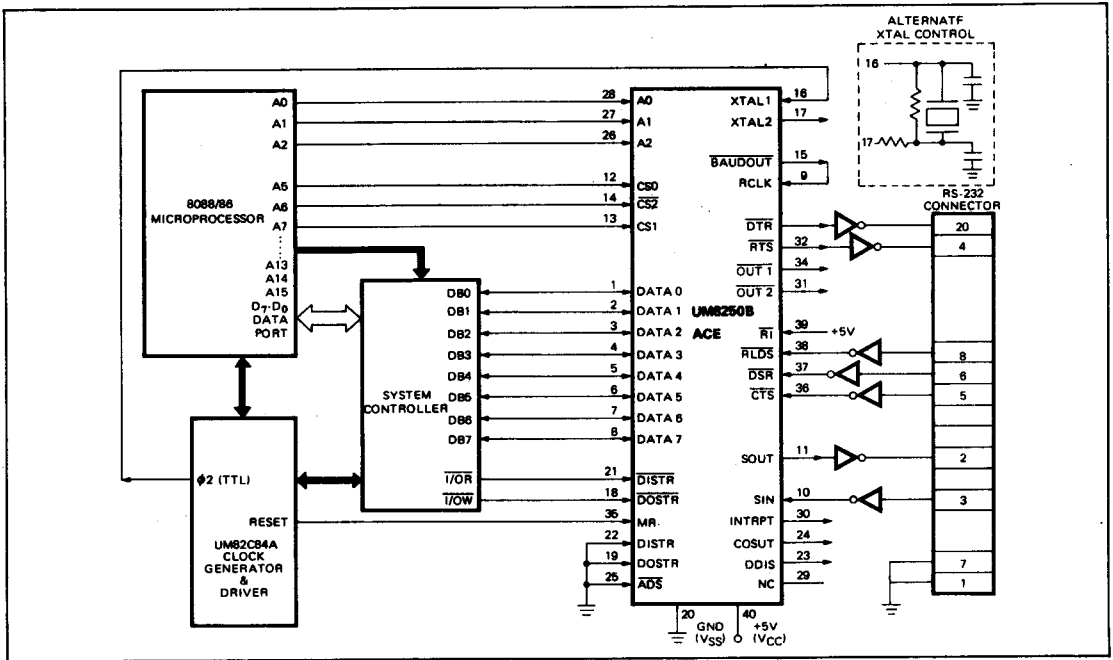
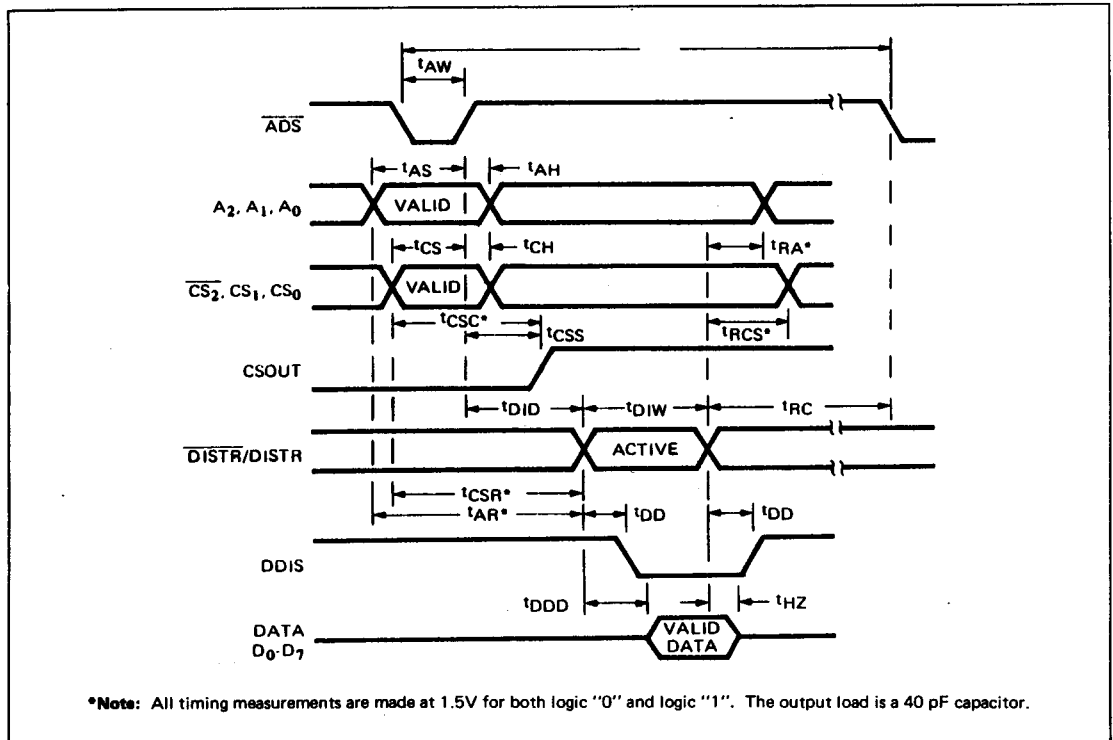
\*Note that whenever bit 0, 1, 2 or 3 is set at logic 1, a MODEM Status interrupt is generated.

**Bit 4:** This bit is the complement of the Clear to Send ( $\overline{CTS}$ ) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to  $\overline{RTS}$  in the MCR.

**Bit 5:** This bit is the complement of the Data Set Ready ( $\overline{DSR}$ ) input. If bit 4 of the MCR is set to a 1, this bit is equivalent of  $\overline{DTR}$  in the MCR.

**Bit 6:** This bit is the complement of the Ring Indicator ( $\overline{RI}$ ) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to  $\overline{OUT1}$  in the MCR.

**Bit 7:** This bit is the complement of the Received Line Signal Detect ( $\overline{RLSD}$ ) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to  $\overline{OUT2}$  of the MCR.


**Figure 3**


\*Note: All timing measurements are made at 1.5V for both logic "0" and logic "1". The output load is a 40 pF capacitor.

**Fig 4 Read Cycle Timing.**

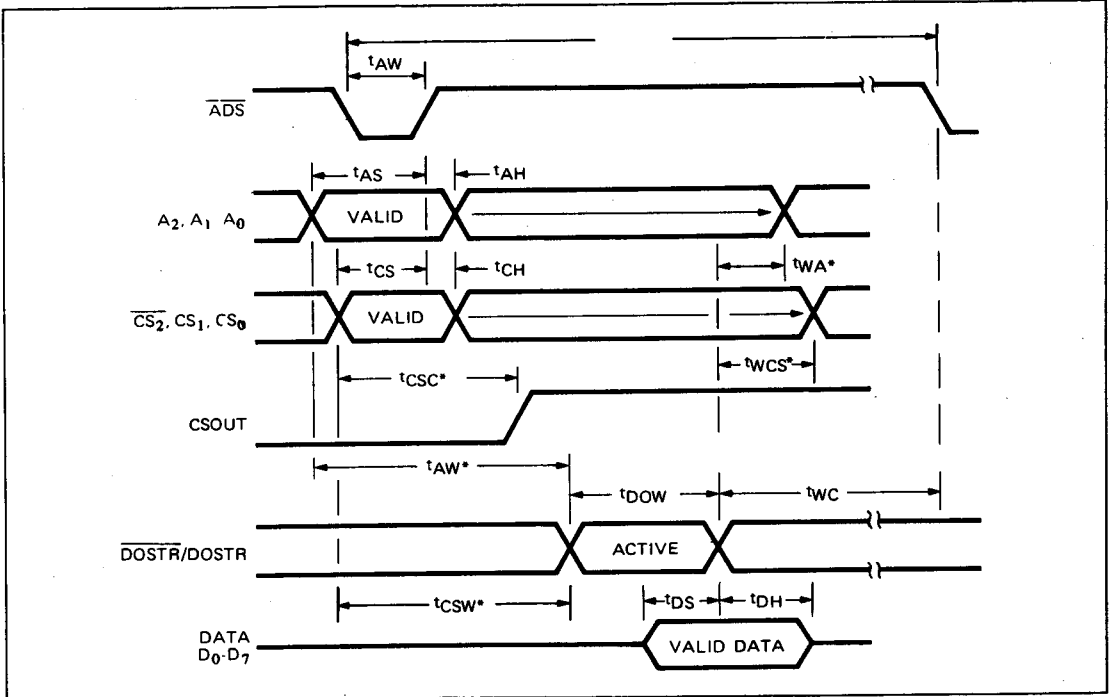


Figure 5 Write Cycle Timing.

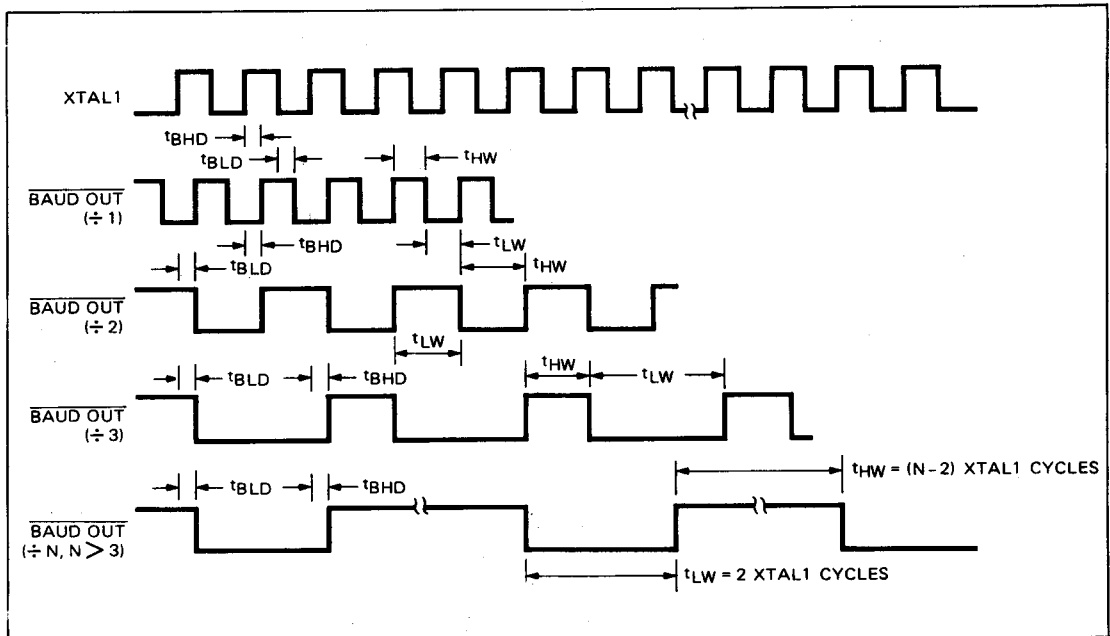


Figure 6 BAUDOUT Timing.

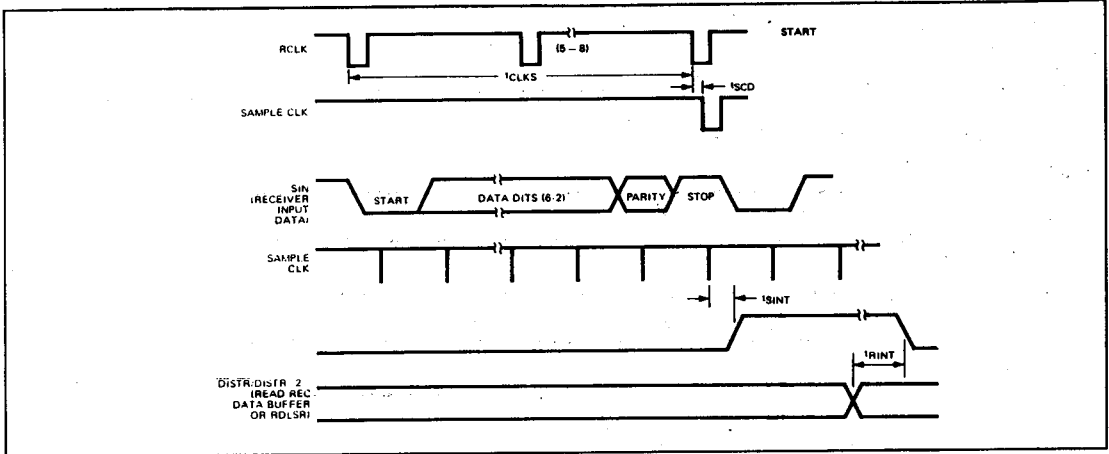


Figure 7 Receiver Timing.

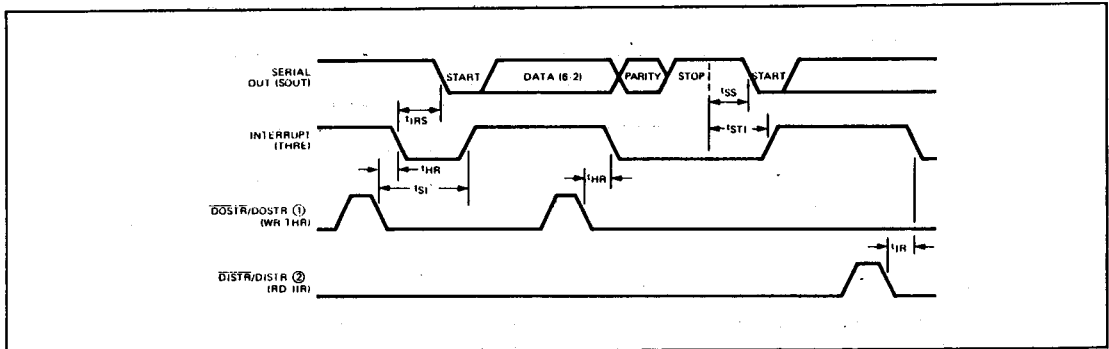


Figure 8 Transmitter Timing.

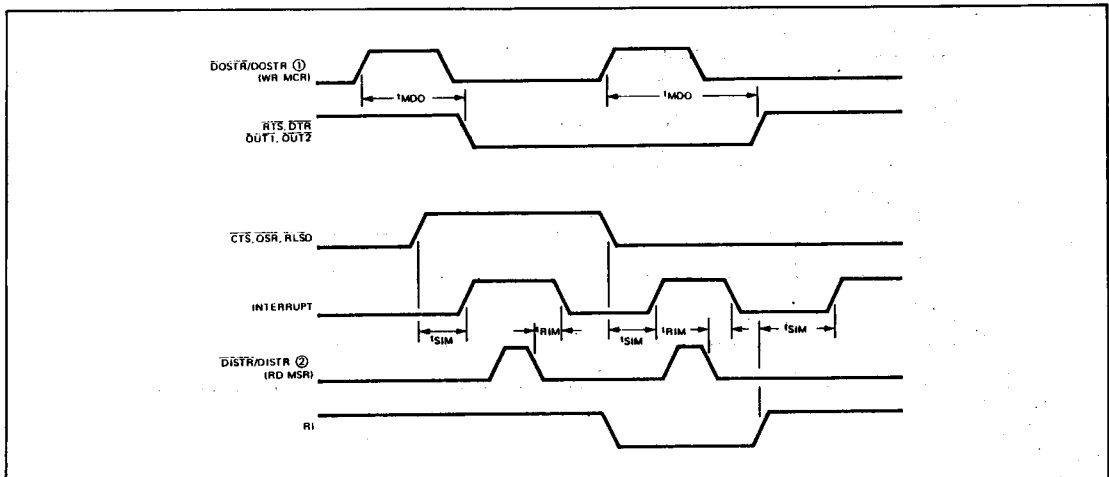
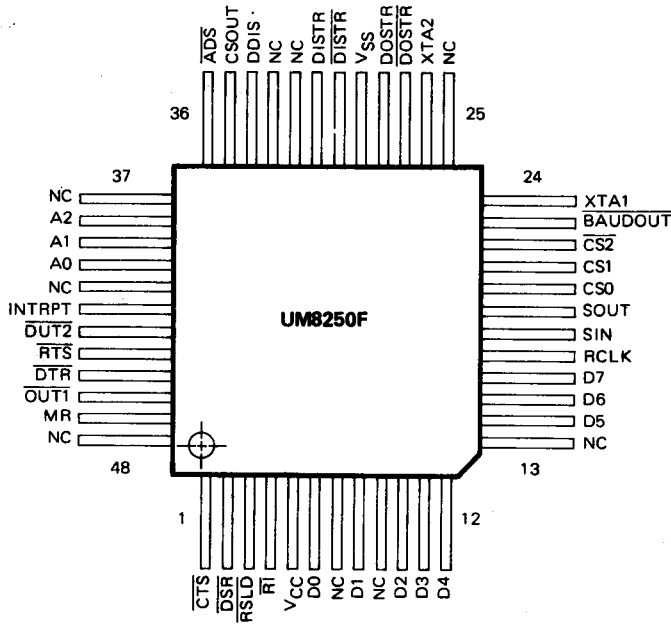


Figure 9 MODEM Timing.



**Pin Configuration**

**Pad Description**

Pad No.	Designation	Pad No.	Designation
1	CTS	25	NC
2	DSR	26	XTA2
3	RSLD	27	DOSTR
4	RI	28	DOSTR
5	V <sub>CC</sub>	29	V <sub>SS</sub>
6	D0	30	DISTR
7	NC	31	DISTR
8	D1	32	NC
9	NC	33	NC
10	D2	34	DDIS
11	D3	35	CSOUT
12	D4	36	ADS
13	NC	37	NC
14	D5	38	A2
15	D6	39	A1
16	D7	40	A0
17	RCLK	41	NC
18	SIN	42	INTRPT
19	SOUT	43	OUT2
20	CS0	44	RTS
21	CS1	45	DTR
22	CS2	46	OUT1
23	BAUDOUT	47	MR
24	XTA1	48	NC