

MAGNETIC TAPE CASSETTE/CARTRIDGE CONTROLLER

DESCRIPTION The NEC μPD371 is a high performance N-Channel LSI tape cassette/cartridge controller designed to interface between most cassette or cartridge tape drives and most microprocessors or minicomputers.

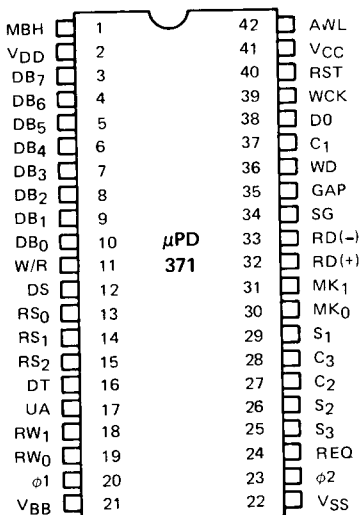
The μPD371 converts 8-bit parallel data into serial phase encoded data to be written on tape and converts phase encoded data read from tape into 8-bit parallel data, calculates the CRC during write operations, verifies the CRC during read operations, informs the processor program when to send data bytes during write operations and when to read bytes during read operations, converts tape drive status signals into register bit levels which may be read by the processor program and converts software commands into signals which may be understood by the tape drive(s).

The μPD371 read and write data paths are completely separate to allow read-after-write data verification.

The μPD371 places no limitation on the selection of tape speed since the μPD371 maximum data transfer rate is considerably faster than that of the fastest cassette or cartridge drive.

- FEATURES**
- Compatible with ANSI, ECMA and ISO standard
 - Also compatible with most other standards
 - Hardware CRC generation and verification
 - Read-after-write capability
 - High speed file search
 - Multiple drive capability
 - May read or write on one drive while rewinding or file searching on another
 - Maximum Data Transfer rate of 375K bits/sec equivalent to 468 IPS at 800 BPI

PIN CONFIGURATION



μ PD371

Operating Temperature	0°C to +70°C
Storage Temperature	-40°C to +125°C
All Output Voltages	-1 to +8 Volts ①
All Input Voltages	-1 to +8 Volts ①
Clock Voltages	-1 to +16 Volts ①
Supply Voltage V _{DD}	-1 to +16 Volts ①
Supply Voltage V _{CC}	-1 to +8 Volts ①
Supply Voltage V _{BB}	-10 to 0 Volts

ABSOLUTE MAXIMUM RATINGS*

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

Note: ① V_{BB} = -5V ± 5%. All voltages measured with respect to GND.

$$T_a = 0 - 70^\circ\text{C} \quad V_{DD} = +12\text{V} \pm 5\% \quad V_{CC} = +5\text{V} \pm 5\% \quad V_{BB} = -5\text{V} \pm 5\% \quad V_{SS} = 0\text{V}$$

DC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V _{IH}	+3.0		V _{CC}	V	
Input Low Voltage	V _{IL}	0		+0.8	V	
Output High Voltage	V _{OH}	+3.5			V	I _{OH} = -1 mA
Output Low Voltage	V _{OL}			+0.4	V	I _{OL} = +1.7 mA
Clock Input High Voltage	V _{OH}	+9		V _{DD}	V	
Clock Input Low Voltage	V _{OL}	0		+0.65	V	
Input Leakage Current	I _{LIH}			+10	μA	V _I = +3.0V
Input Leakage Current	DB ₀ - DB ₇	I _{LIL 1}		-10	μA	V _I = +0.8V
	All Except DB ₀ - DB ₇ (~25K Internal Pull-ups)	I _{LIL 2}		-1.0	mA	V _I = +0.4V
Clock Input Leakage Current	I _{LOH}			+20	μA	V _O = +9.0V
Clock Input Leakage Current	I _{LOL}			-20	μA	V _O = +0.65V
Output Leakage Current	I _{LOH}			+10	μA	V _O = +3.5V
Output Leakage Current	I _{LOL}			-10	μA	V _O = +0.4V
Power Supply Current (V _{DD})	I _{DD}		+20		mA	
Power Supply Current (V _{CC})	I _{CC}		+30		mA	
Power Supply Current (V _{BB})	I _{BB}		-2		mA	

$$T_a = 25^\circ\text{C}, \quad V_{DD} = V_{CC} = V_{SS} = 0\text{V}, \quad V_{BB} = -5\text{V}$$

CAPACITANCE

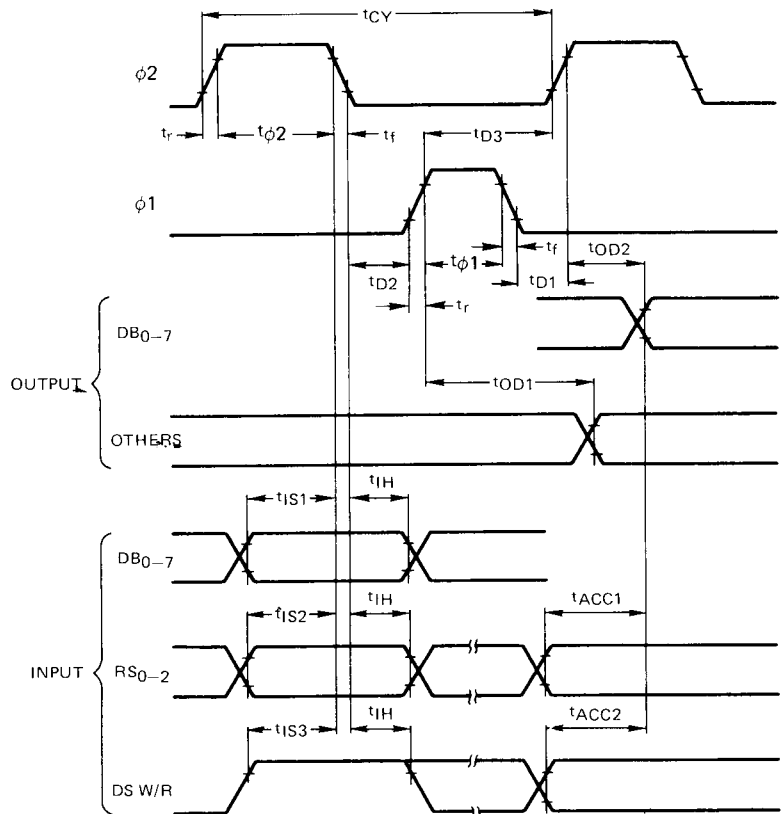
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clock Capacitance	C _O			35	pF	f _c = 1 MHz. All pins except measuring pin are grounded.
Input Capacitance	C _{IN}			10	pF	
Output Capacitance	C _{OUT}			20	pF	

AC CHARACTERISTICS

T_a = 0 – 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = CU

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clock Period	t _{cy}	480		5000	ns	
Clock Rise and Fall Times	t _r , t _f	0		50	ns	
φ1 Pulse Width	t _{φ1}	60			ns	
φ2 Pulse Width	t _{φ2}	220			ns	
φ1 to φ2 Delay	t _{D1}	0			ns	
φ2 to φ1 Delay	t _{D2}	70			ns	
Delay φ1 to φ2 Lead Edges	t _{D3}	80			ns	
Data Out Delay from φ1	t _{OD1}			480	ns	1TTL & CL = 30 pF
Data Out Delay from φ1	t _{OD2}			260	ns	1TTL & CL = 30 pF
RS ₀ – RS ₂ to Output Delay	t _{ACC1}			300	ns	1TTL & CL = 30 pF
DS, W/R to Output Delay	t _{ACC2}			200	ns	1TTL & CL = 30 pF
DB ₀ – DB ₇ to φ2 Setup Time	t _{IS1}	250			ns	
RS ₀ – RS ₂ to φ2 Setup Time	t _{IS2}	350			ns	
DS, W/R to φ2 Setup Time	t _{IS3}	150			ns	
Input Hold Time from φ2	t _{IH}	30			ns	

TIMING WAVEFORMS



Note: Timing Measurement Levels:
 Clock High/Low Voltage = 9.0V/0.65V
 Input High/Low Voltage = 3.0V/0.8V
 Output High/Low Voltage = 2.0V/0.8V



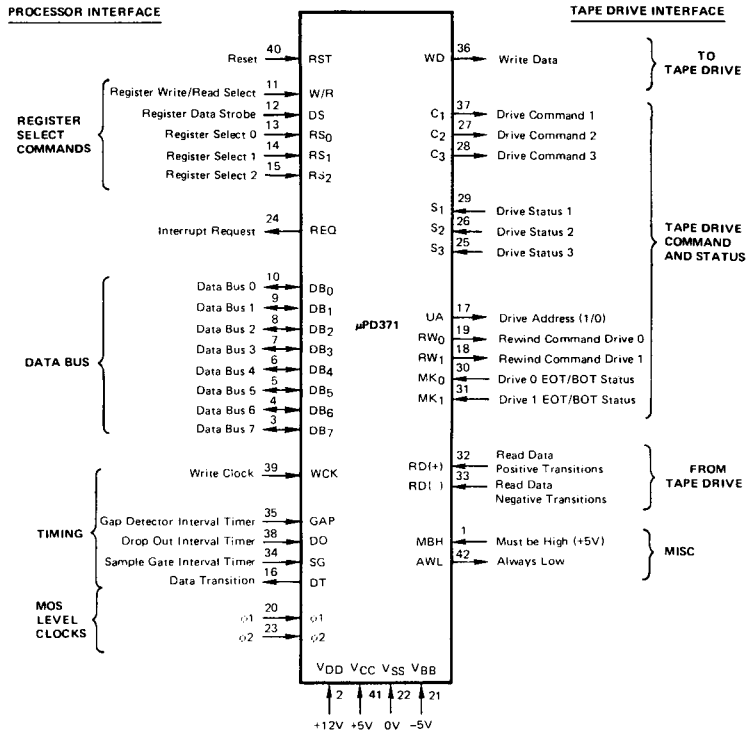
μ PD371

PIN IDENTIFICATION^①

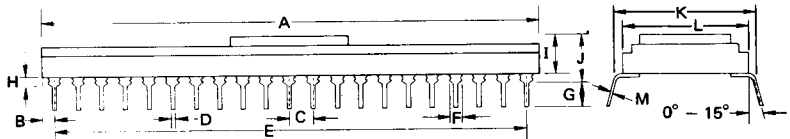
PIN			FUNCTION
NO.	SYMBOL	NAME	
RESET			
40	RST	Reset	A logic one at this pin causes a general reset of the μPD371.
REGISTER SELECT COMMANDS AND DATA BUS			
11	W/R		<p>W/R, DS and RS₀ – RS₂ control Data Bus transfers between the μPD371 and the processor as follows:</p> <p>Writing into a μPD371 register: When W/R is a logic one, information the processor places on DB₀ – DB₇ is written into the μPD371 WRITE REGISTER selected by RS₀ – RS₂. The information is strobed into the register by a logic one at DS.</p> <p>Reading from a μPD371 register: When W/R is a logic zero, information from the μPD371 READ REGISTER selected by RS₀ – RS₂ is placed on DB₀ – DB₇ to be read by the processor. The information remains on DB₀ – DB₇ as long as DS is a logic one.</p>
12	DS		
13 – 15	RS ₀ – RS ₂		
3 – 10	DB ₀ – DB ₇	Data Bus	
INTERRUPT REQUEST			
24	REQ		The μPD371 may be operated with either interrupt or polling techniques. If the interrupt technique is chosen, REQ should be connected to the interrupt request input of the processor. There are three sources of interrupt: READ BUFFER FULL, WRITE BUFFER EMPTY and GAP DETECTION.
TIMING			
			The user must provide four timing signals to the μPD371 – one for write operations and three for read operations. Each is defined in terms of T, where T is the period between successive data transitions in the phase encoded data written onto or read from tape.
39	WCK		<p>WCK determines the WRITE DATA (WD, pin 36) transfer rate. WCK should have a period of 0.5T.</p> <p>DT is a pulse provided by the μPD371 to be used in the generation of the three read timing signals – SG, DO, and GAP. DT occurs at each data transition in the data read from tape.</p> <p>The internal read data sample gate is closed following each data transition and is reopened by a positive transition at SG 0.75T μsec after each DT pulse. A positive transition should be made at DO whenever a DT pulse stream ceases for a period of 1.5T μsec. A positive transition should be made at GAP whenever a DT pulse stream ceases for a period of 4T μsec.</p> <p>φ1 and φ2 are MOS level (12V) clock pulses. The timing of φ1 and φ2 is shown in the Timing Diagram.</p>
16	DT		
34	SG		
38	DO		
35	GAP		
20	φ1		
23	φ2		
WRITE DATA			
36	WD		Phase encoded data to be written on tape leaves the μPD371 at pin 36.
TAPE DRIVE COMMAND AND STATUS			
37	C ₁		<p>C₁, C₂ and C₃ are general purpose tape drive commands. C₁, C₂ and C₃ are set and reset by the software manipulation of bits 5, 6 and 7, respectively, in Write Register 3. Since C₁, C₂ and C₃ are defined by software, they may be configured for any purpose. Typical uses for C₁, C₂ and C₃ are WRITE ENABLE, FORWARD and REVERSE.</p>
27	C ₂		
28	C ₃		
29	S ₁		<p>S₁, S₂ and S₃ are general purpose tape drive status inputs. Their logic levels are indicated by bits 3, 4 and 7 of Read Register 1, respectively. Typical tape drive status signals are WRITE PERMIT, CASSETTE IN PLACE and SIDE.</p> <p>The μPD371 can adapt to any tape drive status signal set with a slight change in software.</p>
26	S ₂		
25	S ₃		
DUAL TAPE DRIVE SYSTEM COMMAND AND STATUS			
17	UA	Unit Address	Selects Drive 0 when low and Drive 1 when high.
19	RW ₀	Rewind 0	Rewind Command for Drive 0.
18	RW ₁	Rewind 1	Rewind Command for Drive 1.
30	MK ₀	Marker 0	EOT/BOT status from Drive 0.
31	MK ₁	Marker 1	EOT/BOT status from Drive 1.
READ DATA			
32	RD(+)	Read Data (+)	A positive pulse from the tape drive at each positive transition in the read data.
33	RD(-)	Read Data (-)	A positive pulse from the tape drive at each negative transition in the read data.
MISCELLANEOUS			
1	MBH		MBH must be tied to the V _{CC} (+5V) supply.
42	AWL		AWL is a logic low output under all normal operating conditions of the μPD371.
POWER SUPPLY VOLTAGES			
2	V _{DD}		+12V
41	V _{CC}		+5V
22	V _{SS}		Ground
21	V _{BB}		-5V

Note: ① Refer to diagram on following page.

PIN IDENTIFICATION
(CONT.)



PACKAGE OUTLINE
μPD371D



ITEM	MILLIMETERS	INCHES
A	53.5 MAX	2.1 MAX
B	1.35	0.05
C	2.54	0.10
D	50.80	2.0
F	1.27	0.05
G	2.54 MAX	0.10 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.21 MAX
K	15.24	0.60
L	13.50	0.53
M	0.3	0.012

μ PD371

From the point of view of the processor program, the μPD371 makes the tape drive (or multiple drive system) appear as ten addressable registers. The program controls the drive(s) and transmits data to be written on tape by manipulating bits in the six μPD371 Write Registers. The program senses the status of the drive(s) and reads data stored on tape by reading bits from the four μPD371 Read Registers.

ADDRESSABLE INTERNAL REGISTERS

REGISTER ADDRESS				REGISTER NAME	BIT NUMBERS							
W/R	RS ₂	RS ₁	RS ₀		7	6	5	4	3	2	1	0

WRITE REGISTERS

1	0	0	0	WR ₀	RST	MBL	SRS	WME	WCR	X	WMD	GNT
1	0	0	1	WR ₁	WRR	RRR	X	RRE	RRD	GRE	GRD	X
1	0	1	0	WR ₂	WD ₇	WD ₆	WD ₅	WD ₄	WD ₃	WD ₂	WD ₁	WD ₀
1	0	1	1	WR ₃	C ₃	C ₂	C ₁	RR1	RW	X	X	X
1	1	0	1	WR ₅	X	X	X	RME	RMD	X	X	X
1	1	1	0	WR ₆	X	X	X	X	X	X	X	UA

READ REGISTERS

0	0	0	0	RR ₀	AWH	AWL	C ₂	C ₃	RDF	GRQ	WRQ	RRQ
0	0	0	1	RR ₁	S ₃	MK	MKF	S ₂	S ₁	RW	C ₁	UA
0	0	1	0	RR ₂	RD ₇	RD ₆	RD ₅	RD ₄	RD ₃	RD ₂	RD ₁	RD ₀
0	0	1	1	RR ₃	WD	GPF	REC	CRE	DOE	COR	NBR	NAR

X = NOT USED

ADDRESSABLE
INTERNAL REGISTER
BIT
IDENTIFICATION

BIT	SYMBOL	NAME
WRITE REGISTER 0		
0	GNT	Gap Noise Tolerance
1	WMD	Write Mode Disable
2	—	Not used
3	WCR	Write CRC
4	WME	Write Mode Enable
5	SRS	Status Reset
6	MBL	Must Be Low
7	RST	Reset
WRITE REGISTER 1		
0	—	Not used
1	GRD	Gap Request Disable
2	GRE	Gap Request Enable
3	RRD	Read Request Disable
4	RRE	Read Request Enable
5	—	Not used
6	RRR	Read Request Reset
7	WRR	Write Request Reset
WRITE REGISTER 2		
0 – 7	WD ₀ – WD ₇	Write Buffer Register
WRITE REGISTER 3		
0	—	Not used
1	—	Not used
2	—	Not used
3	RW	Rewind
4	RR1	Rewind Reset Inhibit
5	C ₁	Command One
6	C ₂	Command Two
7	C ₃	Command Three
WRITE REGISTER 4		
—	—	Not used
WRITE REGISTER 5		
0	—	Not used
1	—	Not used
2	—	Not used
3	RMD	Read Mode Disable
4	RME	Read Mode Enable
5	—	Not used
6	—	Not used
7	—	Not used

BIT	SYMBOL	NAME
WRITE REGISTER 6		
0	UA	Unit Address
1 – 7	—	Not used
READ REGISTER 0		
0	RRO	Read Request
1	WRQ	Write Request
2	GRO	Gap Request
3	RDF	Read Flag
4	C ₃	Command 3
5	C ₂	Command 2
6	AWL	Always Low
7	AWH	Always High
READ REGISTER 1		
0	UA	Unit Address
1	C ₁	Command 1
2	RW	Rewind
3	S ₁	Status 1
4	S ₂	Status 2
5	MKF	Marker Flag
6	MK	Marker
7	S ₃	Status 3
READ REGISTER 2		
0 – 7	RD ₀ – RD ₇	Read Buffer Register
READ REGISTER 3		
0	NAR	Noise After Record
1	NBR	Noise Before Record
2	COR	Command Overrun
3	DOE	Drop Out Error
4	CRE	CRC Error
5	REC	Record Detection
6	GPF	Gap Flag
7	WD	Write Data

