Description

The μPD71088 is a CMOS system bus controller for a μPD70108 (V20™) or μPD70116 (V30™) microprocessor system. It controls the memory or I/O system bus.

Features

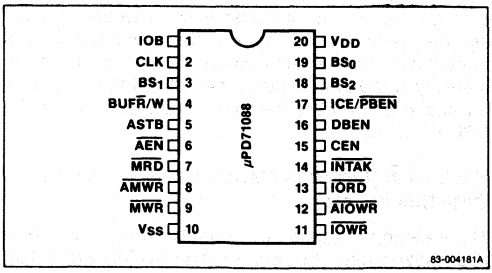
- ☐ CMOS technology
- ☐ Bus controller for microcomputer system expansion
- ☐ Command outputs for system bus control
- ☐ Control outputs for I/O peripheral bus control
- ☐ High drive capability for command and control outputs (I_{OL} = 12 mA)
- ☐ Three-state outputs for command outputs
- ☐ Advanced I/O and memory write command outputs
- ☐ μPD70108, μPD70116 compatible
- ☐ +5-volt ±10% single power supply
- ☐ 20-pin plastic DIP (300 mil) or SO package
- ☐ Industrial temperature range: −40 to +85 °C

Ordering Information

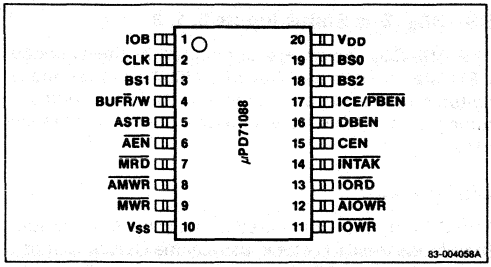
Part Number	Package Type	Max Frequency of Operation
μPD71088C	20-pin plastic DIP	8 MHz
C-10	20-pin plastic DIP	10 MHz
G	20-pin plastic SO	8 MHz

Pin Configurations

20-Pin Plastic DIP



20-Pin Plastic SO



Pin Identification

Symbol	Function
IOB	Input/output bus mode input
CLK	Clock input
BS_1	Bus status input 1
BUFR/W	Buffer read/write output
ASTB	Address strobe output
AEN	Address enable input
MRD	Memory read output
AMWR	Advanced memory write output
MWR	Memory write command output
V_{SS}	Ground
IOWR	I/O write command output
AIOWR	Advanced I/O write command output
IORD	I/O read command output
INTAK	Interrupt acknowledge output
CEN	Command enable input
DBEN	Data buffer enable output
ICE/PBEN	Interrupt cascade enable/Peripheral data bus enable output
BS_2	Bus status input 2
BS_0	Bus status input 0
V_{DD}	Power supply

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Pin Functions

BS_0-BS_2 [Bus Status Inputs 0, 1, 2]

The BS_0-BS_2 inputs are connected to the encoded CPU status outputs. The μPD71088 decodes these status outputs into command and control outputs for timing control. See table 1 for an explanation of these inputs.

CLK [Clock]

The CLK input is connected to the same clock output that drives the CPU clock, usually the CLK output of a μPD71084 or a μPD71011. It is the internal system clock of the μPD71088.

$\overline{AEN}$ [Address Enable]

The $\overline{AEN}$ input controls the command output buffers. When IOB is low, a low-level $\overline{AEN}$ causes the command buffers to output command output signals. A high-level $\overline{AEN}$ makes all command lines go to high impedance. When IOB is high, the μPD71088 is in I/O bus mode, and the command lines are not affected by $\overline{AEN}$.

CEN [Command Enable]

The CEN input controls DBEN, $\overline{PBEN}$ and all command outputs. When CEN is high, all these outputs are active. When CEN is low, they are inactive.

IOB [I/O Bus Mode]

When the IOB input is high, the bus control mode is I/O bus mode. When IOB is low, the bus control mode is system bus mode.

$\overline{MRD}$ [Memory Read Command]

The $\overline{MRD}$ output is the signal to read data from a memory device. $\overline{MRD}$ is three-state, active low.

$\overline{MWR}$ [Memory Write Command]

The $\overline{MWR}$ output is the signal to write data to a memory device. $\overline{MWR}$ is three-state, active low.

$\overline{AMWR}$ [Advanced Memory Write Command]

This command output is the same as $\overline{MWR}$, except that it is generated one state (clock cycle) earlier than $\overline{MWR}$.

$\overline{IORD}$ [I/O Read Command]

The $\overline{IORD}$ output is the signal to read data from an I/O device. $\overline{IORD}$ is three-state, active low.

$\overline{IOWR}$ [I/O Write Command]

The $\overline{IOWR}$ output is the signal to write data to an I/O device. $\overline{IOWR}$ is three-state, active low.

$\overline{AIOWR}$ [Advanced I/O Write Command]

This command output is the same as $\overline{IOWR}$, except that it is generated one state (clock cycle) earlier than $\overline{IOWR}$.

$\overline{INTAK}$ [Interrupt Acknowledge]

The $\overline{INTAK}$ output acknowledges interrupt requests. Requesting devices output an interrupt vector address in response to $\overline{INTAK}$. $\overline{INTAK}$ is three-state, active low.

ASTB [Address Strobe]

The ASTB output control signal latches the address outputs from the CPU into an external address latch, such as a μPD71082 or μPD71083. Address data should be strobed with the trailing edge (high to low) of ASTB.

DBEN [Data Buffer Enable]

The DBEN output activates a data bus buffer/driver such as a μPD71086 or μPD71087 to input or output data between the CPU local bus and the memory or I/O system bus.

$BUF\overline{R}/W$ [Buffer Read/Write]

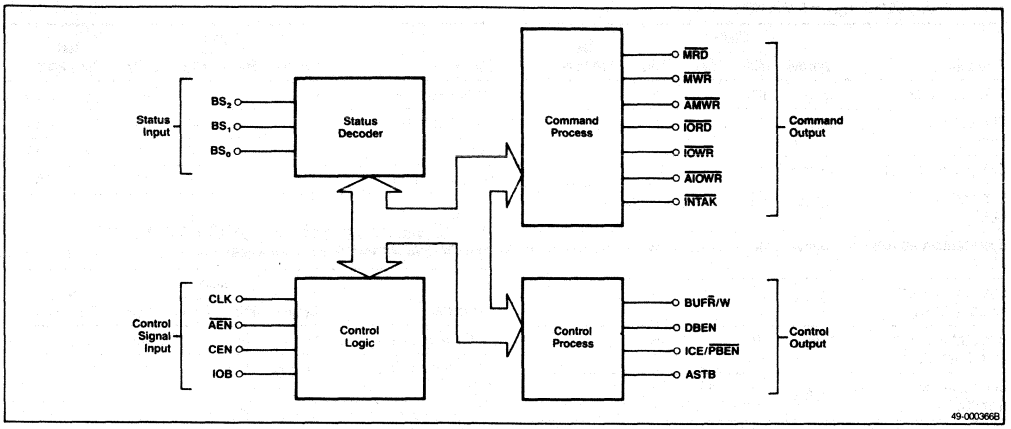
The $BUF\overline{R}/W$ output controls the direction in which data moves through a transceiver between the CPU and the memory or I/O peripherals. When $BUF\overline{R}/W$ is high, data is transferred from the CPU local bus to the memory or I/O system bus. When $BUF\overline{R}/W$ is low, data is transferred from the memory or I/O system bus to the CPU local bus.

ICE/$\overline{PBEN}$ [Interrupt Cascade Enable/Peripheral Data Bus Enable]

The meaning of this output signal depends on IOB. If IOB is low (system bus mode), it is the ICE output. ICE controls the cascade address transfer from a master priority interrupt controller to slave priority interrupt controllers. The slave reads the address from the master when ICE goes high.

When IOB is high, it becomes $\overline{PBEN}$. $\overline{PBEN}$ controls the I/O bus the same way that DBEN controls the system bus. In this case, however, the output is active low.

Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$; $V_{SS} = 0$ V

Power supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−1.0 to V_{DD} + 1.0 V
Output voltage, V_O	−0.5 to V_{DD} ± 0.5 V
Operating temperature, T_{opt}	−40 to +85°C
Storage temperature, T_{stg}	−65 to +150°C
Power dissipation, P_D (DIP)	500 mW
Power dissipation, P_D (SO)	200 mW

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

DC Characteristics

$T_A = -40°C$ to +85°C; $V_{DD} = 5$ V ±10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input voltage, high	V_{IH}	2.2		V	
Input voltage, low	V_{IL}		0.8	V	
Output voltage, high	V_{OH}	V_{DD} − 0.8		V	Commands, $I_{OH} = -12$ mA; Controls, $I_{OH} = -4$ mA
Output voltage, low	V_{OL}		0.45	V	Commands, $I_{OL} = 12$ mA; Controls, $I_{OL} = 4$ mA;
Input current leakage	I_{IL}	−1.0	1.0	μA	$V_I = V_{DD}, V_{SS}$
Leakage current at high impedance	I_{OFF}	−10	10	μA	
Power supply current (static)	I_{DD}		80	μA	$V_I = V_{DD}, V_{SS}$
Power supply current (dynamic)	I_{DDdyn}		20	mA	$f_{in} = 10$ MHz

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AC Characteristics, μPD71088

$T_A = -40$ to $+85°C$; $V_{DD} = 5$ V ±10%

Parameter	Symbol	Limits Min	Limits Max	Units	Test Conditions
CLK cycle time	t_{CYCK}	125		ns	
CLK pulse width, high	t_{PWCKH}	40		ns	
CLK pulse width, low	t_{PWCKL}	60		ns	
Bus status setup to CLK↑	t_{SBSV}	40		ns	
Bus status hold from CLK↓	t_{HBSV}	10		ns	
Bus status inactive setup to CLK↓	t_{SBSIV}	35		ns	
Bus status inactive hold from CLK↑	t_{HBSIV}	10		ns	
Command active delay from CLK↓	t_{DCML}	10	40	ns	
Command inactive delay from CLK↓	t_{DCMH}	10	40	ns	
Command output on delay from $\overline{AEN}$↓	t_{DAECM}		40	ns	
Command active delay from $\overline{AEN}$↓	t_{DAECML}	100	295	ns	
Command active delay from CEN↑	t_{DCECM}		t_{DCML}	ns	
Command output float delay from $\overline{AEN}$↑	t_{FAECM}		50	ns	
ASTB active delay from CLK↓	t_{DCKSTH}		30	ns	
ASTB active delay from BS2, 1, 0	t_{DBSST}		25	ns	
ASTB inactive delay from CLK↑	t_{DCKSTL}	7	25	ns	
DBEN, $\overline{PBEN}$ active delay from CLK↓	t_{DCTV}	10	50	ns	
DBEN, $\overline{PBEN}$ inactive delay from CLK↑	t_{DCT}	10	50	ns	
DBEN, $\overline{PBEN}$ active delay from $\overline{AEN}$↓	t_{DAECTK}		30	ns	
DBEN, $\overline{PBEN}$ active delay from CEN↑	t_{DCECT}		30	ns	
BUF$\overline{R}$/W↑ delay from CLK↑	t_{DCKWR}		40	ns	
BUF$\overline{R}$/W↓ delay from CLK↑	t_{DCKRD}		60	ns	
ICE active delay from CLK↓	t_{DCKIC}		30	ns	
ICE active delay from BS2, 1, 0	t_{DBSIC}		25	ns	
ICE inactive delay from CLK↓	t_{DICL}	10	50	ns	
Input rise time	t_{RI}		20	ns	0.8 V → 2.0 V
Input fall time	t_{FI}		12	ns	2.0 V → 0.8 V
Output rise time	t_{RO}		20	ns	0.8 V → 2.0 V
Output fall time	t_{FO}		12	ns	2.0 V → 0.8 V

AC Characteristics, μPD71088-10

$T_A = -10$ to $+70°C$; $V_{DD} = 5$ V ±10%

Parameter	Symbol	Limits Min	Limits Max	Units	Test Conditions
CLK cycle time	t_{CYCK}	100		ns	
CLK pulse width, high	t_{PWCKH}	41		ns	
CLK pulse width, low	t_{PWCKL}	49		ns	
Bus status setup to CLK↑	t_{SBSV}	35		ns	
Bus status hold from CLK↓	t_{HBSV}	10		ns	
Bus status inactive setup to CLK↓	t_{SBSIV}	35		ns	
Bus status inactive hold from CLK↑	t_{HBSIV}	10		ns	
Command active delay from CLK↓	t_{DCML}	10	35	ns	
Command inactive delay from CLK↓	t_{DCMH}	10	35	ns	
Command output on delay from $\overline{AEN}$↓	t_{DAECM}		40	ns	
Command active delay from $\overline{AEN}$↓	t_{DAECML}	115	200	ns	
Command active delay from CEN↑	t_{DCECM}		t_{CLML}	ns	
Command output float delay from $\overline{AEN}$↑	t_{FAECM}		40	ns	
ASTB active delay from CLK↓	t_{DCKSTH}		20	ns	
ASTB active delay from BS2, 1, 0	t_{DBSST}		20	ns	
ASTB inactive delay from CLK↑	t_{DCKSTL}	7	25	ns	
DBEN, $\overline{PBEN}$ active delay from CLK↓	t_{DCTV}	10	35	ns	
DBEN, $\overline{PBEN}$ inactive delay from CLK↑	t_{DCT}	10	35	ns	
DBEN, $\overline{PBEN}$ active delay from $\overline{AEN}$↓	t_{DAECTK}		30	ns	
DBEN, $\overline{PBEN}$ active delay from CEN↑	t_{DCECT}		30	ns	

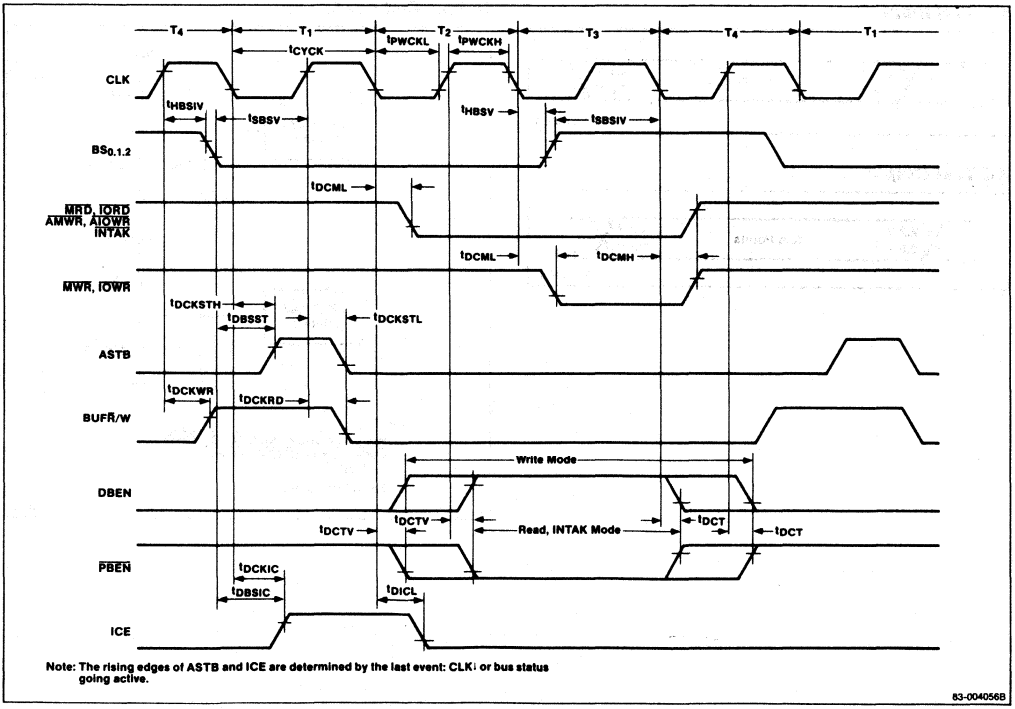
AC Characteristics, μPD71088-10 (cont)

$T_A = -10$ to $+70°C$; $V_{DD} = 5$ V ±10%

Parameter	Symbol	Limits Min	Limits Max	Units	Test Conditions
BUF$\overline{R}$/W↑ delay from CLK↑	t_{DCKWR}		40	ns	
BUF$\overline{R}$/W↓ delay from CLK↑	t_{DCKRD}		40	ns	
ICE active delay from CLK↓	t_{DCKIC}		30	ns	
ICE active delay from BS2, 1, 0	t_{DBSIC}		20	ns	
ICE inactive delay from CLK↓	t_{DICL}	10	40	ns	
Input rise time	t_{RI}		20	ns	0.8 V → 2.0 V
Input fall time	t_{FI}		12	ns	2.0 V → 0.8 V
Output rise time	t_{RO}		20	ns	0.8 V → 2.0 V
Output fall time	t_{FO}		12	ns	2.0 V → 0.8 V

Timing Waveforms

General



Note: The rising edges of ASTB and ICE are determined by the last event: CLKi or bus status going active.

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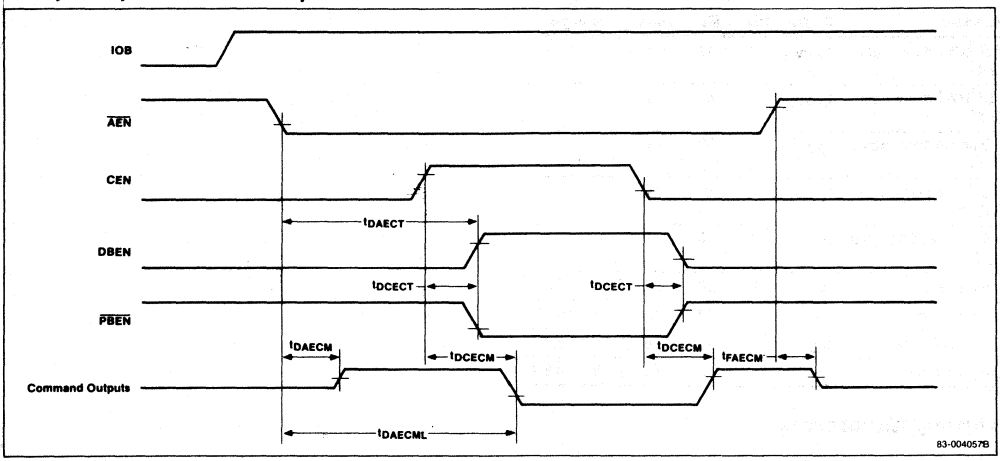
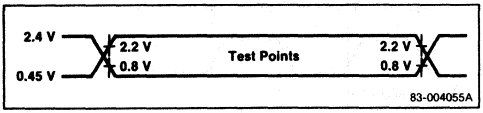
Timing Waveforms (cont)

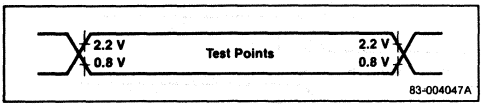
DBEN, $\overline{PBEN}$, and Command Output



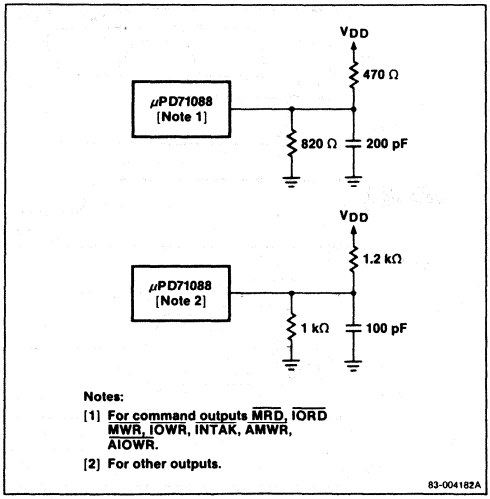
AC Test Input



AC Test Output



Output Test Loads



Bus Controller Functional Description

Command Logic

The μPD71088 decodes the CPU bus status outputs into command outputs. The bus status outputs (BS_0-BS_2) and their decoded commands are shown in table 1.

Table 1. Command Logic

BS_2	BS_1	BS_0	CPU Status	μPD71088 Command Output
Low	Low	Low	Interrupt acknowledge	$\overline{INTAK}$
Low	Low	High	I/O read mode	$\overline{IORD}$
Low	High	Low	I/O write mode	$\overline{IOWR}$, $\overline{AIOWR}$
Low	High	High	Halt mode	None
High	Low	Low	Instruction fetch mode	$\overline{MRD}$
High	Low	High	Memory read mode	$\overline{MRD}$
High	High	Low	Memory write mode	$\overline{MWR}$, $\overline{AMWR}$
High	High	High	No bus cycle mode	None

Bus Control Mode

The CEN, IOB, and $\overline{AEN}$ signals control the bus controller mode as shown in table 2.

Table 2. Bus Control Mode

Control Input			Command Output		Control Output	
			Memory	I/O		
CEN	IOB	$\overline{AEN}$	$\overline{MRD}$, $\overline{MWR}$, $\overline{AMWR}$	$\overline{IOWR}$, $\overline{AIOWR}$, $\overline{IORD}$, $\overline{INTAK}$	ICE/$\overline{PBEN}$	ASTB, BUF$\overline{R}$/W, DBEN
H	H (I/O bus mode)	H	High impedance	Outputs enabled (NC)	$\overline{PBEN}$ (NC)	Outputs enabled (NC)
		L	Outputs enabled			
H	L (System bus mode)	H	High impedance	High impedance	ICE (NC)	Outputs enabled (NC)
		L	Outputs enabled	Outputs enabled		
L (Command disable mode)	x	x	H	H	$\overline{PBEN}$ = H	Outputs enabled (DBEN = L: ASTB, BUFR/W are NC)

Note:

x = Don't care, NC = No change, H = High, L = Low

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