NEC

NEC Microcomputers, Inc.

Application Note 14

Power-On-Reset Circuitry For μCom-4 Microcomputer Designs

Any product designed around one of the μCOM-4 4-bit single chip microcomputers will require connection of some external circuitry to the RESET input for correct operation. This circuitry ensures the proper timing sequence for the various portions of the microcomputer's internal logic during power-up. The product design engineer should be aware of several approaches to this circuitry design and the associated cost-performance trade-offs.

Under ideal conditions, the rise time (t_r) of the RESET input signal need not be very fast. Once the high level is reached, the RESET input signal should remain stable at that level for a minimum of 4 instruction cycles (40 μs). The fall time (t_f) of the RESET input signal should be as short as possible to minimize any possible effects of noise. The t_f should be less than one instruction cycle (10 μs) for optimal performance.

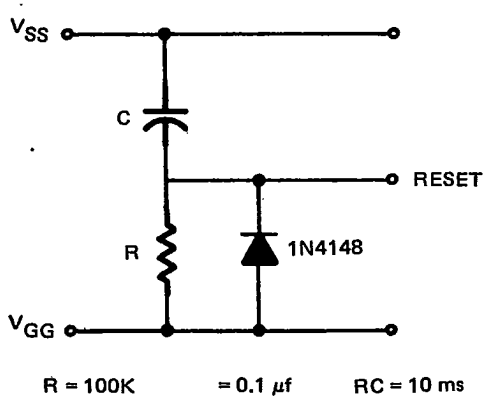
Under actual conditions, the design engineer should make t_f as close to 10 μs as possible while maintaining the overall cost-performance objectives for his product. The application engineers at NEC Microcomputers, Inc. have developed several implementations of the external power-on-reset circuitry which allow the design engineer to attain those objectives. All of these circuits work equally well with the following μCOM-4 4-bit microcomputers:

μPD546	μPD547	μPD550
μPD553	μPD547L	μPD550L
μPD556	μPD552	μPD554
μPD557L	μPD651	μPD554L
μPD650		μPD652

For products where there is little or no noise on the power supply lines, as with a battery power supply design, the t_f requirements of the RESET input signal are not critical. The design engineer can obtain very satisfactory system performance at low cost with the power-on-reset circuit shown in Figure 1.

For products where there is noise on the power supply lines, as with switching or A/C-transformer power supply designs, the t_f requirements of the RESET input signal are critical, and the above circuit does not provide a fast enough t_f for consistently good performance. Instead, the design engineer can obtain very satisfactory system performance at reasonable cost with either of the power-on-reset circuits shown in Figure 2.

Simple R-C Reset Circuit



Reset Voltage Vs. Time

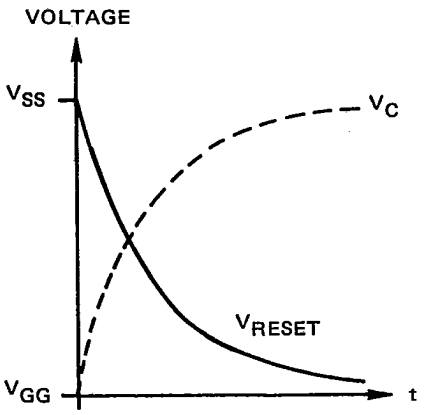
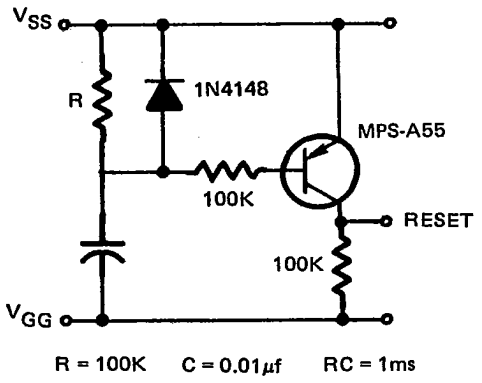


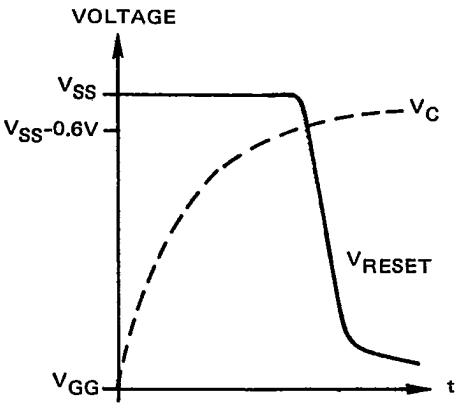
Figure 1

Transistor-Switch Reset Circuit

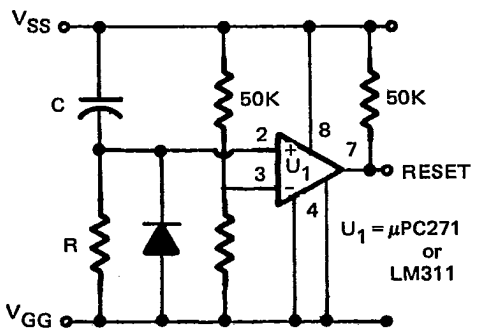


R = 100K C = 0.01μf RC = 1ms

Reset Voltage Vs. Time



Comparator Reset Circuit



R = 10K C = 10μf RC = 100ms

Reset Voltage Vs. Time

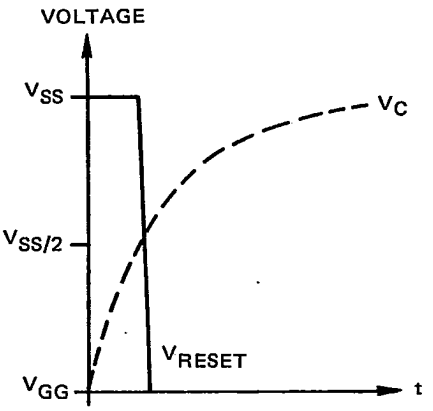


Figure 2

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