μPD8155/56
2048-BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

Description

The μPD8155 and μPD8156 are μPD8085A family components having 256 × 8-bit static RAM, 3 programmable I/O ports, and a programmable timer. They directly interface to the multiplexed μPD8085A bus with no external logic. The μPD8155 has an active low chip enable while the μPD8156 is active high.

The μPD8155 and μPD8156 contain 2048 bits (256 × 8) of static RAM. The 256 words of memory may be selected anywhere within the system's 64K memory space by coding the upper 8 bits of address from the μPD8085A as a chip select.

The two general purpose 8-bit ports (PA and PB) may be programmed for input or output either in interrupt or status mode. The single 6-bit port (PC) may be used as a control for PA and PB or as a general purpose I/O port. The μPD8155 and μPD8156 are programmed for their system personalities by writing into their command/status (C/S) registers upon system initialization.

The timer is a single 14-bit down counter which is programmable for 4 modes of output operation; see table 3.

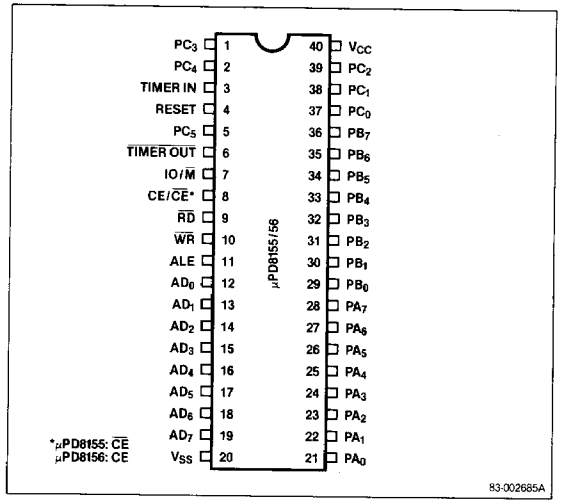
Features

- ☐ 256 × 8-bit static RAM
- ☐ Two programmable 8-bit I/O ports
- ☐ One programmable 6-bit I/O port
- ☐ Single +5 V ± 10% power supply
- ☐ Directly interfaces to the μPD8085A and μPD8085A-2
- ☐ Programmable 14-bit binary counter/timer

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD8155C/55HC	40-pin plastic DIP	3 MHz
μPD8155C-2/55HC-2	40-pin plastic DIP	5 MHz
μPD8156C/56HC	40-pin plastic DIP	3 MHz
μPD8156C-2/56HC-2	40-pin plastic DIP	5 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1, 2, 5, 37-39	PC_0-PC_5	6-bit I/O port or control lines
3	TIMER IN	Timer clock input
4	RESET	Reset input
6	$\overline{\text{TIMER OUT}}$	Timer counter output
7	IO/$\overline{M}$	I/O or memory select input
8	CE/$\overline{CE}$	Chip enable input
9	$\overline{RD}$	Read strobe input
10	$\overline{WR}$	Write strobe input
11	ALE	Address low enable input
12-19	AD_0-AD_7	Low address/data bus I/O
20	V_{SS}	Ground
21-28	PA_0-PA_7	8-bit I/O port A
29-36	PB_0-PB_7	8-bit I/O port B
40	V_{CC}	+5 V power supply

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Pin Functions

AD_0-AD_7 (Low Address/Data Bus)

Three-state address/data (AD) lines that interface with the CPU lower 8-bit address/data bus. The 8-bit address is loaded into the internal address latch on the falling edge of ALE. The 8-bit data is then written to or read from the chip, based on $\overline{WR}$ and $\overline{RD}$ strobe inputs.

PA_0-PA_7 (Port A)

8-bit general purpose I/O port. Data direction is selected by programming the command status register.

PB_0-PB_7 (Port B)

8-bit general purpose I/O port. Data direction is selected by programming the command status register.

PC_0-PC_5 (Port C)

6-bit general purpose I/O port or control signals for PA and PB. Port C function is selected by programming the command status register.

ALE (Address Low Enable)

This input control signal latches the address on the AD_0-AD_7 lines and the states of CE/$\overline{CE}$ and IO/$\overline{M}$ into the chip on the falling edge of ALE.

CE/$\overline{CE}$ (Chip Enable)

The chip enable input is active low for μPD8155 and active high for μPD8156.

IO/$\overline{M}$ (I/O or Memory Select)

This input selects either internal RAM memory if low or I/O and command status registers if high.

RESET (Reset)

The reset input from μPD8085A initializes ports A, B, and C to the input mode.

TIMER IN (Timer Clock In)

Clock input to the 14-bit binary down counter.

$\overline{TIMER\ OUT}$ (Timer Counter Output)

The timer output is programmable for 4 output waveform modes. The selected output waveform can be a single pulse or a continuous pulse train, or it can be a single square wave or a continuous square wave.

$\overline{RD}$ (Read Strobe)

The $\overline{RD}$ input will strobe the addressed RAM data onto the AD bus if the IO/$\overline{M}$ pin is low; otherwise the content of the selected I/O port or command status registers will be strobed onto the AD bus.

$\overline{WR}$ (Write Strobe)

The $\overline{WR}$ input will strobe the available data on the AD bus into addressed RAM location or I/O ports and command status registers depending on IO/$\overline{M}$.

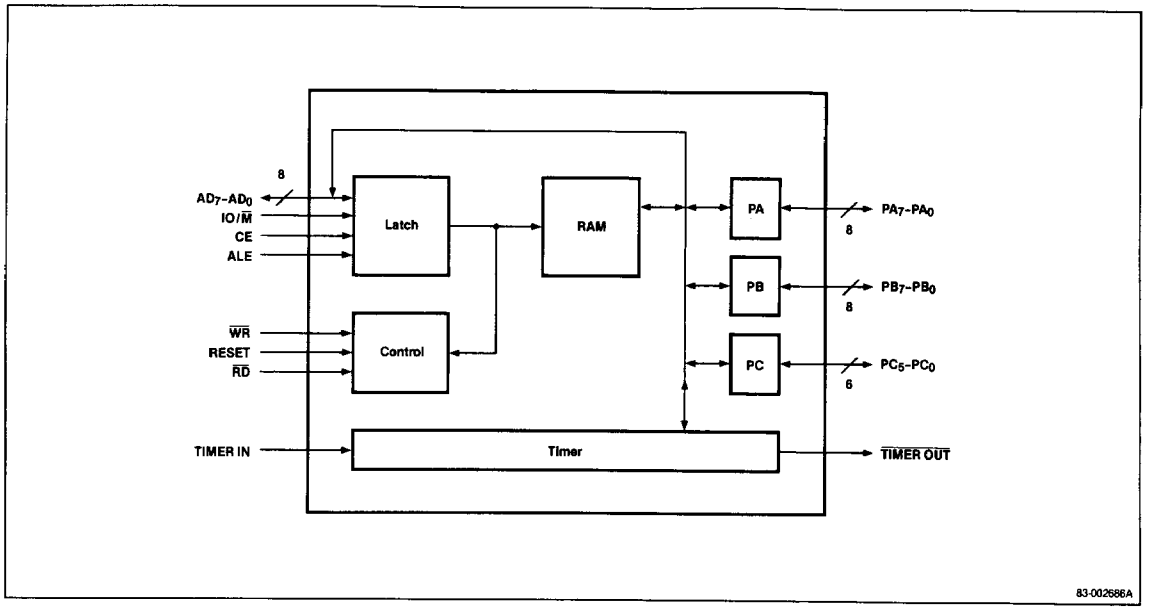
V_{CC} (Power Supply)

+5 V power supply input.

V_{SS} (Ground)

Ground.

Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{CC}	−0.5 V to +7 V
Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Power dissipation, P_D	1.5 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.5		0.8	V	
Input voltage high	V_{IH}	2.0		$V_{CC}+0.5$	V	
Output voltage low	V_{OL}			0.45	V	$I_{OL} = 2.0\,mA$
Output voltage high	V_{OH}	2.4			V	$I_{OH} = 400\,\mu A$
Input leakage current	I_{LI}			±10	μA	$V_I = V_{CC}$ to 0 V
Output leakage current	I_{LO}			±10	μA	$0.45\,V \leq V_{OUT} \leq V_{CC}$
Power supply current (V_{CC})	I_{CC}			180	mA	8155/56, 8155-2/56-2
				125	mA	8155H/56H, 8155H-2/56H-2
Chip enable leakage	μPD8155 I_{IL}(CE)			+100	μA	$V_I = V_{CC}$ to 0 V
	μPD8156			−100	μA	$V_I = V_{CC}$ to 0 V

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AC Characteristics

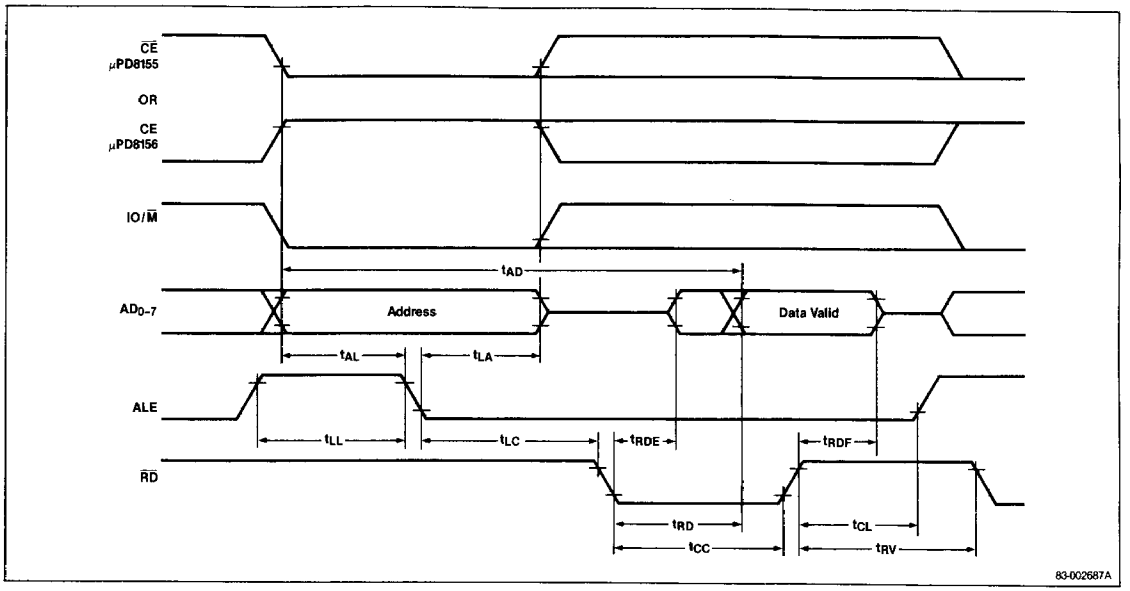
$T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$

Parameter	Symbol	Limits μPD8155/56/55H/56H Min	Limits μPD8155/56/55H/56H Max	Limits μPD8155-2/56-2/55H-2/56H-2 Min	Limits μPD8155-2/56-2/55H-2/56H-2 Max	Unit	Test Conditions(1)
Address to latch setup time	t_{AL}	50		30		ns	
Address hold time after latch	t_{LA}	80		30		ns	
Latch to READ / WRITE control	t_{LC}	100		40		ns	
Valid data out delay from READ control	t_{RD}		170		140	ns	
Address stable to data out valid	t_{AD}		400		330	ns	
Latch enable width	t_{LL}	100		70		ns	
Data bus float after READ	t_{RDF}	0	100	0	80	ns	
READ / WRITE control to latch enable	t_{CL}	20		10		ns	
READ / WRITE control width	t_{CC}	250		200		ns	
Data in to WRITE setup time	t_{DW}	150		100		ns	
Data in hold time after WRITE	t_{WD}	0		0		ns	
Recovery time between controls	t_{RV}	300		200		ns	
WRITE to port output	t_{WP}		400		300	ns	
Port input setup time	t_{PR}	70		50		ns	
Port input hold time	t_{RP}	50		10		ns	
Strobe to buffer full	t_{SBF}		400		300	ns	
Strobe width	t_{SS}	200		150		ns	
READ to buffer empty	t_{RBE}		400		300	ns	
Strobe to INTR on	t_{SI}		400		300	ns	
READ to INTR off	t_{RDI}		400		300	ns	
Port setup time to strobe	t_{PSS}	50		0		ns	
Port hold time after strobe	t_{PHS}	120		100		ns	
Strobe to buffer empty	t_{SBE}		400		300	ns	
WRITE to buffer full	t_{WBE}		400		300	ns	
WRITE to INTR off	t_{WI}		400		300	ns	
TIMER IN to $\overline{\text{TIMER OUT}}$ low	t_{TL}		400		300	ns	
TIMER IN to $\overline{\text{TIMER OUT}}$ high	t_{TH}		400		300	ns	
Data bus enable from READ control	t_{RDE}	10		10		ns	
Clock TIMER IN	t_{CYC}	320		200		ns	
CLK rise and fall time	t_r, t_f		30		30	ns	
CLK pulse width	t_1	80		40		ns	
	t_2	120		70		ns	

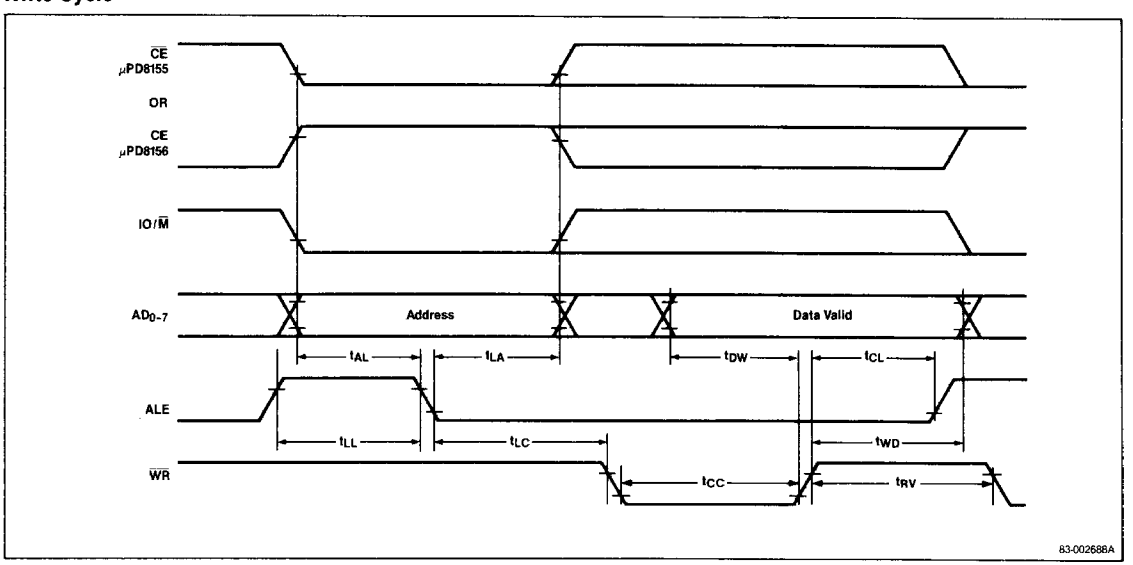
Note:
(1) 150 pF load

Timing Waveforms

Read Cycle



Write Cycle



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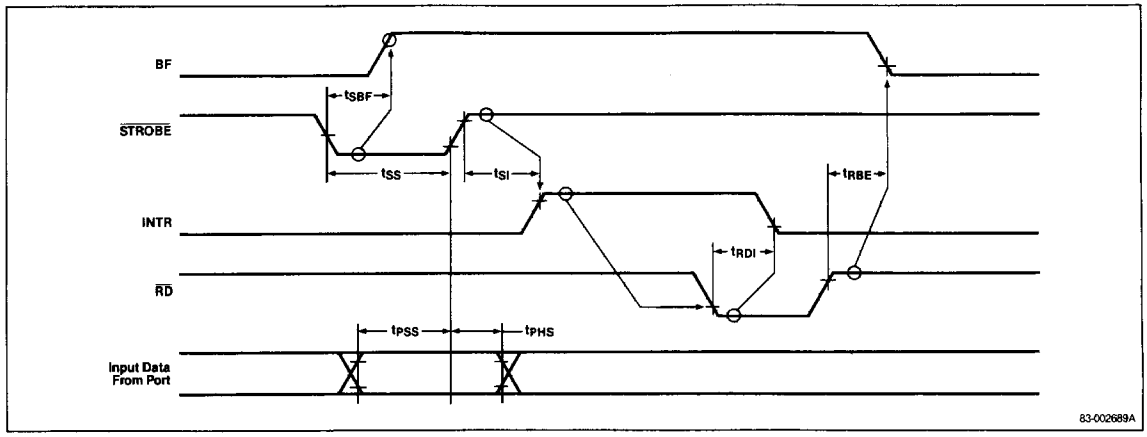
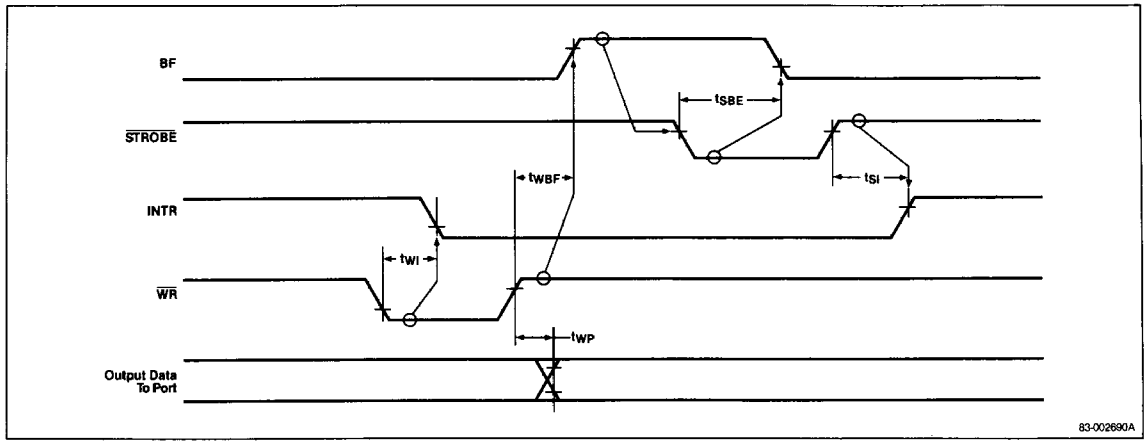
Timing Waveforms (cont)

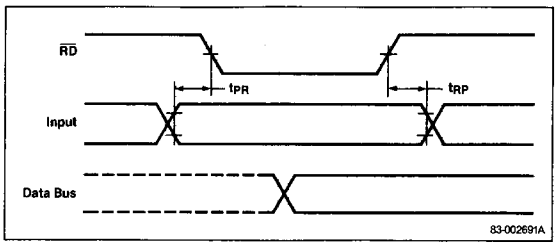
Strobed Input Mode



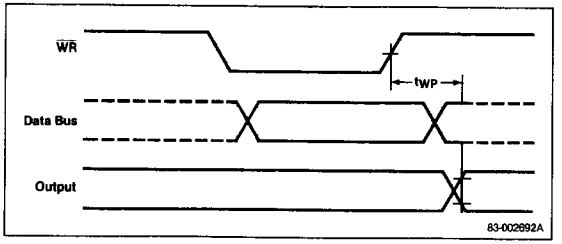
Strobed Output Mode



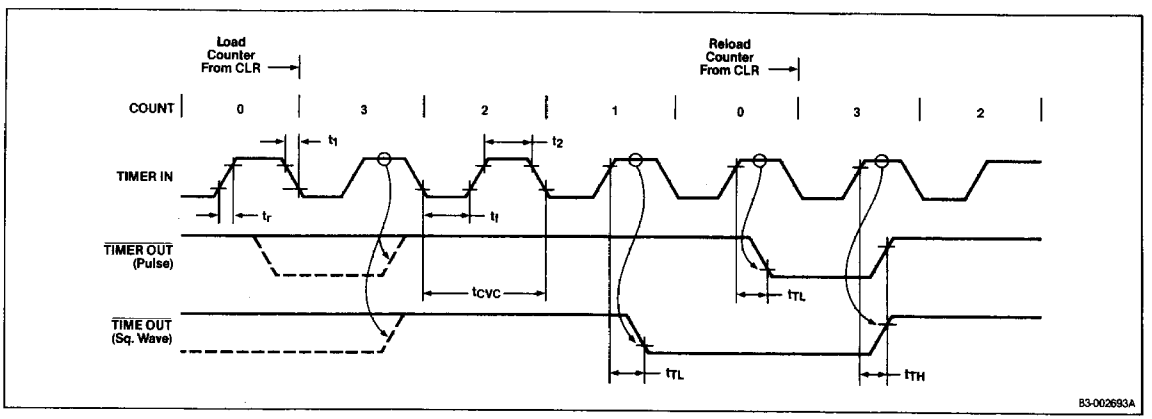
Basic Input Mode



Basic Output Mode



Time Output



Functional Description

Command Status Register

The command status register is an 8-bit register which must be programmed before the μPD8155/56 can perform any useful functions. Its purpose is to define the mode of operation of the three ports and the timer. Programming of the device may be accomplished by writing to I/O address XXXXX000 (X = don't care) with a specific bit pattern. Reading of the command status register can be accomplished by performing an I/O read operation at address XXXXX000. The pattern returned will be a 7-bit status report of PA, PB and the timer. The bit patterns for the command status register read and write are shown in tables 1 and 2.

Table 1. Command Status Write

TM2	TM1	IEB	IEA	PC_2	PC_1	PB	PA

where:
TM2-TM1 = Define timer mode
IEB = Enable port B interrupt
IEA = Enable port A interrupt
PC_2-PC_1 = Define port C mode
PB/PA = Define port B/A as in or out(1)

The timer mode of operation is programmed as follows during command status write:

TM2	TM1	Timer Mode
0	0	Don't affect timer operation
0	1	Stop timer counting
1	0	Stop counting after TC
1	1	Start timer operation

Interrupt enable status is programmed as follows:

IEB/IEA	Interrupt Enable Port B/A
0	No
1	Yes

Port C may be placed in four possible (Alt) modes of operation as outlined below. The modes are selected during command status write as follows:

PC_2	PC_1	Port C Mode
0	0	Alt 1
0	1	Alt 3
1	0	Alt 4
1	1	Alt 2

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The function of each pin of port C in the four possible modes is outlined as follows:

Pin	Alt 1	Alt 2	Alt 3(2)	Alt 4(2)
PC_0	In	Out	A INTR	A INTR
PC_1	In	Out	A BF	A BF
PC_2	In	Out	A STB	A STB
PC_3	In	Out	Out	B INTR
PC_4	In	Out	Out	B BF
PC_5	In	Out	Out	B STB

Note:

(1) PB/PA sets port B/A mode: 0 = input; 1 = output

(2) In Alt 3 and Alt 4 modes, the control signals are initialized as follows:

Control	Input	Output
STB (Input strobe)	Input control	Output control
INTR (Interrupt request)	Low	High
BF (Buffer full)	Low	Low

Table 2. Command Status Read

	TI	INTE B	B BF	INTR B	INTE A	A BF	INTR A

where:

TI = Indicates a timer interrupt. This bit is set when terminal count is reached. It is reset when starting a new count, or a hardware reset occurs, or after reading the CS register.

INTE B/A = Port B/A interrupt. High = active.

B/A BF = Indicates whether port B/A is full if in input mode or empty if in output mode. High = active.

INTR B/A = Port B/A interrupt request. High = active.

The programming address summary for the status, ports, and timer are as follows:

I/O Address	Number of Bits	Function
XXXXX000	8	Command status
XXXXX001	8	PA
XXXXX010	8	PB
XXXXX011	6	PC
XXXXX100	8	Timer low
XXXXX101	8	Timer high

Timer Operation

The internal timer is a 14-bit binary down counter capable of operating in 4 output modes which are programmable at any time during operation. Any TTL clock meeting timer in requirements (see AC Characteristics) may be used as a time base and fed to the timer input. The timer output may be looped around and cause an interrupt or may be used as I/O control. The output modes are defined in table 3 and programmed as the two MSBs of the higher order byte of the timer count register.

Table 3. Timer Output Modes

M_2	M_1	Operation
0	0	Single square wave cycle from start to terminal count
0	1	Continuous square wave (period = count length)
1	0	Single pulse at terminal count
1	1	Continuous single pulse occurring at terminal count

Programming the timer requries two words to be written to the μPD8155/56 at I/O address XXXXX100 and XXXXX101 for the low and high order bytes, respectively. Valid count length must be between 0002H and 3FFFH. The bit assignments for the high and low programming words of the timer count register are as follows:

Word	*Timer Count Register*								*I/O Address*
High byte	M_2	M_1	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	XXXXX101
Low byte	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0	XXXXX100

The control of the timer is performed by TM2 and TM1 of the command status word.

Note that counting will be stopped by a hardware reset. A start command must be issued via the command status register to begin counting. A new mode and/or count length can be loaded while the counter is counting, but will not be used until a start command is issued.

When an external nonsynchronous event is used as the timer input, the signal must first be synchronized to the system clock. A D-type flip-flop can be used for this purpose.