

Description

The NEC μ PD8253 contains three independent, programmable, multi-model 16-bit counter/timers. It is designed as a general purpose device, fully compatible with the 8080 family. The μ PD8253 interfaces directly to the buses of the processor as an array of I/O ports.

The μ PD8253 can generate accurate time delays under the control of system software. The three independent 16-bit counters can be clocked at rates from DC to 5 MHz. The system software controls the loading and starting of the counters to provide accurate multiple time delays. The counter output flags the processor at the completion of the time-out cycles.

System overhead is greatly improved by relieving the software from the maintenance of timing loops. Some other common uses for the μ PD8253 in microprocessor based systems are:

- Programmable baud rate generator
- Event counter
- Binary rate multiplier
- Real time clock
- Digital one-shot
- Complex motor controller

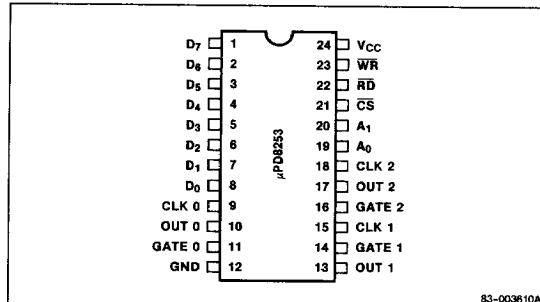
Features

- ☐ Three independent 16-bit counters
- ☐ Clock rate: DC to 5 MHz
- ☐ Binary count or BCD
- ☐ Single +5 V power supply, $\pm 10\%$

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μ PD8253C-2	24-pin plastic DIP	5 MHz
μ PD8253C-5	24-pin plastic DIP	4 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1-8	D ₇ -D ₀	Three-state data bus
9,15,18	CLK 0,1,2	Counter clock inputs 0-2
10,13,17	OUT 0,1,2	Counter outputs 0-2
11,14,16	GATE 0,1,2	Counter gate inputs 0-2
12	GND	Ground
19,20	A ₀ ,A ₁	Counter select
21	$\overline{CS}$	Chip select
22	$\overline{RD}$	Read counter
23	$\overline{WR}$	Write command or data
24	V _{CC}	+5 V power supply

Pin Functions

D₇-D₀ (Data Bus)

These pins form a three-state, bidirectional data bus that interfaces with the 8080AF/8085 microprocessor system.

CLK 0,1,2 (Counter Clock Inputs 0-2)

CLK 0, CLK 1, and CLK 2 input the clock signal for counter 0, counter 1, and counter 2, respectively.

OUT 0,1,2 (Counter Outputs 0-2)

OUT 1, OUT 2, and OUT 3 are outputs signals for counter 0, counter 1, and counter 2, respectively.

GATE 0,1,2 (Counter Gate Inputs 0-2)

The GATE 0, GATE 1, and GATE 2 inputs gate counter 0, counter 1, and counter 2, respectively.

GND (Ground)

Connection to ground.

A₀, A₁ (Counter Select)

These inputs are normally connected to the processor's address bus. Their function is to select which of the three counters will be operated on, and to address the control word register for mode selection.

$\overline{\text{CS}}$ (Chip Select)

A low level input to this pin enables the μ PD8253. Reading and writing will not occur unless the device is selected. This input has no effect on the actual operation of the counters.

$\overline{\text{RD}}$ (Read Counter)

A low level input to this pin instructs the μ PD8253 to send the selected counter value to the processor.

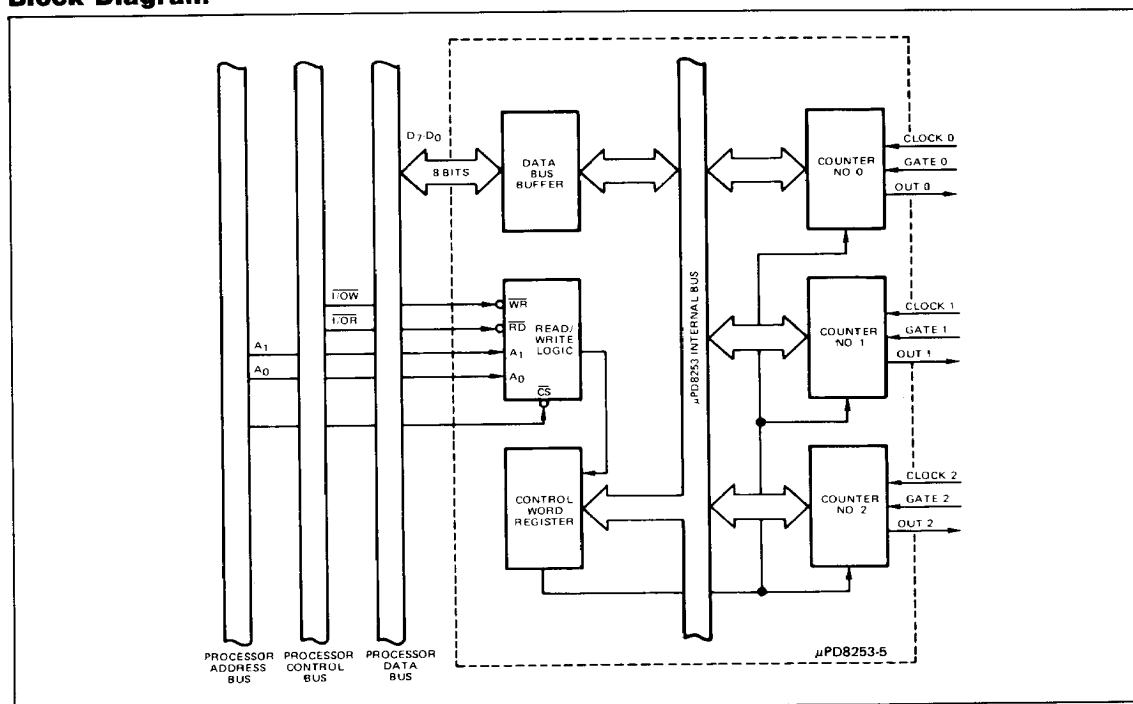
$\overline{\text{WR}}$ (Write Command or Data)

A low level input to this pin instructs the μ PD8253 to receive mode information or counter input data from the processor.

V_{cc}

+5 V power supply.

Block Diagram



Functional Description

The three-state, bidirectional data bus buffer interfaces the μPD8253 to the 8080AF/8085A micro-processor system. Data transfer is according to the input or output instructions executed by the processor. The data bus buffer has three basic functions:

- Programming the μPD8253 modes
- Loading the count registers
- Reading the count values

The read/write logic controls the overall operation of the μPD8253 and is governed by inputs received from the processor system bus.

When A₀ and A₁ are high level, data from the data bus buffer is stored in the control word register. This data controls the operational mode of the counters, the selection of BCD or binary counting, and the loading of the count registers.

Counters 0, 1, and 2 are identical 16-bit down counters that are functionally independent, allowing for separate mode configurations and counting operations. Each counter can operate in either binary or BCD. Gate, input, and output line configurations are determined by the operational mode data stored in the control word register. System software overhead can be reduced by allowing the control word to govern the loading of the count data.

It is possible to read the contents of a counter when it is operating, without disturbing its operation. The following table shows how the counters are manipulated by input signals to the read/write logic.

CS	RD	WR	A ₁	A ₀	Function
0	1	0	0	0	Load counter no. 0
0	1	0	0	1	Load counter no. 1
0	1	0	1	0	Load counter no. 2
0	1	0	1	1	Write mode word
0	0	1	0	0	Read counter no. 0
0	0	1	0	1	Read counter no. 1
0	0	1	1	0	Read counter no. 2
0	0	1	1	1	No-operation, 3-state
1	X	X	X	X	Disable, 3-state
0	1	1	X	X	No-operation, 3-state

Absolute Maximum Ratings

Operating temperature	0°C to +70°C
Storage temperature	−65°C to +150°C
Voltage on any pin	−0.5 to +7 volts (1)

Note:

(1) With respect to ground.

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C; V_{CC} = GND = 0 V

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input capacitance	C _{IN}		10		pF	f _c = 1 MHz
Input/Output capacitance	C _{I/O}		20		pF	Unmeasured pins returned to V _{SS}

DC Characteristics

T_A = 0°C to +70°C; V_{CC} = +5 V ± 10%

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input low voltage	V _{IL}	−0.5		0.8	V	
Input high voltage	V _{IH} (1)	2.0		V _{CC} + 0.5	V	
Output low voltage	V _{OL}			0.45	V	I _{OL} = 2.2 mA
Output high voltage	V _{OH}	2.4			V	I _{OH} = −400 μA
Input load current	I _{IL}			±10	μA	0 ≤ V _{IN} ≤ V _{CC}
Output float leakage current	I _{OFL}			±10	μA	0.45 ≤ V _{OUT} ≤ V _{CC}
V _{CC} supply current	I _{CC}			140	mA	

Note:

(1) V_{IH} 2.2 min for μPD8253-2.

AC Characteristics

T_A = 0°C to +70°C; V_{CC} = +5 V ±10%; GND = 0 V

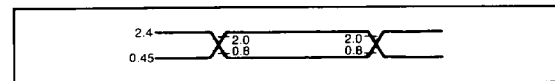
Parameter	Symbol	Limits μPD8253-2		Limits μPD8253-5		Unit	Test Conditions
		Min	Max	Min	Max		
Read							
Address stable before READ	t _{AR}	30		0		ns	
Address hold time for READ	t _{RA}	0		0		ns	
READ pulse width	t _{RR}	200		250		ns	
Data delay from READ	t _{RD}		140		170	ns	C _L = 150 pF
READ to data floating	t _{DF}	10	85	25	100	ns	C _L = 150 pF
Recovery time between READS	t _{RV}	200		1000		ns	
Write							
Address stable before WRITE	t _{AW}	0		0		ns	
Address hold time for WRITE	t _{WA}	0		0		ns	
WRITE pulse width	t _{WW}	160		250		ns	
Data set up time for WRITE	t _{DW}	130		150		ns	
Data hold time for WRITE	t _{WD}	0		0		ns	
Recovery time between WRITES	t _{RV}	200		1000		ns	
Clock and Gate Timing							
Clock period	t _{CLK}	200		250	DC	ns	
High pulse width	t _{PWH}	80		160		ns	
Low pulse width	t _{PWL}	80		90		ns	
Gate pulse width high	t _{GW}	120		150		ns	
Gate set up time to clock ↑	t _{GS}	70		100		ns	
Gate hold time after clock ↑	t _{GH}	50		50		ns	
Low gate width	t _{GL}	120		100		ns	
Output delay from Clock ↓	t _{OD}		250		300	ns	C _L = 150 pF
Output delay from gate	t _{ODG}		250		300	ns	C _L = 150 pF

Note:

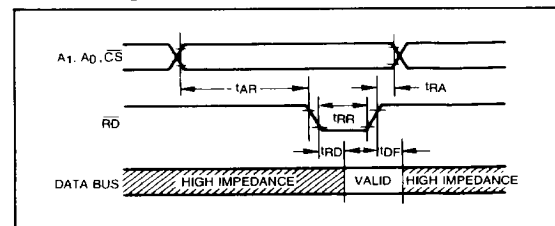
(1) AC timing measured at V_{OH} = 2.0 V; V_{OL} = 0.8 V.

Timing Waveforms

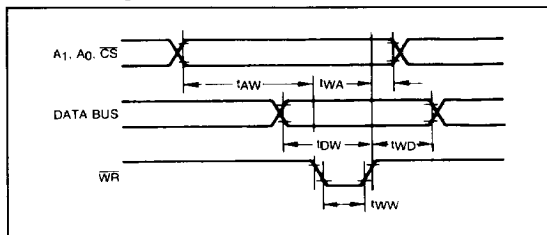
AC Test Conditions



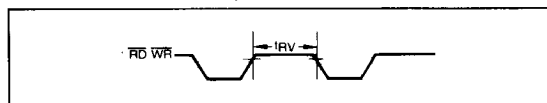
Read Timing



Write Timing

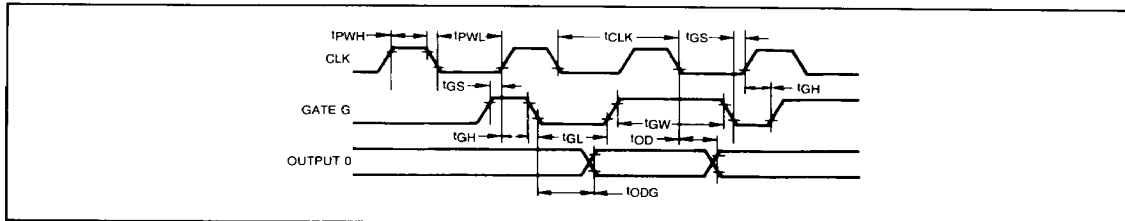


Read and Write Timing



Timing Waveforms (cont)

Clock and Gate Timing



Programming the μPD8253

The programmer can select any of the six operational MODES for the counters using system software. Individual counter programming is accomplished by loading the CONTROL WORD REGISTER with the appropriate control word data ($A_0, A_1 = 11$).

Control Word Format

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
SC ₁	SC ₀	RL ₁	RL ₀	M ₂	M ₁	M ₀	BCD

RL — Read/Load

RL ₁	RL ₀	
0	0	Counter latching operation
1	0	Read/Load most significant byte only
0	1	Read/Load least significant byte only
1	1	Read/Load least significant byte first, then most significant byte

SC — Select Counter

SC ₁	SC ₀	
0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2
1	1	Invalid

BCD

0	Binary counter, 16-bits
1	BCD counter, 4-decades

M-Mode

M ₂	M ₁	M ₀	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

Operational Modes

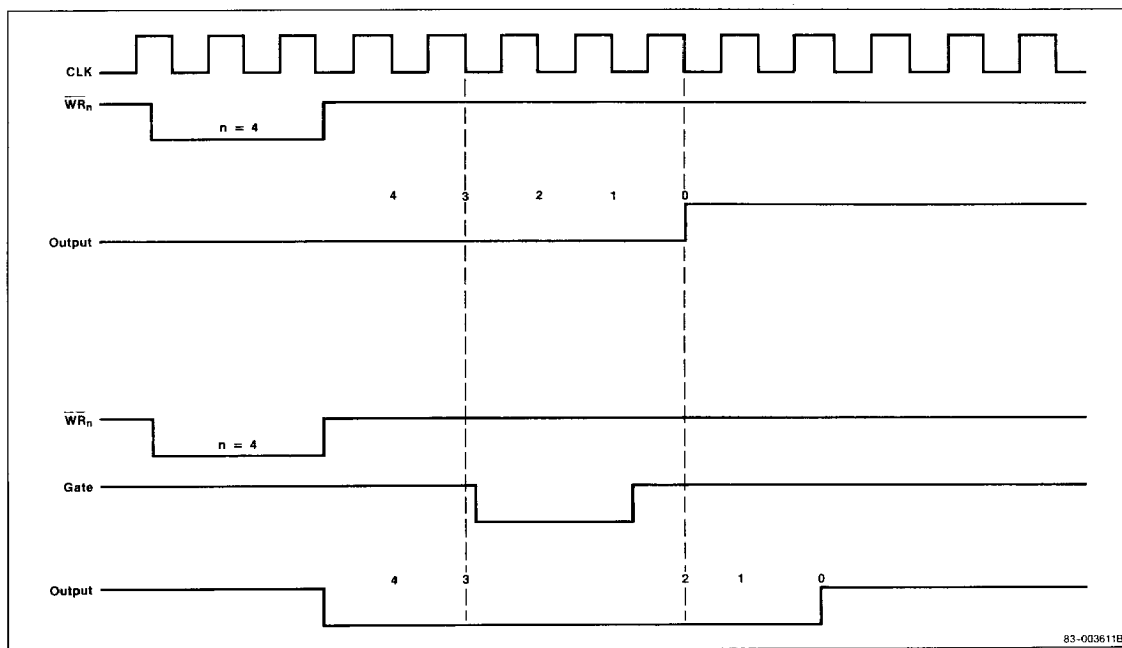
Each of the three counters can be individually programmed with different operating MODES by appropriately formatted control words. The following is a summary of the MODE operations.

Mode 0: Interrupt on Terminal Count

The initial MODE set operation forces the OUTPUT low. When the specified counter is loaded with the count value, it will begin counting. The OUTPUT will

remain low until the terminal count sets it high. It will remain in the high state until the trailing edge of the second WR pulse loads in COUNT data. If data is loaded during the counting process, the first WR stops the count. Counting starts with the new count data triggered by the falling clock edge after the second WR. If a GATE pulse is asserted while counting, the count is terminated for the duration of GATE. The falling edge of CLK following the removal of GATE restarts counting from the terminated point.

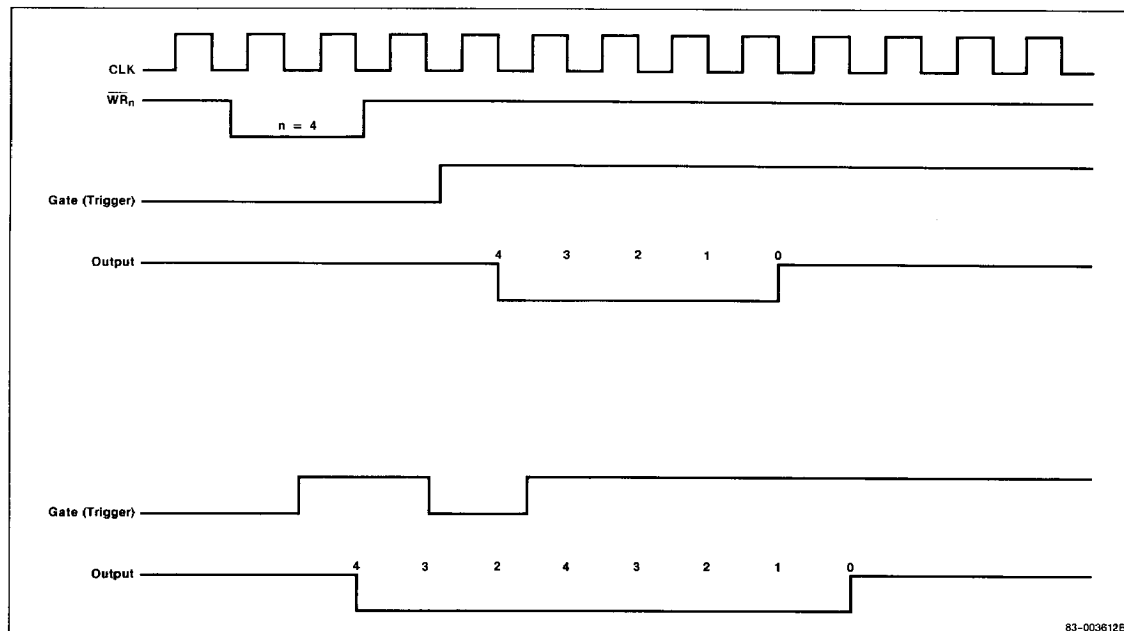
Mode 0: Interrupt on Terminal Count



Mode 1: Programmable One-Shot

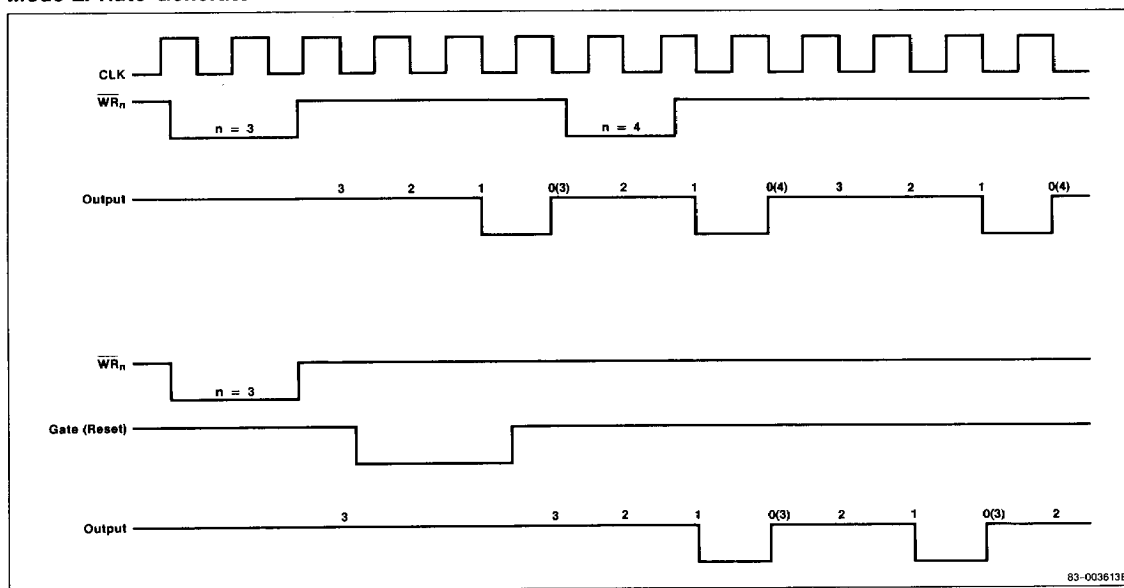
The OUTPUT is set low by the falling edge of CLOCK following the trailing edge of GATE. The OUTPUT is set high again at the terminal count. The output pulse is not affected if new count data is loaded while the OUTPUT is low. The new data will be loaded on the rising edge of the next trigger pulse. The assertion of a trigger pulse while OUTPUT is low, resets and retriggeres the one-shot. The OUTPUT will remain low for the full count value after the rising edge of TRIGGER.

Mode 1: Programmable One-Shot



Mode 2: Rate Generator

The RATE GENERATOR is a variable modulus counter. The OUTPUT goes low for one full CLOCK period as shown in the following timing diagram. The count data sets the time between OUTPUT pulses. If the count register is reloaded between output pulses the present period will not be affected. The subsequent period will reflect the new value. The OUTPUT will remain high for the duration of the asserted GATE input. Normal operation resumes on the falling CLOCK edge following the rising edge of GATE.

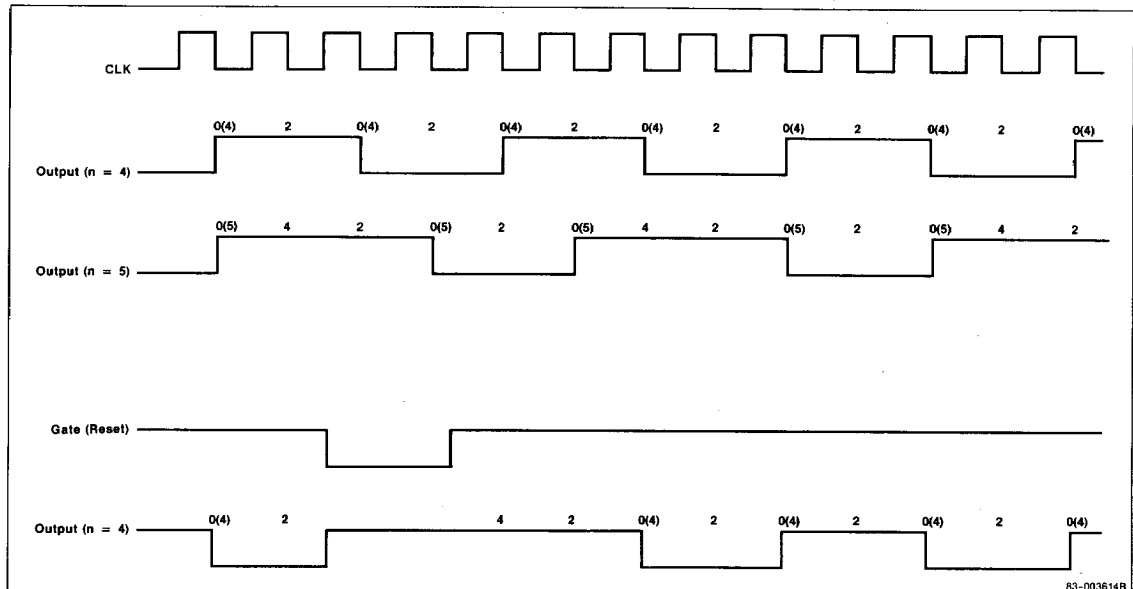
Mode 2: Rate Generator

Mode 3: Square Wave Generator

MODE 3 resembles MODE 2 except the OUTPUT will be high for half of the count and low for the other half (for even values of data). For odd values of count data the OUTPUT will be high one clock cycle longer than when it is low (High Period $\rightarrow \frac{N+1}{2}$ clock cycles; Low Period $\rightarrow \frac{N-1}{2}$ clock periods, where N is the decimal value of count data). If the count register is reloaded with a new value during counting, the new value will be reflected immediately after the output transition of the current count.

The OUTPUT will be held in the high state while GATE is asserted. Counting will start from the full count data after the GATE has been removed.

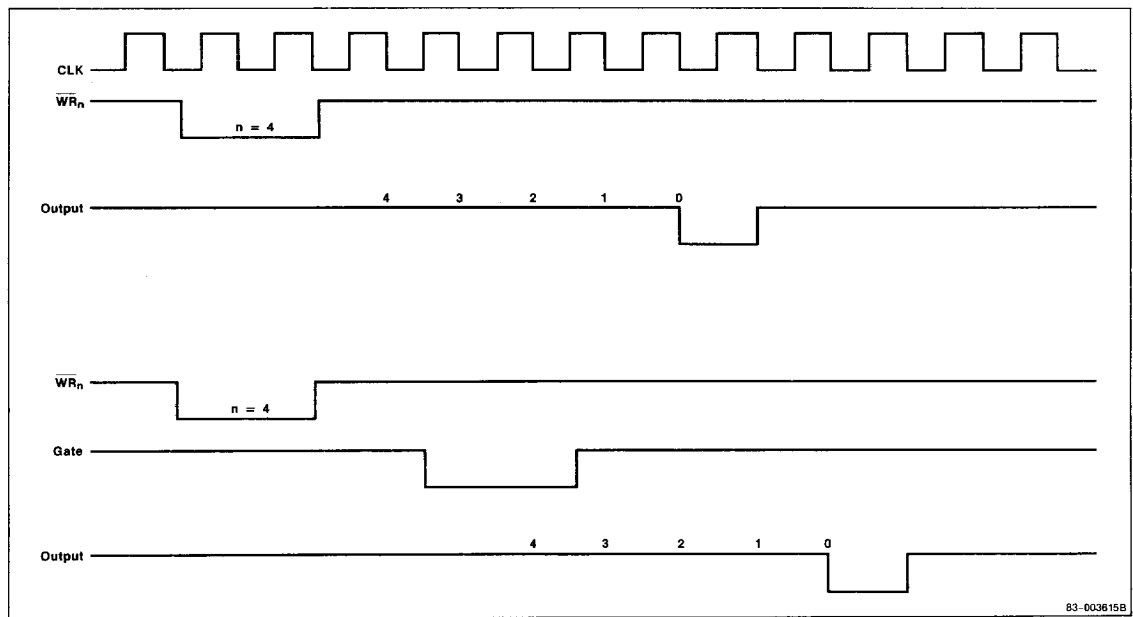
Mode 3: Square Wave Generator



Mode 4: Software Triggered Strobe

The OUTPUT goes high when MODE 4 is set, and counting begins after the second byte of data has been loaded. When the terminal count is reached, the OUTPUT will pulse low for one clock period. Changes in count data are reflected in the OUTPUT as soon as the new data has been loaded into the count registers. During the loading of new data, the OUTPUT is held high and counting is inhibited.

The OUTPUT is held high for the duration of GATE. The counters are reset and counting begins from the full data value after GATE is removed.

Mode 4: Software Triggered Strobe

Mode 5: Hardware Triggered Strobe

Loading MODE 5 sets OUTPUT high. Counting begins when count data is loaded and GATE goes high. After terminal count is reached, the OUTPUT will pulse low for one clock period. Subsequent trigger pulses will restart the counting sequence with the OUTPUT pulsing low on terminal count following the last rising edge of the trigger input. (Reference the bottom half of the timing diagram.)

Mode 5: Hardware Triggered Strobe

