WESTERN DIGITAL
CORPORATION

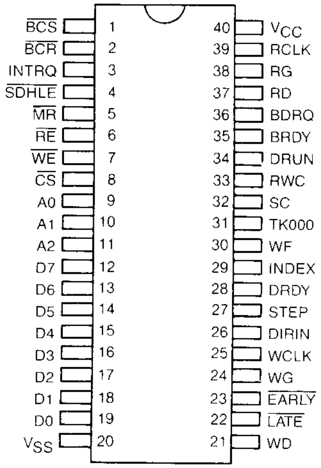
PRELIMINARY

WD2010-05 Winchester Disk Controller

WD2010-05

FEATURES

- COMPATIBLE WITH MOST MICROPROCESSORS VIA AN 8 BIT DATA BUS
- DATA RATE OF 5 MBS
- MULTIPLE SECTOR READ AND WRITE COMMANDS
- FORMATTING AND SECTOR INTERLEAVE CAPABILITY
- SEEK COMBINED WITH READ AND WRITE COMMANDS
- SINGLE OR MULTIPLE SECTOR BUFFER USING FIFO OR RAM/COUNTER
- BUFFER ACCESS VIA PROGRAMMED I/O OR DMA
- 32 BIT ECC OR 16 BIT CRC SELECTED BY SOFTWARE
- SECTOR LENGTH OF 128, 256, 512, 1024 BYTES SELECTED BY SOFTWARE
- PROGRAMMABLE RETRY ALGORITHM
- CAPABLE OF CORRECTING ERRORS WHEN A SECTOR BUFFER IS USED
- 5 OR 11 BIT CORRECTION SPAN SELECTED BY PROGRAM



$\overline{\text{BCS}}$ 1 40 V_{CC}
$\overline{\text{BCR}}$ 2 39 RCLK
INTRQ 3 38 RG
$\overline{\text{SDHLE}}$ 4 37 RD
$\overline{\text{MR}}$ 5 36 BDRQ
$\overline{\text{RE}}$ 6 35 BRDY
$\overline{\text{WE}}$ 7 34 DRUN
$\overline{\text{CS}}$ 8 33 RWC
A0 9 32 SC
A1 10 31 TK000
A2 11 30 WF
D7 12 29 INDEX
D6 13 28 DRDY
D5 14 27 STEP
D4 15 26 DIRIN
D3 16 25 WCLK
D2 17 24 WG
D1 18 23 $\overline{\text{EARLY}}$
D0 19 22 $\overline{\text{LATE}}$
V_{SS} 20 21 WD

PIN DESIGNATION

DESCRIPTION

The WD2010 Winchester Disk Controller is a single chip device designed for use with the Shugart Associates SA1000 and Seagate Technology ST506 8″ and 5.25″ disk drives. The WD2010-05 is software compatible with the WD1010-05 and reads or writes at a rate of 5 Mbits.

The WD2010 operates with an external buffer such as WD1510 128X9 FIFO memory or a combination of a 256X8 static RAM and an 8-bit resettable counter, or a DMA controller. Data bytes are transferred to and from the buffer every 1.6 μsec. Transfers from the buffer to the CPU are made via programmed I/O or DMA.

The WD2010 generates counter control signals to minimize external gating, and hand shake signals to control DMA operation for multiple sector transfers.

A 32-bit ECC (Error Correction Code) polynomial or a 16-bit CRC are selectable.

The WD2010 has three possible alternatives in handling an error during a Read operation:

A. It may be directed to correct the data in the Sector Buffer automatically, providing the Host with good data.

B. Supply the Host with the error location and pattern, allowing the Host to correct the error.

C. Take no action other than setting the error flag and letting the Host do the entire error correction process.

The WD2010 is a TTL compatible 40 pin DIP NMOS device requiring a single +5V supply.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	$\overline{\text{BCS}}$	$\overline{\text{BUFFER}}$ $\overline{\text{CHIP}}$ SELECT	O	When asserted, it enables reading or writing the external Sector Buffer, as well as controlling bus switching.
2	$\overline{\text{BCR}}$	$\overline{\text{BUFFER}}$ COUNTER $\overline{\text{RESET}}$	O	$\overline{\text{BCR}}$ is asserted prior to read and write functions and at the completion of a command. $\overline{\text{BCR}}$ is not used if the Sector Buffer is a FIFO.
3	INTRQ	INTERRUPT REQUEST	O	INTRQ is asserted upon completion of a command and remains that way until the Status Register is read, or a new command is written into the Command Register. This signal may be programmed by a Read Command to occur with BDRQ and DRQ.
4	$\overline{\text{SDHLE}}$	$\overline{\text{SDH}}$ $\overline{\text{LATCH}}$ $\overline{\text{ENABLE}}$	O	$\overline{\text{SDHLE}}$ is asserted when the $\overline{\text{SDH}}$ Register is to be written into by the Host. (See Figure 3.)
5	$\overline{\text{MR}}$	$\overline{\text{MASTER RESET}}$	I	When asserted, $\overline{\text{MR}}$ initializes all internal logic except the Task File.
6	$\overline{\text{RE}}$	$\overline{\text{READ}}$ $\overline{\text{ENABLE}}$	I/O	Tri-state, bi-directional signal. $\overline{\text{RE}}$ is an input when reading the Task File, and an output when reading the Sector Buffer.
7	$\overline{\text{WE}}$	$\overline{\text{WRITE}}$ $\overline{\text{ENABLE}}$	I/O	Tri-state, bi-directional signal. Used as an input when writing to the WD2010 Task File. Used as an output when the WD2010 is writing to the Sector Buffer.
8	$\overline{\text{CS}}$	$\overline{\text{CHIP}}$ $\overline{\text{SELECT}}$	I	$\overline{\text{CS}}$ must be asserted to read from or write to the WD2010 Task File.
9 thru 11	A0 thru A2	ADDRESS 0 thru ADDRESS 2	I	Provide the address of the register within the Task File that is to transmit or receive on the data bus.
12 thru 19	D7 thru D0	DATA 7 thru DATA 0	I/O	8-bit, tri-state, bi-directional bus used for the transfer of commands, status, and data.
20	V_{SS}	GROUND		Ground
21	WD	WRITE DATA	O	WD is the MFM data to be written to the disk. The frequency is controlled internally by WCLK and should be stabilized further externally by a D flip flop clocked at twice the WCLK frequency. The output has an active pullup and pulldown that can sink 6.0ma.
22	$\overline{\text{LATE}}$	$\overline{\text{LATE}}$	O	This signal is used in the Write Precompensation circuitry along with $\overline{\text{EARLY}}$ to control the delay of WD.
23	$\overline{\text{EARLY}}$	$\overline{\text{EARLY}}$	O	This signal is used in the Write Precompensation circuitry along with $\overline{\text{LATE}}$ to control the delay of WD.
24	WG	WRITE GATE	O	WG is asserted when valid data is to be written. It enables write current to the head and is immediately de-asserted if a Write Fault (WF) is detected.
25	WCLK	WRITE CLOCK	I	A 5 MHz clock used internally to control WD.

PIN DESCRIPTION (Continued)

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
26	DIRIN	DIRECTION IN	O	This signal determines the direction of the read/write heads when stepped. Asserted moves them in; de-asserted, out.
27	STEP	STEP PULSE	O	This signal is used for pulsing the stepping motor. (See Stepping Rate Description.)
28	DRDY	DRIVE READY	I	DRDY must be asserted to execute any drive related commands.
29	INDEX	INDEX PULSE	I	The leading edge of this signal indicates that the index mark has been detected.
30	WF	WRITE FAULT	I	When asserted, indicates a write error at the drive. This halts all write, read, and stepping commands.
31	TK000	TRACK 000	I	This signal is asserted when the read/write heads are positioned over track 0 (cyl. 000). It is used to verify proper completion of a restore command.
32	SC	SEEK COMPLETE	I	The leading edge of SC indicates that the drive has settled down after stepping. It is static tested if the rising edge has not been received within 10 revolutions after the stepping pulses.
33	RWC	REDUCE WRITE CURRENT	O	RWC can be programmed to reduce the write current starting at a selected cylinder. (See Write Precomp Cylinder Register.)
34	DRUN	DATA RUN	I	DRUN informs the WD2010 when a field of all ones or zeros has been detected. (See Drive Interface.)
35	BRDY	BUFFER READY	I	When asserted, the Sector Buffer is full or empty.
36	BDRQ	BUFFER DATA REQUEST	O	BDRQ represents the same state as DRQ (bit 3 of the Status Register). This signal is asserted when the Sector Buffer is to be read from or written to by the Host. BDRQ can be used for DMA or Programmed I/O. If DRQ is used it must be polled by the Host during Programmed I/O.
37	RD	READ DATA	I	MFM data and clocks are received from the drive. The clocks and data are separated internally.
38	RG	READ GATE	O	RG is asserted when a search for an address mark is initiated. It remains asserted until the end of the ID or data field. (See Drive Interface.)
39	RCLK	READ CLOCK	I	This clock is generated by a VCO, phase locked to data read from the disk.
40	V_{CC}	+5V		+5 Volts

ARCHITECTURE

The WD2010 provides the necessary interface control between the Host processor and a 5.25″ or 8″ Winchester disk drive. The controller is made up of seven major building blocks connected to the processor via a Host interface on one side and a drive interface on the other. Figure 1 illustrates the major sections and how they relate to each other.

The WD2010 timing is controlled by two clock input signals, RCLK and WCLK. RCLK is used for MFM decoding and is a 5 Mbit/sec data rate. WCLK is used for MFM encoding at the same rate as reading, PLA Controller, Host Interface, and Buffer Control.

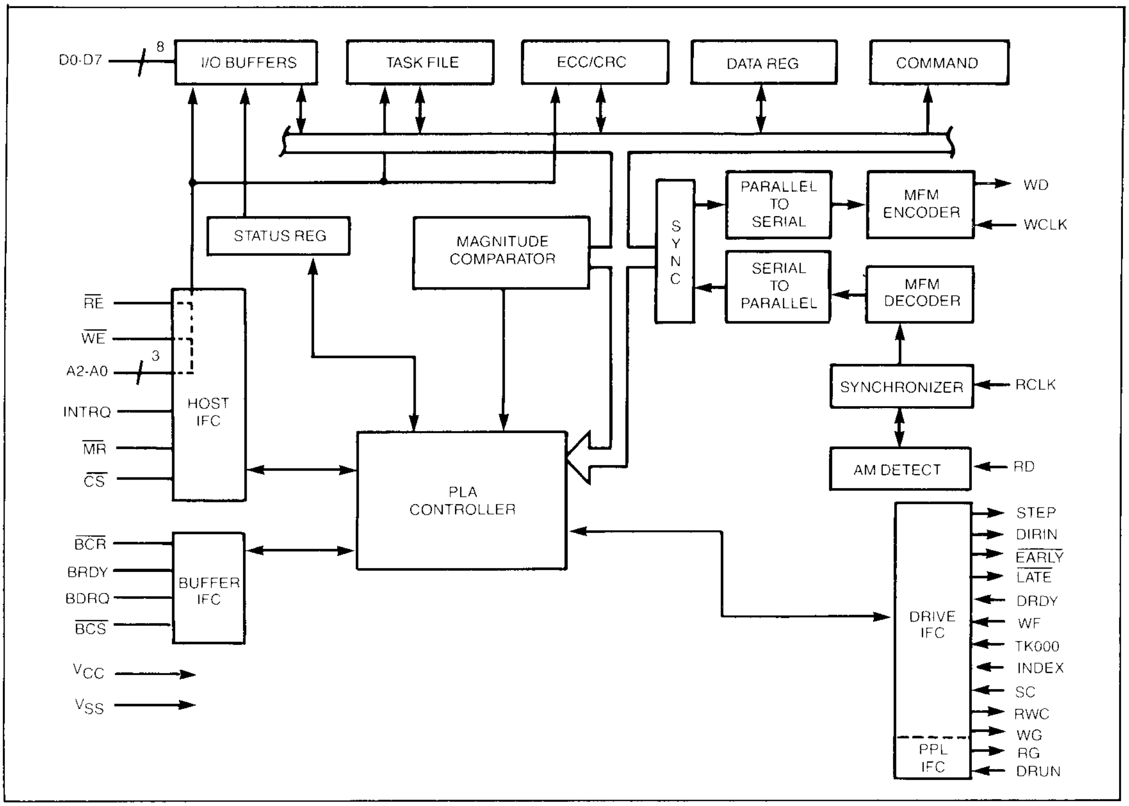


FIGURE 1. WD2010 BLOCK DIAGRAM

Programmable Logic Array (PLA) Controller

The Command Register, is the last of the Task File Registers to be written into, and starts the PLA control. The PLA controller, synchronized by WCLK, interprets the command, generates control signals, and operates in a hand shake mode when communicating with the MFM encoding block.

Magnitude Comparator

The magnitude (number of steps) and direction required to move the heads from their present cylinder to their desired cylinder is performed by an 11-bit comparator. It compares the cylinder number recorded in the Task File (it's desired location) with the Present Cylinder Position Register recorded internally. From this, the direction and number of steps that must be performed to place the head on the desired track is calculated.

A separate high speed equivalence comparator is used to compare ID field bytes when searching for a sector ID field.

CRC and ECC Generator and Checker.

The CRC mode of the operation, defined by the SDH (Sector Size, Head, drive select) Register (Bit 7 = 0), provides a means of verifying the accuracy of the data read from the disk but does not attempt to correct it.

The CRC generator computes and checks cyclic redundancy check characters that are to be written to, and read from the disk following the ID and data fields. The polynomial used is $X^{16} + X^{12} + X^5 + 1$. The CRC Register is preset to all one's before computation starts.

The ID field always has a 2-byte CRC character appended to it, while the data field may have either a 2-byte CRC (SDH 7 = 0) or a 4-byte ECC character (SDH 7 = 1).

If the CRC character being generated while reading the data does not equal the one previously written, an error exists. If there is a CRC failure in the ID field, an ID not found is indicated by bit 4 of the Error Register being set. If the failure is in the data field, bit 6 of the Error Register is set.

The ECC mode of operation (SDH 7 = 1) is only applicable to the data field. This feature built into the WD2010 provides the user with the ability to detect and correct errors in the data field automatically.

A summary of the parameters to be considered when ECC is desired are:

1. SDH Register bit 7.
2. Read Command bit 0 (T).
3. Read and Write Command bit 1 (L).

4. Compute Correction Command.
5. Set Parameter Command.
6. Error correction successful, bit 2 of the Status Register.
7. Error occurred, bit 0 of the Status Register.
8. Uncorrectable error, bit 6 of the Error Register.

The SDH register bit 7 must be equal to one to change from the CRC mode to the ECC mode.

The T bit (bit 0) within the Read Command controls whether or not error correction is to be attempted.

When T = 0 and an error is detected, the WD2010 tries up to 10 times to correct the error. If successful, bit 2 of the Status Register is set. The Host can interrogate the Status Register and detect that a problem does exist, but was corrected. If the error is not correctable, bit 6 of the Error Register is set. The Host can read the data, even though errors do exist.

When T = 1, and an error is detected, no attempt is made to correct it and bit 0 of the Status Register and bit 6 of the Error Register is set. The user now has two choices:

1. Ignore the error and make no attempt to correct it.
2. Use the Compute Correction Command to determine the pattern and location of the error, and correct it within the user's program.

When the Compute Correction Command is implemented, it should be done before executing any command that can alter the content of the ECC Register. The Read, Write, Scan, and Format commands alter the syndrome and correction is impossible. The Compute Correction Command determines that the error is uncorrectable, at which point the error bits in the Status Register and Error Register are set.

Although ECC generation starts with the first bit of the F8 byte in the data ID field, the actual ECC bytes produced for the sector are the same as if the A1 byte was included.

The ECC polynomial used is,

$$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^{6} + X^{2} + 1.$$

For auto correction the external data buffer must be implemented with a static RAM and counter, not a FIFO memory.

The Set Parameter Command is used to select a 5 or 11-bit correction span.

Read and Write Commands, with the L bit (bit 1) equal to one, are referred to as Readlong and Writelong Commands. With these commands, no ECC or CRC characters are generated or checked by the WD2010. In effect, the 4 ECC bytes are handled as an additional 4 bytes of data which pass through the data buffer.

With proper use of the Write, Readlong, Writelong, and Read commands, a diagnostic routine may be developed to test the accuracy of the error correction process.

MFM Encoding and Decoding

The MFM encoder receives its data one byte at a time from an 8-bit parallel-to-serial register, and with the frequency of WCLK, develops the MFM WD. Depending on the bit pattern of the data, $\overline{\text{EARLY}}$ or $\overline{\text{LATE}}$ may be asserted. External circuitry uses these signals to compensate for the shift caused by the influence one bit has over another. The WD2010 examines three bits, the last one written, the one being written, and the next one to be written. From this, $\overline{\text{EARLY}}$ or $\overline{\text{LATE}}$ is asserted. Since the bit leaving the WD2010 has already occurred, it is too late to make it early, therefore the external delay circuit must be as follows.

$\overline{\text{EARLY}}$ (asserted) and $\overline{\text{LATE}}$ (de-asserted) = no delay

$\overline{\text{EARLY}}$ (de-asserted) and $\overline{\text{LATE}}$ (de-asserted) = one unit delay

$\overline{\text{EARLY}}$ (de-asserted) and $\overline{\text{LATE}}$ (asserted) = two units delay

These signals are not dependent upon the Write Precomp Cylinder register (RWC). Figure 6 illustrates one method of using these signals.

The MFM decode operates from RCLK, a bit rate clock generated from the external Data Separator. RCLK and WCLK need not be synchronized.

Address Mark (AM) Detection

An address mark is comprised of two unique bytes preceding both the ID field and the data field. The first byte is used for resynchronization. The second byte indicates whether it is an ID field or a data field.

The first byte, A1 hex, normally has a clock pattern of OE hex. However, one clock pulse has been supressed, making it QA hex. With this pattern, the detector knows it is looking at an address mark. It now examines the next byte to determine if it is an ID or data field. If bits 7 thru 2 are 1111X1XX, it is an ID field (bits 3, 1, and 0 are the high order cyl. #bits). If the second byte is F8, it is a data field.

Host Interface

The primary interface between the Host processor and the WD2010 is an 8-bit bi-directional bus. This bus is used to transmit and receive data for both the WD2010 and the Sector Buffer. The Sector Buffer consists of either a FIFO memory, or a static RAM and counter. Since the WD2010 makes the bus active when accessing the Sector Buffer, a transceiver must be used to isolate the Host during this time. Figure 2 illustrates a typical interface with a Sector Buffer, implemented with a RAM memory. Whenever the WD2010 is not using the Sector Buffer, it turns control of the Sector Buffer and data bus over to the Host by de-asserting its output term, $\overline{\text{BCS}}$. This de-selects the Sector Buffer and switches the data bus transceivers.

When the Host wants to access the Sector Buffer it produces an address of zero (A0 thru A2 = 0). A decoder recognizing A0 thru A2 = 0 asserts a $\overline{\text{BCS}}$ of its own. The Host then asserts $\overline{\text{WE}}$ or $\overline{\text{RE}}$ for the counter, at the leading edge, the location within the Sector Buffer addressed by the counter is accessed, at the trailing edge the counter advances to the next count. The decoder asserts $\overline{\text{CS}}$ to the WD2010 any time the address does not equal zero (A0 thru As ≠ 0).

During Write Sector commands the Host sets up data in the Task File and issues the command. The WD2010 asserts $\overline{BCR}$ to zero the counter. It then generates a status to inform the Host it can load the Sector Buffer with the data to be written. When the counter reaches its maximum count, BRDY is asserted by the carry out of the counter, informing the WD2010 that the Sector Buffer is full. (BRDY is asserted with a rising edge and is ignored if asserted before the WD2010 asserts $\overline{BCR}$.) $\overline{BCS}$ is then asserted, disconnecting the Host through the transceivers, and $\overline{RE}$ and $\overline{WE}$ become outputs from the WD2010 to allow access to the Sector Buffer. When the WD2010 is done using the Sector Buffer, it deasserts $\overline{BCS}$ which again allows the Host to access this local bus.

The Read Sector Command operates in a similar manner, except that the Sector Buffer is loaded by the WD2010 instead of the Host.

When BDRQ is used, it can either be connected to a DMA controller or used for programmed I/O. In either case it signals that the WD2010 is ready to receive or transmit data. DRQ status bit, if used, must be polled by the Host, therefore is limited to programmed I/O.

When INTRQ is asserted, the Host is signaled that a command has terminated (either a normal termination or an aborted command). In the case of the Read Command, INTRQ can be programmed by bit 3 to be asserted upon termination as the other commands, or at the same time BDRQ is asserted. In either case, INTRQ remains asserted until the Host reads the Status Register to determine the result of the termination, or writes a new command into the Command Register.

The WD2010 asserts $\overline{SDHLE}$ to the Host whenever the SDH register is being written into. This makes it possible to store the same information in an external register for decoding. Figure 3 illustrates one method.

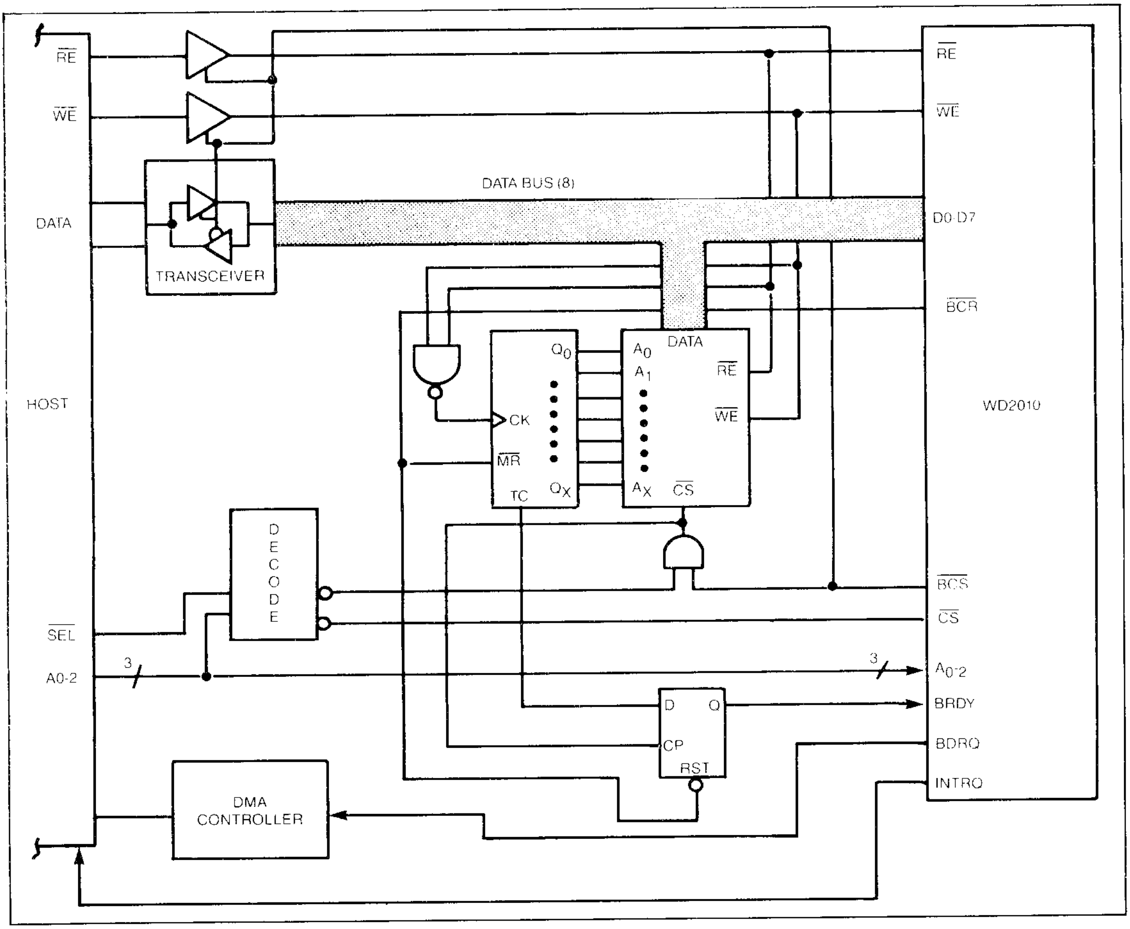


FIGURE 2. HOST INTERFACE

Drive Interface

The drive side of the WD2010 controller requires three sections of external logic. These are interface/Sector Buffers, data separator, and write precompensation. Figure 3 illustrates the drive interface.

The control lines are buffered, single-ended, and resistor terminated at TTL levels. The data lines to and from the drive also require buffering, and are terminated with RS-422 drivers. The interface specification for the drive can be found in the manufacturer's OEM manual. The WD2010 supplies TTL compatible signals, and interfaces with most driver devices.

When the SDH Register is written into, the Head and Drive select signals are latched externally by the latch enable signal $\overline{\text{SDHLE}}$. See Figure 3A, 3B.

The data recovery circuits consist of a phase lock loop, data separator, and associated components. The WD2010 interacts with the data separator through DRUN and RG. The block diagram of the data separator circuit is illustrated in Figure 4. Data read from the drive is presented to the RD input of the WD2010, the reference multiplexor, and a retirggerable one shot. The RG is de-asserted when the WD2010 is not inspecting data. The PLL at this time should remain locked to the reference clock.

When any Read or Write Command is initiated and a search for an address mark begins, DRUN is examined. The DRUN one-shot is set slightly longer than one bit time, allowing it to retrigger constantly on a field of all ones or all zeros. An internal counter times out to see that DRUN is asserted for 2 byte times. RG is asserted by the WD2010 switching the data separator to lock onto the incoming data stream. If DRUN is de-asserted prior to 7 byte times, RG is de-asserted and the process is repeated. RG remains asserted until a non-zero, non-address mark is detected. It then de-asserts RG for two byte times (to allow the PLL to lock back on the reference clock) and starts the DRUN search over again. If an address mark is detected, RG

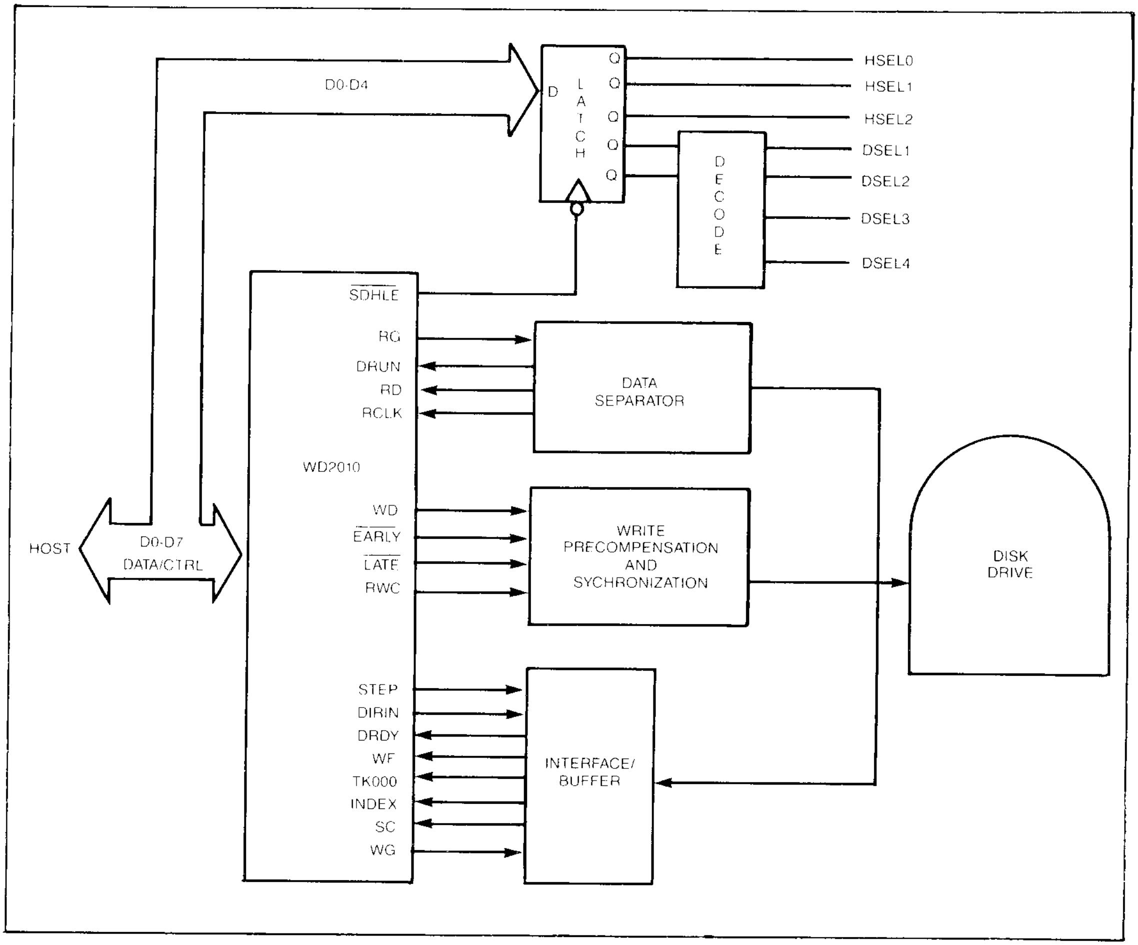


FIGURE 3A. DRIVE INTERFACE BLOCK DIAGRAM

remains asserted and the command continues searching for the proper ID field. This sequence is illustrated in Figure 5.

The Write Precompensation circuitry is designed to reduce the shift in the data caused by the effect one bit has over another. The Write precompensation logic is divided into two areas: RWC and $\overline{\text{Early}}$ or $\overline{\text{Late}}$ writing of the bits. A block diagram of the Write Precomp circuit is illustrated in Figure 6.

RWC is controlled by the Write Precomp Cylinder Register in the Task File. This register is written into by the Host. When a cylinder is called for that is equal to, or greater than the content of this register, the write current will be reduced, thus lessening the effect one bit can have over another.

Shift may also be caused by the bit pattern. With certain combinations of ones and zeros some of the bits can drift far enough apart to become difficult to read without error. This phenomenon can be minimized by using $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ as described under MFM Encoder.

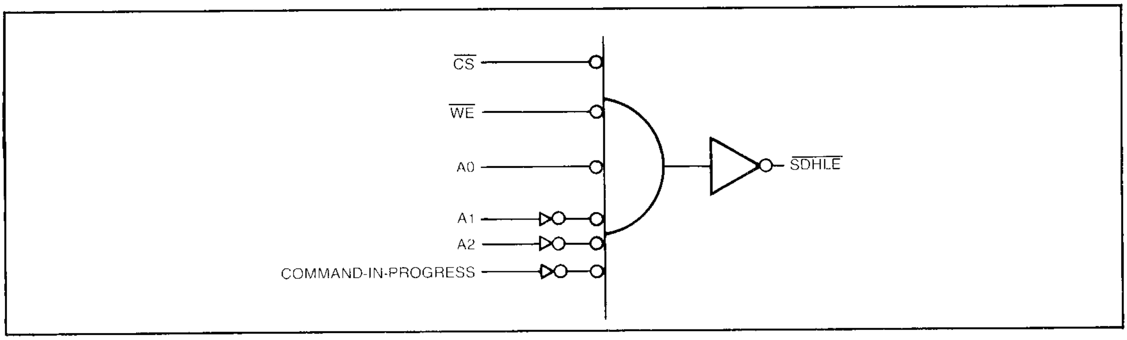


FIGURE 3B. $\overline{\text{SDHLE}}$ SIGNAL

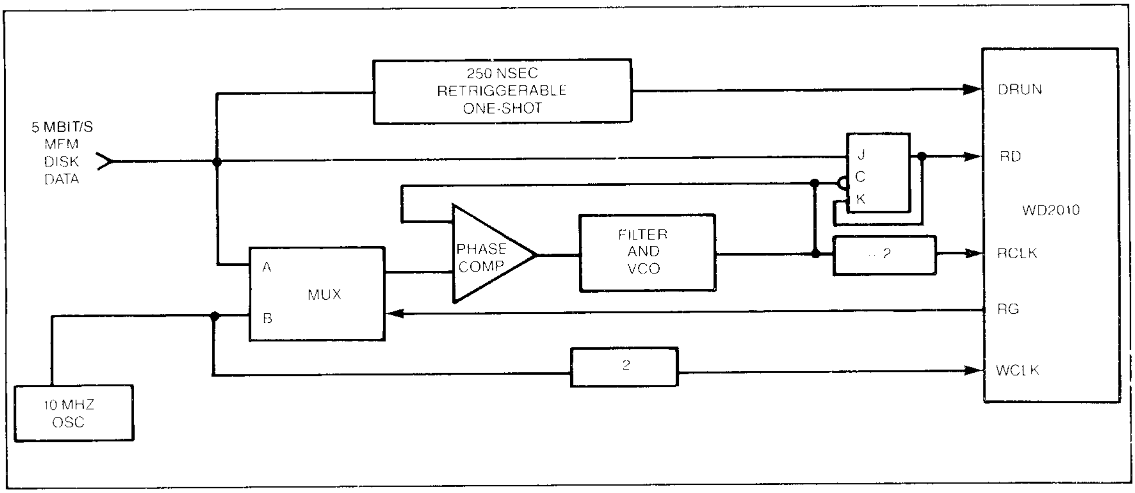


FIGURE 4. DATA SEPARATOR CIRCUIT

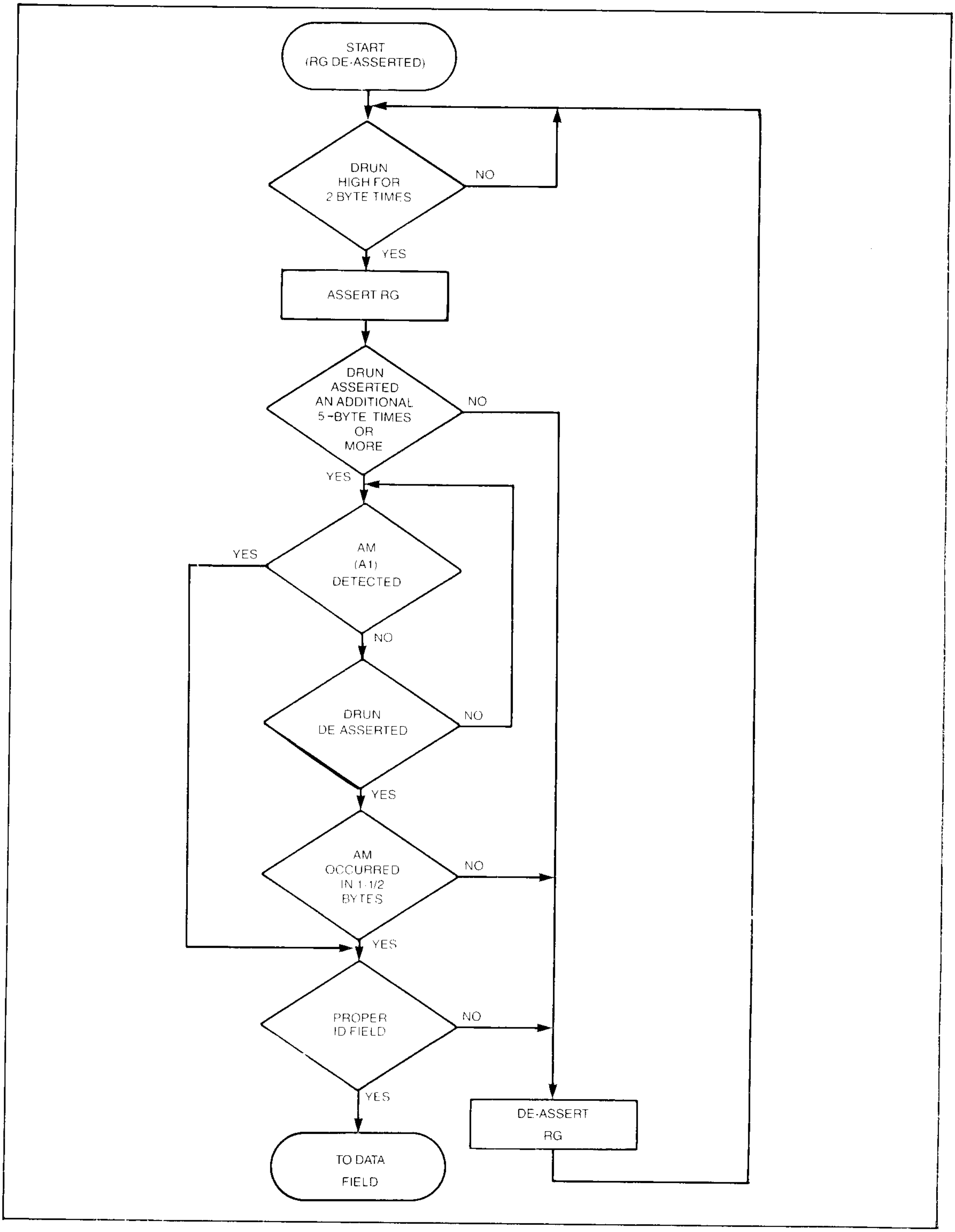


FIGURE 5. PLL CONTROL SEQUENCE FOR ID FIELD

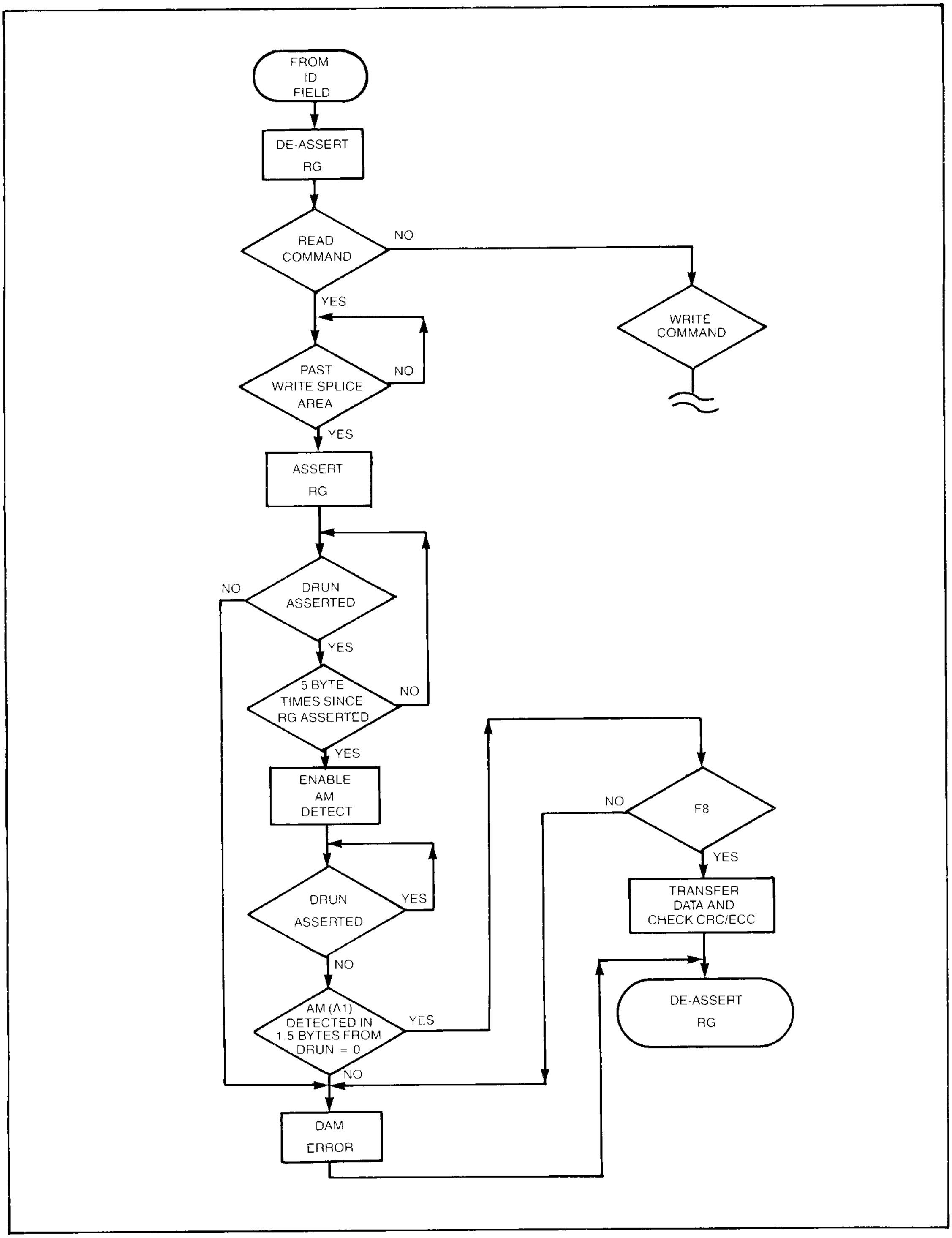


FIGURE 5A. PLL CONTROL SEQUENCE FOR DATA FIELD

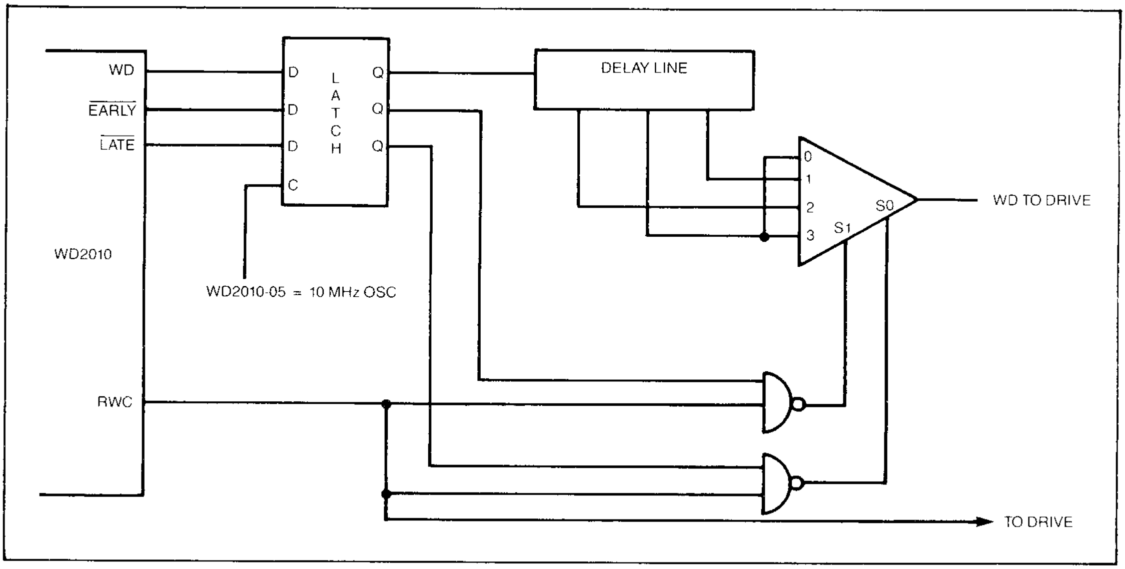


FIGURE 6. WRITE PRECOMPENSATION CIRCUIT

Task File

The Task File is a bank of nine, 8-bit registers used to hold status information indicating the success or failure of an operation, as well as the parameters under which the drive is to operate. They are addressed by the A0 through A2 lines. A0 through A2 = 0 is unused by the WD2010 and when received, puts its bus in the tri-stated condition isolating it from the bus.

ERROR REGISTER (A2 thru A0 = 1 READ)

This register contains specific error status pertaining to the completion of a command. These bits are defined as follows:

7	6	5	4	3	2	1	0
BB	CRC/ECC	0	ID	0	AC	TK	DM

Bit 7 — Bad Block Detect

This bit is set when an ID field has been encountered that contains a Bad Block Mark. It is used for bad sector mapping.

Bit 6 — CRC/ECC Data Field Error

CRC mode of operation (SDH 7 = 0): this bit is set when a CRC error occurs in the data field. When Retry is enabled, ten more attempts are made to read the sector correctly. If none of these attempts are successful, bit zero in the Status Register is set also. If one of the attempts is successful, this bit remains set to inform the Host that a marginal condition exists. However, the zero status bit is not set. No attempt is made to correct the error.

ADDRESS			TASK FILE	
A2	A1	A0	READ ONLY	WRITE ONLY
0	0	0	**BUS TRI-STATED**	
0	0	1	Error Register	Write Precomp Cylinder
0	1	0	Sector Count	
0	1	1	Sector Number	
1	0	0	Cylinder Low	
1	0	1	Cylinder High	
1	1	0	SDH Register	
1	1	1	Status Register	Command Register

NOTE: These registers are not cleared by $\overline{\text{MR}}$ being asserted.

ECC mode of operation (SDH 7 = 1). This bit is set when the first non-zero syndrome is detected. When Retry is enabled, up to ten attempts are made to correct the error. If successful, this bit remains on. However, bit 2 of the Status Register is set to inform the Host that the error has been corrected. If unsuccessful, this bit remains on and bit zero of the Status Register is set also. When Retry is disabled no attempt is made to correct the error.

The data may be read even if errors do exist.

NOTE: If the Long Mode bit is set in the Read or Write command, no error checking is performed.

Bit 5 — Reserved
Not used, forced to zero.

Bit 4 — ID Not Found
This bit is set to indicate that the correct cylinder, head, sector, or size parameter could not be found, or a CRC error occurred on the ID field. This bit is set on the first failure and remains set even if the error is recovered on a retry. When recovery is unsuccessful, the Error Status bit is set also.

For a Scan ID Command with Retry enabled (T = 0), the Error Status bit is set after ten unsuccessful attempts have been made to find the correct ID. With Retry disabled (T = 1) only two attempts are made before setting the Error Status.

For a Read and Write Command with Retry enabled (T = 0), ten attempts are made to find the correct ID field. If there is still an error on the tenth try, an auto-scan and auto-seek are performed. Then, ten more tries are made before setting the Error Status. When the Retry is disabled (T = 1) only two tries are made, and no auto-scan or auto-seek operations are performed.

Bit 3 — Reserved
Not used, forced to zero.

Bit 2 — Aborted Command
The command is aborted and this bit set if, DRDY has not been asserted, WF is asserted, or the command issued had an undefined command code.

Bit 1 — Track Zero Error
This bit is set during a Restore Command when TK000 input has not indicated that the head has reached track zero by 2047 steps.

Bit 0 — Data Address Mark Not Found
This bit is set during a Read Sector Command if the Data Address Mark is not found following the proper sector ID.

WRITE PRECOMP CYLINDER (A2 thru A0 = 1 write)

This register is used to define the cylinder number where the RWC output signal is to be asserted.

7	6	5	4	3	2	1	0
CYLINDER NUMBER ÷ 4							

The value 00-FF loaded into this register is internally multiplied by four to specify the actual cylinder where RWC is to be asserted. Thus a value of 9C hex causes the RWC to be asserted on cylinder 270 hex, 9D hex on cylinder 274 hex, etc. RWC is asserted when the present cylinder is equal to, or greater than the value of this register. For example, the ST506 requires precomp 80 hex (128 dec.) and above. Therefore, the write precomp cylinder should be loaded with 20 hex (32 dec.).

A value of FF hex causes RWC to remain de-asserted, regardless of the cylinder number values.

SECTOR COUNT (A2 thru A0 = 2)

In a multiple sector operation, this register contains the number of sectors involved with Read Sector, Write Sector, and Format commands.

7	6	5	4	3	2	1	0
NUMBER OF SECTORS							

The value written into this register is decremented by one after each sector is transferred to or from the Sector Buffer. A zero represents a 256 sector transfer, a 1 = one sector, etc. This register is disregarded when a single sector command is specified.

SECTOR NUMBER (A2 thru A0 = 3)

This register holds the number of the desired sector.

7	6	5	4	3	2	1	0
SECTOR NUMBER							

This is the starting sector in a multiple sector command. It is incremented by one after each sector has been transferred to or from the Sector Buffer. The register can contain any value from 0 to 255.

This register also specifies the minimum GAP 3 length, minus 3, during a Format Command.

CYLINDER NUMBER LOW (A2 thru A0 = 4)

This register holds the least significant 8 bits of the desired cylinder number.

7	6	5	4	3	2	1	0
LS BYTE OF CYL. NUMBER							

It is used in conjunction with the Cylinder Number High Register to specify a range of 0 to 2047.

CYLINDER NUMBER HIGH (A2 thru A0 = 5)

This register contains the three most significant bits of the desired cylinder number.

7	6	5	4	3	2	1	0
x	x	x	x	x	#	#	#

These registers determine where the R/W heads are to be positioned. The Host writes the desired cylinder number into these registers. Internal to the WD2010 is another pair of registers pointing to where the heads are presently located. When any command, other than a Restore, is executed these registers are compared. The difference between them results in DIRIN and STEP signaling the drive how many cylinders to move the heads and in which direction.

The Present Cylinder Position Register is updated to equal the Cylinder Number Register at the completion of the seek.

When a Restore Command is executed, the Present Cylinder Position Register is reset to zero, while DIRIN and STEP move the heads to track zero.

A SCAN ID Command reads the cylinder number from the track on which the heads are presently located, and writes this into the Present Cylinder Position Register.

When a different drive is selected just prior to a Read, Format, Write, or Seek command, the WD2010 issues an auto-scan ID command. This updates the Present Cylinder Position Register to reflect the position of the heads on this drive.

SDH REGISTER (A2 thru A0 = 6)

This register contains the desired sector size, drive number, and head number parameters.

7	6 5	4 3	2 1 0
EXT	SIZE	DRIVE	HEAD

6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

4	3	DRIVE #
0	0	DSEL 1
0	1	DSEL 2
1	0	DSEL 3
1	1	DSEL 4

2	1	0	HEAD #
0	0	0	HSEL 0
0	0	1	HSEL 1
0	1	0	HSEL 2
0	1	1	HSEL 3
1	0	0	HSEL 4
1	0	1	HSEL 5
1	1	0	HSEL 6
1	1	1	HSEL 7

NOTE:

Drive select and head select lines must be generated externally. Figure 3 represents one method of achieving this.

As shown below, the SDH byte written in the ID field during the Format Command is not the same as the contents of the SDH Register.

Bit 7 — One selects the ECC mode for the data field. Zero selects the CRC mode for the data field.

7	6 5	4 3		2 1 0
BAD B.	SIZE	0	0	HEAD

STATUS REGISTER (A2 thru A0 = 7 read)

The Status Register is used to inform the Host of certain events performed by the WD2010 as well as reporting status from the drive control lines. Reading the Status Register de-asserts INTRQ

7	6	5	4	3	2	1	0
BSY	RDY	WF	SC	DRQ	DWC	CIP	ERR

Bit 7 — Busy

BUSY is asserted when a command is written into the Command Register and, except for the Read Command, it is de-asserted at the end of the command. When executing a Read Sector Command, BUSY is de-asserted when the Sector Buffer is full. Commands should not be loaded into the Command Register when this bit is set. When the BUSY bit is set, no other bits in the Status or Error Register are valid.

Bit 6 — Ready
This bit reflects the status of DRDY. When this bit equals zero, the command is aborted and the status of this bit is latched.

Bit 5 — Write Fault
This bit reflects the status of WF. When this bit equals one, the command is aborted, INTRQ is asserted, and the status of this bit is latched.

Bit 4 — Seek Complete
This bit reflects the status of SC. When a seek or implied seek has been initiated by a command, it pauses until the seek is complete. This bit is latched after an "aborted command" error.

Bit 3 — Data Request
DRQ reflects the same status as BDRQ. It is asserted when the data Sector Buffer must be written into, or read from. DRQ and BDRQ remain asserted until BRDY indicates that the Sector Buffer has been filled or emptied, depending upon the command. DRQ is used during Program Interrupt and must be interrogated by the Host to determine that the WD2010 is ready. BDRQ operates through a DMA controller for data transfers.

Bit 2 — Data Was Corrected
When a one, this bit indicates an error has been detected during the ECC mode of operation and the data in the Sector Buffer has been corrected. This provides the user with an indication that there may be a marginal condition within the drive before the errors become uncorrectable. This bit is forced to zero when not in the ECC mode of operation.

Bit 1 — Command in Progress (CIP)
When this bit is set, a command is being executed and a new command should not be loaded. Although a command is being executed the Sector Buffer is still available for access by the Host. When the WD2010 is no longer busy, (bit 7 = 0) the Status Register can be read. Any attempt to read the other registers results in reading the status.

Bit 0 — Error
This bit indicates that a non-recoverable error has occurred. When the Host reads the status and finds this bit set, it must then read the Error Register to determine what type of error it was.

COMMAND REGISTER (A2 thru A0 = 7 write)
The command to be executed is written into this register.

7	6	5	4	3	2	1	0
COMMAND							

The command asserts BUSY and CIP, and begins to execute as soon as it is written into this register. Therefore, all necessary information should be loaded into the Task File prior to entering the command. Any attempt to write into these registers is ignored until the command has terminated, as indicated by the CIP status. INTRQ is de-asserted if it is still active at the time the command is written.

COMMAND SUMMARY:

	BIT							
COMMAND	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESTORE	0	0	0	1	R3	R2	R1	R0
SEEK	0	1	1	1	R3	R2	R1	R0
READ SECTOR	0	0	1	0	I	M	L	T
WRITE SECTOR	0	0	1	1	0	M	L	T
SCAN ID	0	1	0	0	0	0	0	T
WRITE FORMAT	0	1	0	1	0	0	0	0
COMPUTE CORRECTION	0	0	0	0	1	0	0	0
SET PARAMETER	0	0	0	0	0	0	0	S

Stepping Rate Field R3-R0

For 5 MHz WCLK:

R3-R0 = 0000	35μsec	1010	5.0msec
0001	.5msec	1011	5.5msec
0010	1.0msec	1100	6.0msec
0011	1.5msec	1101	6.5msec
0100	2.0msec	1110	3.2μsec
0101	2.5msec	1111	16μsec
0110	3.0msec		
0111	3.5msec		
1000	4.0msec		
1001	4.5msec		

STEP PULSE WIDTH =
1.6μsec at 3.2μsec rate
8.0μsec at all others.

I — Interrupt Control

I = 0 INTRQ occurs with BDRQ/DRQ indicating the Sector Buffer is full (valid only when M = 0).

I = 1 INTRQ occurs when the command is completed and the Host has read the Sector Buffer.

M — Multiple Sector Flag

M = 0 Transfer one sector (the sector count is ignored)

M = 1 Transfers multiple sectors

L — Long Mode

L = 0 Normal mode, normal CRC or ECC functions are performed.

L = 1 Long mode, no CRC or ECC bytes are developed or error checking performed on the data field. The WD2010 appends the four additional bytes supplied by the Host or disk to the data field.

T — Retry Flag

T = 0 Enable Retry

T = 1 Disable Retry

S — Error Correction Span

S = 0 5-bit span

S = 1 11-bit span

RESTORE COMMAND

The Restore command is used to position the read/write heads over track zero. It is usually issued by the Host when a drive has just been turned on.

The stepping rate used for the restore is determined by SC. The WD2010 issues a Step pulse and then waits for the leading edge of SC before starting another step. If the leading edge of SC is not seen within 10 revolutions (index pulses) the WD2010 switches to sensing the level of SC. If after 2047 Stepping pulses TK000 is not asserted, the WD2010 sets the Track Zero error bit, asserts INTRQ and terminates the operation. An interrupt also occurs if WRITE FAULT is asserted or DRDY is de-asserted during execution.

The stepping rate field is stored in an internal register for future use by commands with implied seeks.

SEEK COMMAND

By not testing SC, the Seek Command is capable of overlapping seeks on multiple drives. R3 through R0 controls the stepping rate, as well as being written into an internal register for use by those commands with implied seek capability.

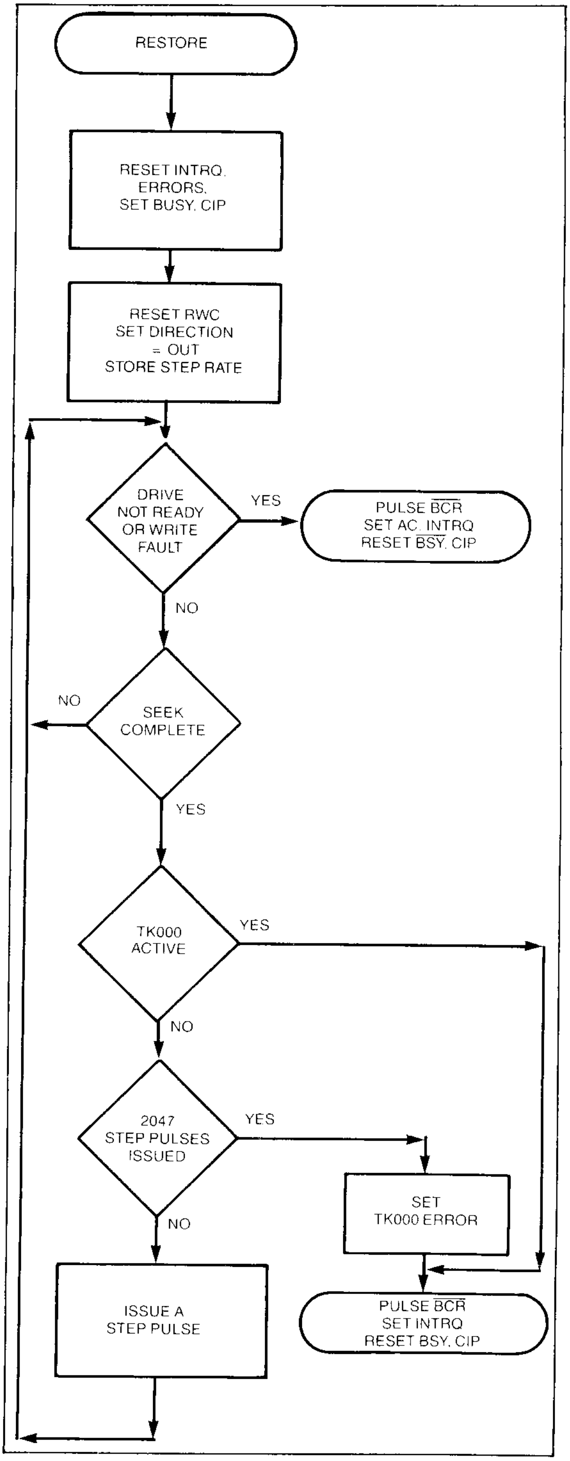

RESTORE
RESET INTRQ. ERRORS. SET BUSY. CIP
RESET RWC SET DIRECTION = OUT STORE STEP RATE
DRIVE NOT READY OR WRITE FAULT
YES
PULSE BCR SET AC. INTRQ RESET BSY. CIP
NO
SEEK COMPLETE
NO
YES
TK000 ACTIVE
YES
NO
2047 STEP PULSES ISSUED
YES
SET TK000 ERROR
NO
ISSUE A STEP PULSE
PULSE BCR SET INTRQ RESET BSY. CIP

FIGURE 7. RESTORE COMMAND

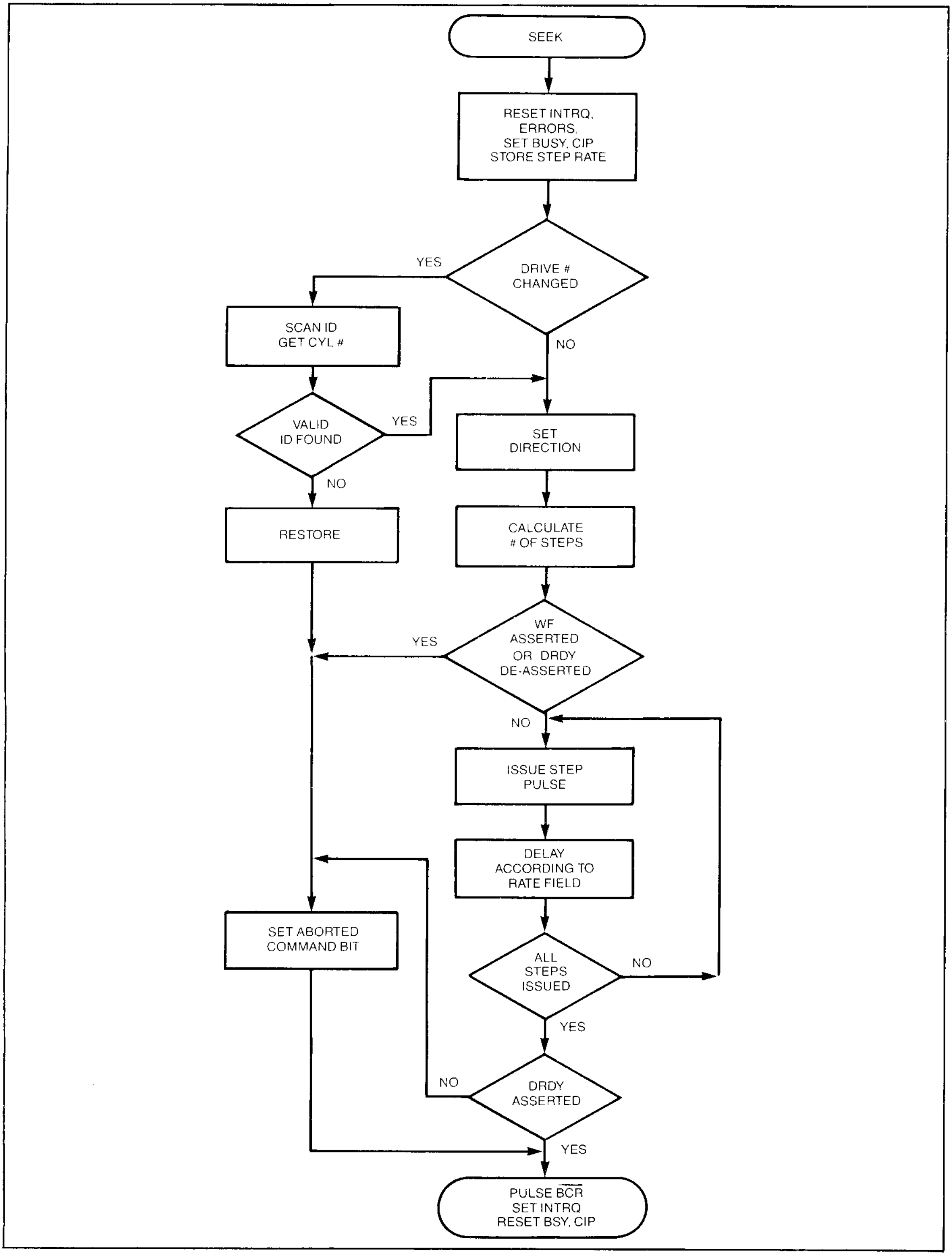


FIGURE 8. SEEK COMMAND

The direction and number of step pulses needed are calculated by comparing the contents of the cylinder number in the Task File to the present cylinder position number stored internally. After all the steps have been issued, the present position cylinder number is updated, INTRQ asserted and the command terminated. If DRDY is de-asserted or WF is asserted during the execution of the command, INTRQ is asserted, and the command aborts setting the AC error.

If an implied seek is performed, the stepping rate for all but the last step is controlled by R3 through R0. On the last step the seek continues until the leading edge of SC is detected.

READ SECTOR

The Read Sector command is used to transfer one or more sectors of data from the disk to the Sector Buffer. Upon receipt of this command, the WD2010 compares the cylinder number in the Task File with the Present Cylinder Position Register. From this, the direction and number of steps required for the seek are calculated. As stated in the Seek Command, if an implied seek is performed, the stepping rate for all but the last step is controlled by R3 through R0. On the last step the seek continues until the leading edge of SC is detected.

If the WD2010 detects a change in the drive number since the last Read Command, an Auto Scan ID is performed. This updates the Present Cylinder Position Register to reflect the current drive before the seek begins.

After the WD2010 senses SC (with or without an implied seek) it must find an ID field with the correct cylinder, head, sector size, and CRC. With Retry enabled (T = 0), ten attempts are made to find the correct ID field. If there is still an error on the tenth try, an auto-scan and auto-seek are performed. Then, ten more tries are made before setting the ID Not Found Error. When Retry is disabled (T = 1) only two tries are made, and no auto-scan or auto-seek operations are performed.

When the Data Address Mark is found, the WD2010 is ready to transfer data into the Sector Buffer (if after successfully reading the correct ID field, the Data Address Mark is not found a DAM error is set). When the disk has filled the Sector Buffer, the WD2010 asserts BDRQ and DRQ and then checks the I flag. If the flag is 0, INTRQ is asserted also, signaling the Host to read the content of the Sector Buffer. If the I flag is 1, INTRQ occurs after the Host has read the Sector Buffer and terminated the command.

An optional M flag can be set for multiple sector transfers. When M = 0, one sector is transferred and the sector count is ignored. When M = 1, multiple sectors are enabled. After each sector is transferred, the WD2010 decrements the sector count and increments the sector number. The next logical sector is transferred, regardless of the interleave. Sectors are numbered by a byte in the ID field during the Format Command.

For the WD2010 to make multiple sector transfers to the Sector Buffer, the BRDY signal must toggle from low to high for each sector. The sector transfers continue until the sector count equals zero. If the sector count is not zero (indicating more sectors are to be read) and the Sector Buffer is full, BDRQ is asserted and the Host must unload the Sector Buffer. Once this occurs, the Sector Buffer is free to accept the next sector.

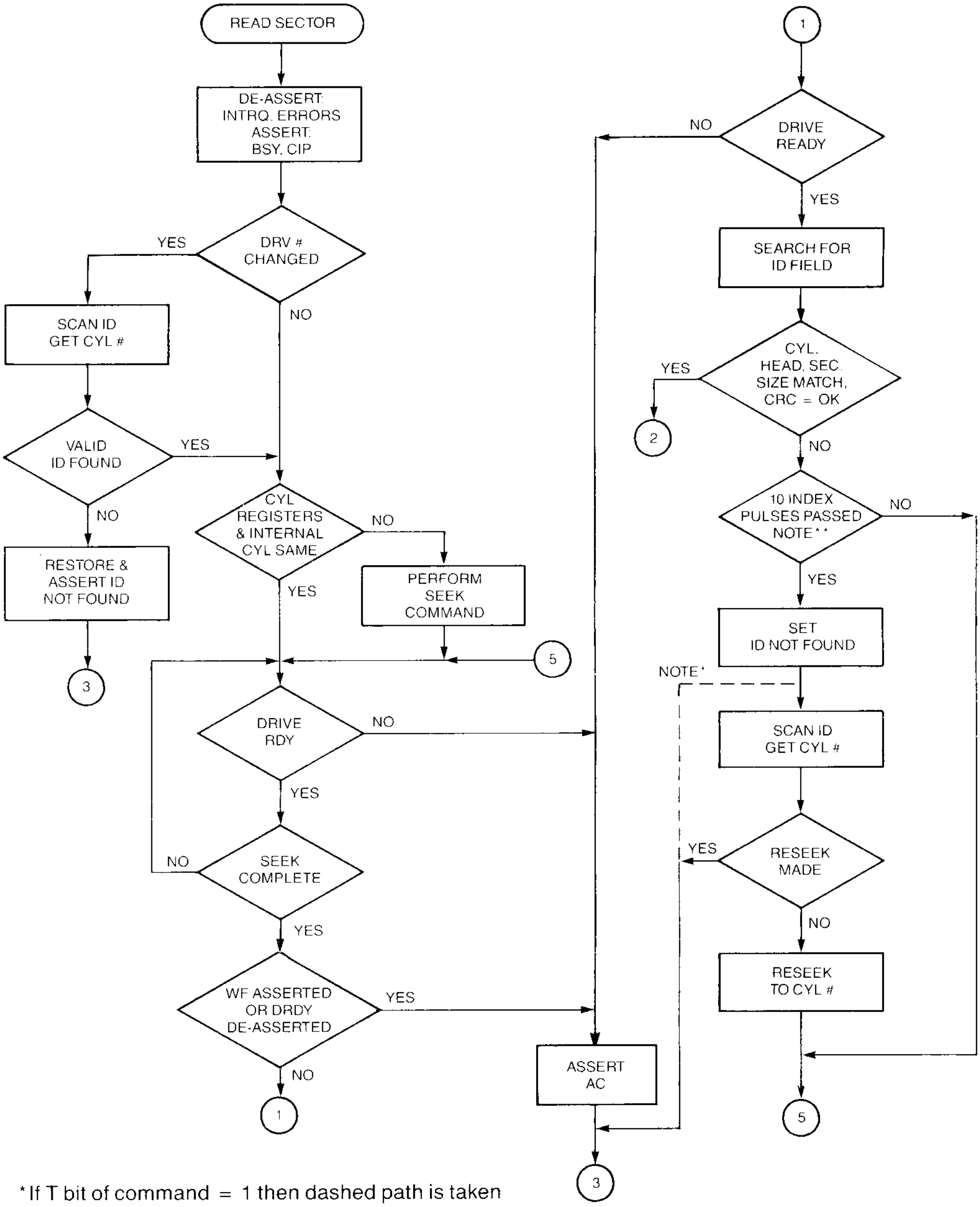
WF and DRDY are monitored throughout the command. If WF becomes asserted, or DRDY de-asserted, the command terminates and the AC error flag is set. For a description of the error checking procedure on the data field see the explanation under CRC and ECC Generator and Checker. Both the Read and Write commands feature a simulated completion to ease programming. BDRQ, DRQ, and INTRQ are generated in a normal manner upon detecting an error condition. This allows the same program flow for successful or unsuccessful completion of a command.

When M = 0 (Single Sector Read)

(1) Host: Sets up parameters; issues Read Sector command.
(2) 2010: Finds sector specified; asserts $\overline{BCR}$ and $\overline{BCS}$. Sector Buffer data transfer via $\overline{WE}$.
(3) 2010: Asserts $\overline{BCR}$ de-asserts $\overline{BCS}$.
(4) 2010: Asserts BDRQ and DRQ flag.
(5) 2010: If I bit = 0 then (8).
(6) Host: Reads contents of Sector Buffer (by asserting $\overline{RE}$).
(7) 2010: Waits for BRDY then asserts INTRQ; End.
(8) 2010: Asserts INTRQ.
(9) Host: Reads contents of Sector Buffer (by asserting $\overline{RE}$); End.

When M = 1 (Multiple Sector Read)

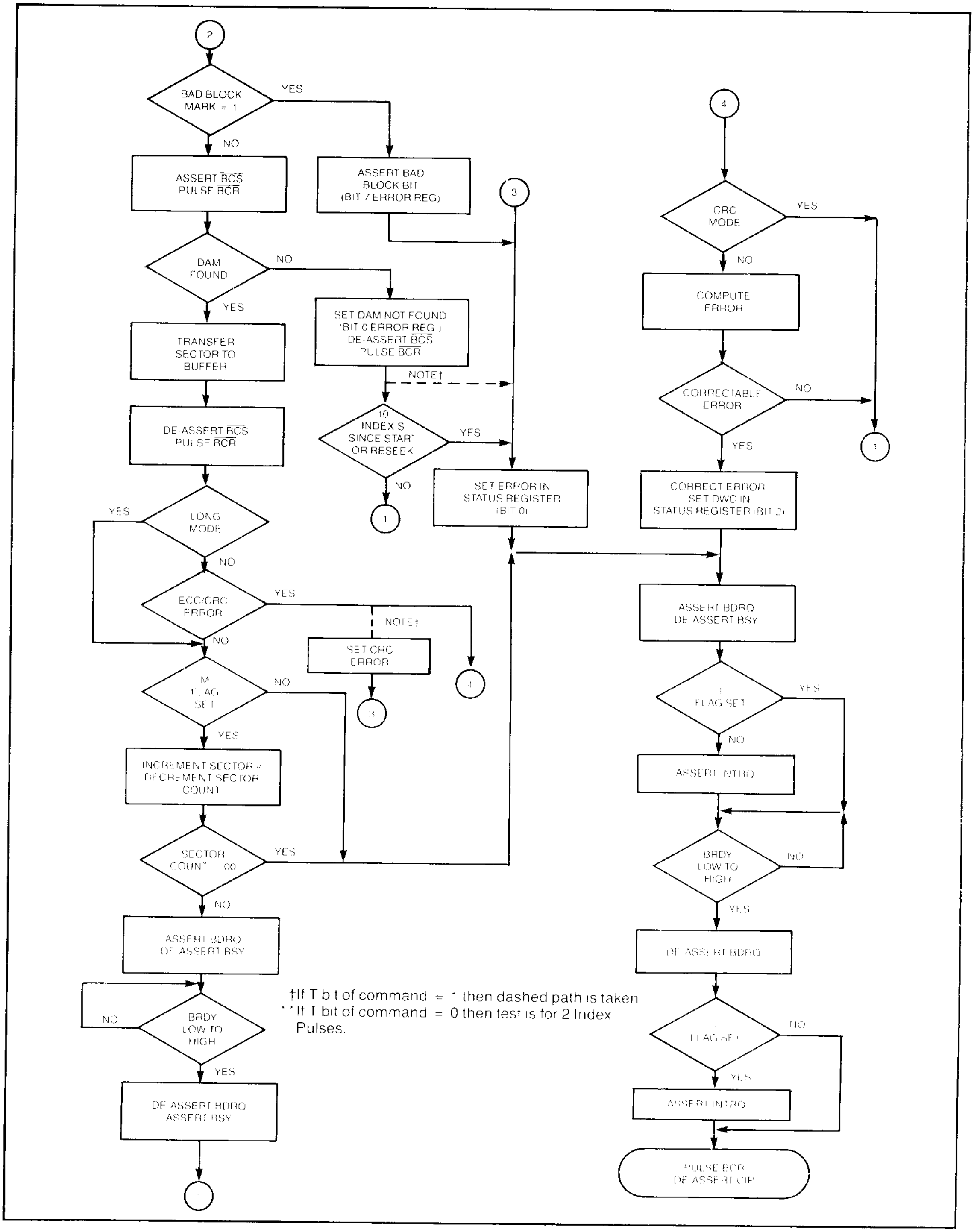
(1) Host: Sets up parameters; issues Read Sector command.
(2) 2010: Finds sector specified; asserts $\overline{BCR}$ and $\overline{BCS}$. Sector Buffer data transfer via $\overline{WE}$.
(3) 2010: Asserts $\overline{BCR}$; de-asserts $\overline{BCS}$.
(4) 2010: Asserts BDRQ and DRQ flag.
(5) Host: Reads contents of Sector Buffer (by asserting $\overline{RE}$).
(6) Sector Buffer: Indicates data has been transferred by asserting BRDY.
(7) 2010: When BRDY is asserted, decrements sector count; increments sector number, go to (9) if sector count = 0
(8) 2010: Go to Step (2).
(9) 2010: Asserts INTRQ; End.



*If T bit of command = 1 then dashed path is taken after 2 index pulses.

**If T bit of command = 1 then test is for 2 Index Pulses.

FIGURE 9. READ COMMAND



†If T bit of command = 1 then dashed path is taken
**If T bit of command = 0 then test is for 2 Index Pulses.

FIGURE 9. READ COMMAND (Continued)

WRITE SECTOR

The Write Sector Command is used to write one or more sectors of data from the Sector Buffer to the disk. Upon receipt of this command, the WD2010 compares the cylinder number in the Task File with the present position cylinder number. From this, the direction and number of steps required for the seek are calculated. As stated in the Seek Command, if an implied seek is performed, the stepping rate is controlled by R3 through R0. After the last step the WD2010 waits until the leading edge of SC is received.

If the WD2010 detects a change in the drive number since the last Write Command, an auto-Scan ID takes place. This updates the Present Cylinder Position Register to reflect the current drive before the seek begins.

After the WD2010 senses SC (with or without an implied seek), BDRQ and DRQ signals are asserted and the Host proceeds filling the Sector Buffer. When BRDY is asserted, a search for an ID with the specified cylinder, head, sector size, and CRC is initiated. If the ID is not found and Retry is enabled (T = 0), ten attempts are made to find the correct ID field. If there is still an error on the tenth try, an auto-scan and auto-seek is performed. Then ten more tries are made before setting the Error Status bit. (The ID Not Found error is set on the first failure.) When Retry is disabled (T = 1), only two tries are made and no auto-scan or auto-seek operations are performed.

When the correct ID is found, WG is asserted and data is written to the disk. When SDH 7 bit is zero, WD2010 generates a two byte CRC character to be appended to the data. When SDH 7 bit is one, four ECC bytes replaces the CRC character. When the L bit within the Write Command is one, the polynomial generation of the data is inhibited, and neither CRC or ECC bytes are generated. Instead, four bytes of data supplied by the Host is written.

During a multiple sector write operation (M flag = 1), the sector number is incremented and sector count decremented. If BRDY is asserted after the first sector is read from the Sector Buffer, WD2010 continues to read data from the Sector Buffer for the next sector. If BRDY is de-asserted, WD2010 asserts BDRQ and waits for the Host to place more data in the Sector Buffer.

Summary of a write sector operation:

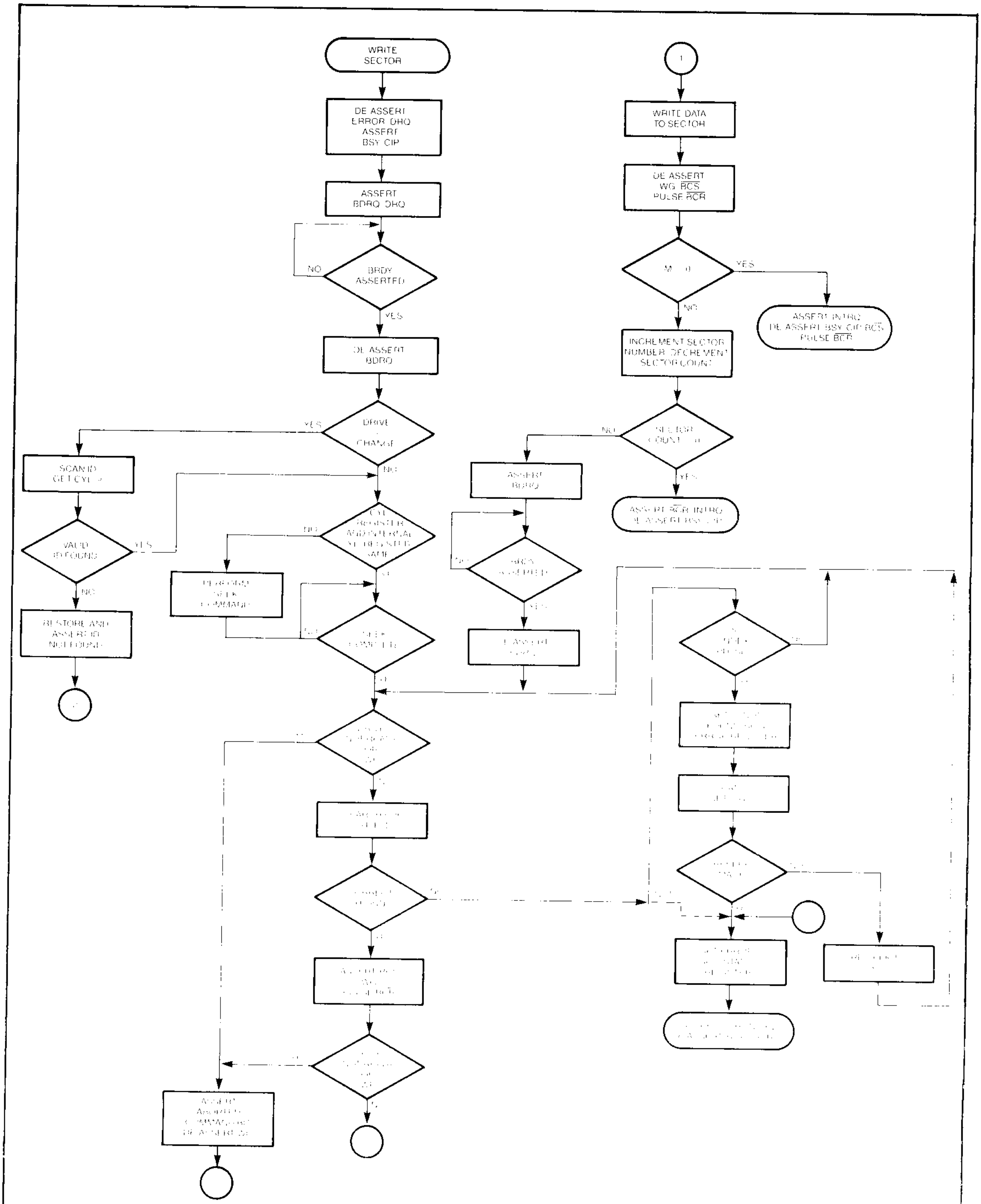
(1) Host: Sets up parameters; issues write sector command.
(2) 2010: Asserts BDRQ and DRQ.
(3) Host: Loads Sector Buffer with data (by asserting $\overline{WE}$).
(4) 2010: Waits for leading edge of BRDY.
(5) 2010: Finds specified ID field, write to sector.
(6) 2010: If M = 0, assert INTRQ; End.
(7) 2010: Increments sector number, decrements sector count.
(8) 2010: If sector count = 0, assert INTRQ; End.
(9) 2010: Go to (2).

SCAN ID

The Scan ID Command is used to update the head, sector size, sector number, and cylinder registers.

When the first ID field is encountered, the ID information is loaded into the SDH cylinder, and sector number registers in the Task File. The Present Position Cylinder Register is also updated. If this is an Auto-Scan caused by a change in drive numbers, only the present position cylinder number is altered.

If the ID field is not found and Retry is enabled (T = 0), ten attempts are made to read it. If Retry is disabled (T = 1), only two tries are made. There is no implied seek in this command and the Sector Buffer remains unchanged. When DRDY is de-asserted or WF asserted the command aborts and the appropriate error flags are asserted.


WRITE SECTOR
DE ASSERT ERROR DRQ ASSERT BSY CIP
ASSERT BDRQ DRQ
NO
BRDY ASSERTED
YES
DE ASSERT BDRQ
YES
DRIVE CHANGE
NO
SCAN ID GET CYL #
VALID ID FOUND
YES
NO
RESTORE AND ASSERT ID NOT FOUND
CYL REGISTER AND INTERNAL CYL REGISTER SAME
NO
PERFORM SEEK COMMAND
SEEK COMPLETE
1
WRITE DATA TO SECTOR
DE ASSERT WG BCS PULSE BCR
M = 0
YES
ASSERT INTRQ DE ASSERT BSY CIP BCS PULSE BCR
NO
INCREMENT SECTOR NUMBER DECREMENT SECTOR COUNT
NO
SECTOR COUNT = 0
YES
ASSERT BCR INTRQ DE ASSERT BSY CIP
ASSERT BDRQ
NO
BRDY ASSERTED
YES
DE ASSERT BDRQ

*If retries disabled then dashed path is taken after 2 Index Pulses.

FIGURE 10. WRITE COMMAND

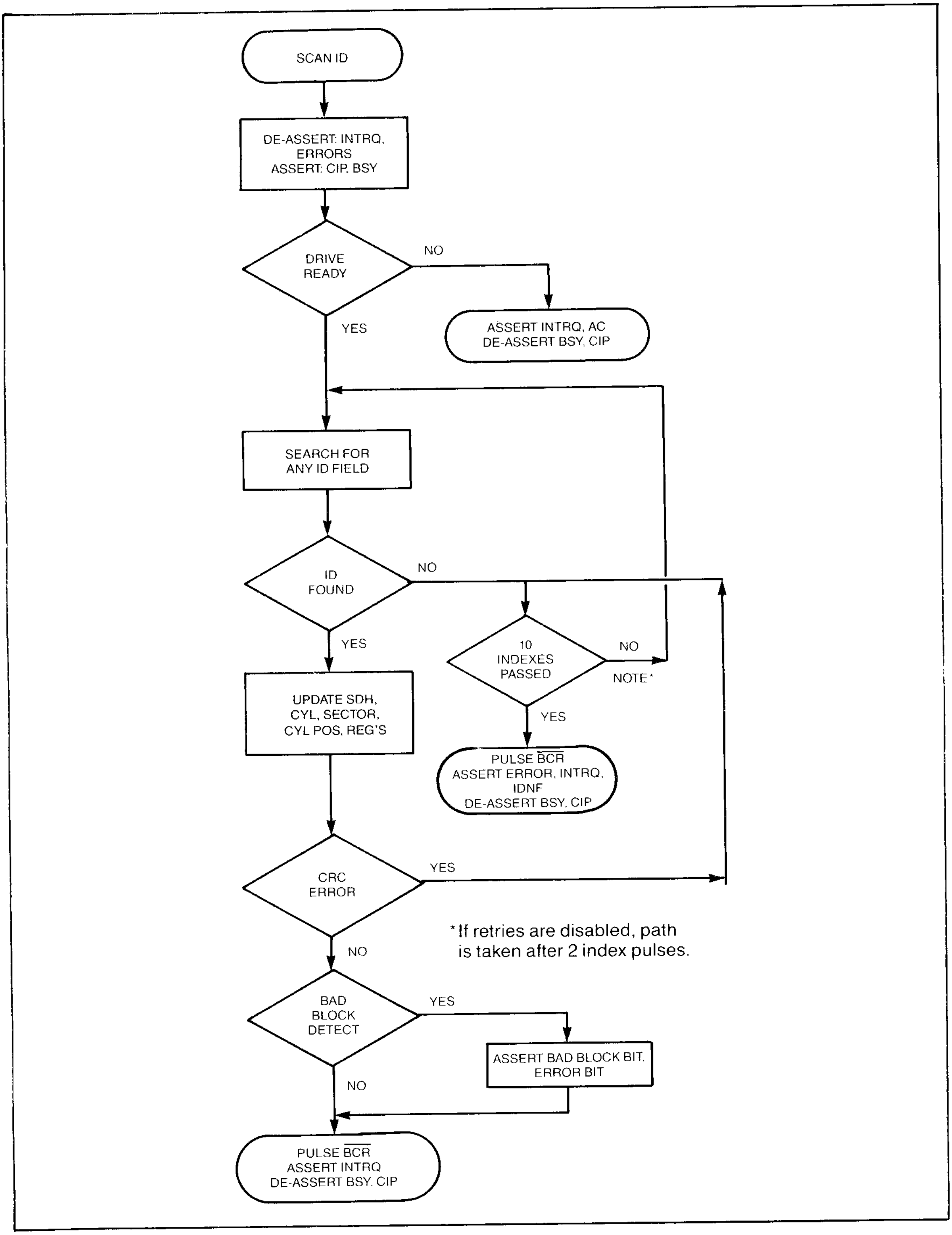


FIGURE 11. SCAN ID COMMAND

FORMAT

The Format Command is used to format one track using the Task File and Sector Buffer. During this command the Sector Buffer contains additional parameter information instead of data. Figure 12 shows the contents of the Sector Buffer for a 32 sector track format with an interleave factor of two.

Each sector requires a two byte sequence. The first byte designates if a Bad Block Mark is to be recorded in the ID field. A 00 is normal; an 80 hex is a Bad Block Mark. In the example of Figure 12, sector 04 gets a Bad Block Mark recorded. The second byte indicates the logical sector number to be recorded. Using this scheme, sectors can be recorded in any interleave factor desired. The rest of the Sector Buffer is filled with any value, BRDY is asserted, and the WD2010 begins formatting the track.

The Sector Count Register holds the total number of sectors to be formatted, while the Sector Number Register holds the number of bytes, minus three, to be used for Gap 1 and Gap 3. For instance, if the Sector Count value is 2 and the Sector Number value is 3, then 2 sectors are written and 6 bytes of 4E hex are written for Gap 1 and Gap 3. The data fields are filled with FF hex, and the CRC or ECC is generated as specified by the related coding.

The Gap 3 value is determined by the drive motor speed variation, data sector length, and the interleave factor. The interleave factor is only important when 1:1 interleave is used. The formula for determining the minimum Gap 3 is:

Gap 3 = 2 X M X S + K

M = motor speed variation (e.g. .03 for ± 3%)
S = sector length in bytes
K = 18 for an interleave factor of 1
K = 0 for any other interleave factor

When WF is asserted or DRDY de-asserted the command terminates and the AC error is asserted. Figure 13 shows the format that is written on the disk.

	DATA							
ADDR	0	1	2	3	4	5	6	7
00	00	00	00	10	00	01	00	11
08	00	02	00	12	00	03	00	13
10	80	04	00	14	00	05	00	15
18	00	06	00	16	00	07	00	17
20	00	08	00	18	00	09	00	19
28	00	0A	00	1A	00	0B	00	1B
30	00	0C	00	1C	00	0D	00	1D
38	00	0E	00	1E	00	0F	00	1F
40	FF	FF	FF	FF	FF	FF	FF	FF
				⋮				
F0	FF	FF	FF	FF	FF	FF	FF	FF

FIGURE 12. FORMAT COMMAND BUFFER CONTENTS

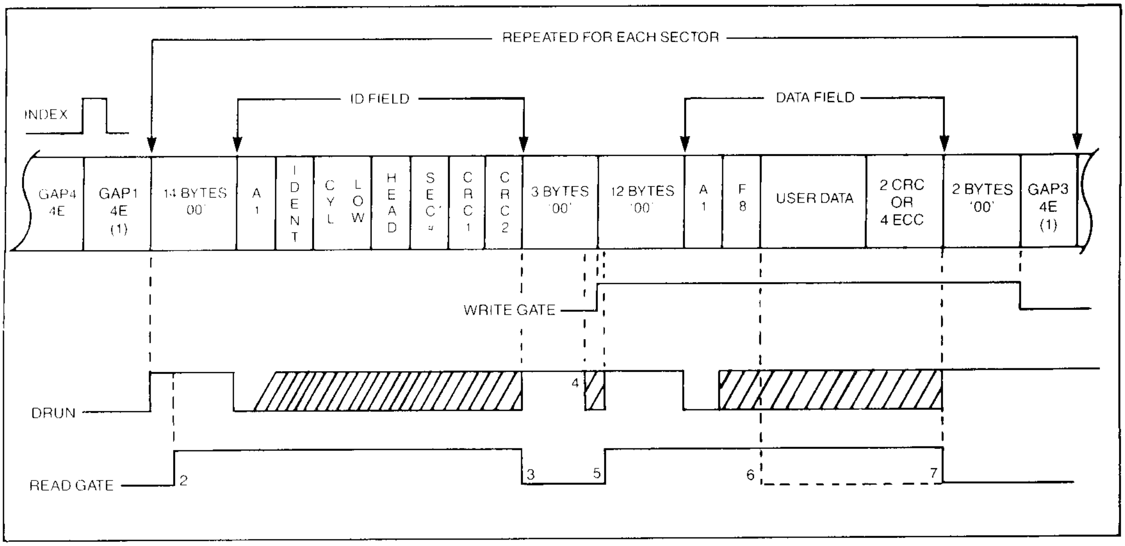


FIGURE 13. FORMAT

ID FIELD

A1 = A1 hex with 0A hex clock
IDENT = Bits 3, 1, 0 = Cylinder High
FE = 0-255 Cylinders
FF = 256-511 Cylinders
FC = 512-767 Cylinders
FD = 768-1023 Cylinders
F6 = 1024-1279 Cylinders
F7 = 1280-1535 Cylinders
F4 = 1536-1791 Cylinders
F5 = 1792-2047 Cylinders
HEAD = Bits 0, 1, 2 = Head Number
Bits 3, 4 = 0
Bits 5, 6 = Sector Size
Bit 7 = Bad Block Mark
Sec # = Logical Sector Number

DATA FIELD

A1 = A1 hex with 0A hex clock
F8 = Data Address Mark; Normal Clock
USER = Data Field 128 to 1024 Bytes

NOTES:

1. GAP 1 and 3 length determined by Sector Number Register contents during formatting.
2. The decision to assert RG is made 2 bytes after the start of DRUN.
3. RG de-asserted:
   - If DRUN does not last until A1
   - When any part of ID does not match the one expected.
   - After CRC if correct ID has been read.
4. Write splice recorded on disk by asserting WG.
5. RG is suppressed until after write splice.
6. Not a proper A1 or F8, set DAM error.
7. Sector size as stated in ID field, plus two for CRC or 4 for ECC.

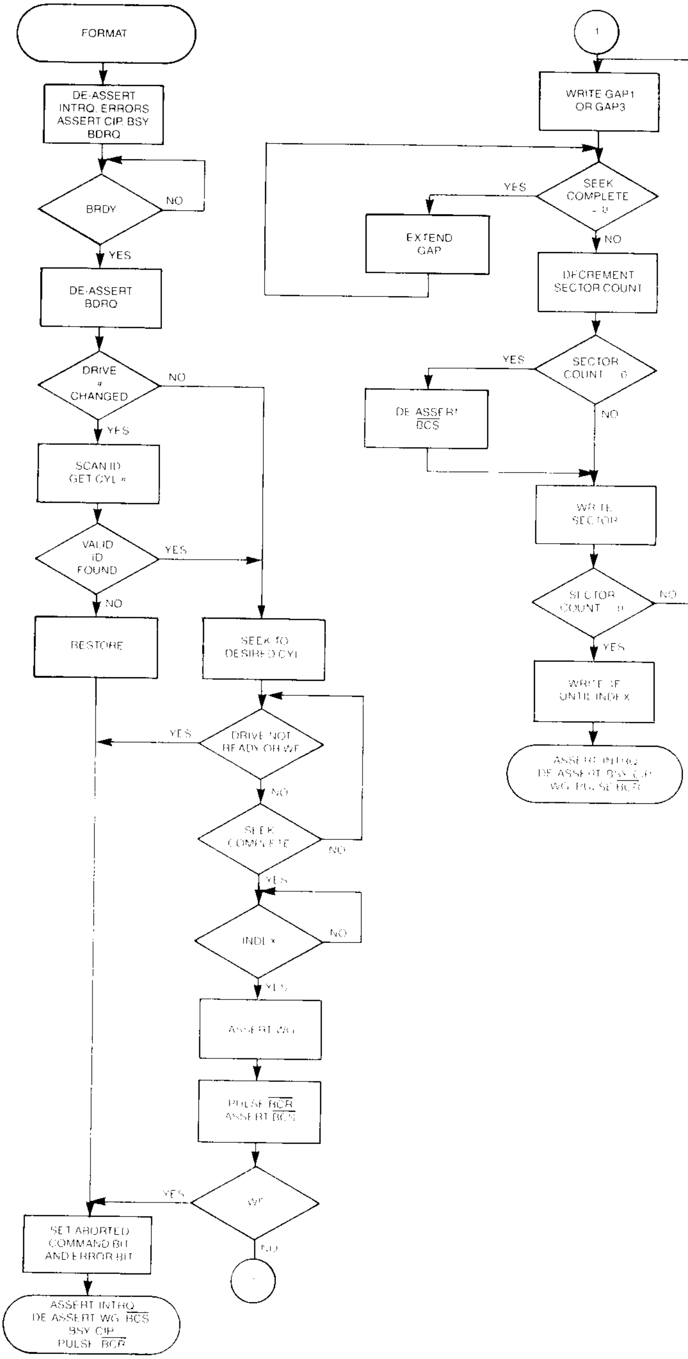


FIGURE 14. FORMAT COMMAND

COMPUTE CORRECTION

The Compute Correction Command determines the location and pattern of a single burst error, but does not correct it. The Host, using the data provided by the WD2010, must perform the actual correction. The Compute Correction Command is used following a data field ECC Error. The command initiating the read operation must specify no Retry. (T = 1).

The Compute Correction Command first writes the four syndrome bytes from the internal ECC Register to the Sector Buffer then the ECC Register is clocked. With each clock, a counter is incremented and the pattern examined. If the pattern is correctable, the procedure is stopped and the count and pattern are written to the Sector Buffer, following the syndrome. The process is also stopped if the count exceeds the sector size before a correctable pattern is found.

When the command terminates the Sector Buffer contains the following data.

Syndrome	MSB
Syndrome	
Syndrome	
Syndrome	
Error Pattern Offset	
Error Pattern Offset	
Error Pattern	
Error Pattern	
Error Pattern	LSB

As an example, when the Error Pattern Offset is zero the following procedure may correct the error. The first data byte of the sector is exclusive OR'ed with the MSB of the Error Pattern, the second byte of data with the second byte of the Error Pattern, and the third byte of data with the LSB of the Error Pattern.

If the Sector Buffer count exceeds the sector size, or the burst is greater than that selected by the Set Parameter Command, the ECC/CRC error (bit 6) and the Error Status bit (bit 0) is set.

The WD2010 defaults to a 5-bit correction span if a Set Parameter Command has not been executed since the last $\overline{\text{MR}}$.

SET PARAMETER

This command selects the correction span to be used by the error correction process. A 5-bit span is selected when bit zero of the command equals 0, and 11-bit span when 1. The WD2010 defaults to a five bit span following a Master Reset.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) . . . . +7V
Max Voltage on any Pin with
  respect to V_{SS} . . . . −0.5V to +7V
Operating Temperature . . 0°C (32°F) to 70°C (158°F)
Storage Temperature . . −55°C (−67°F) to + 125°C (257°F)

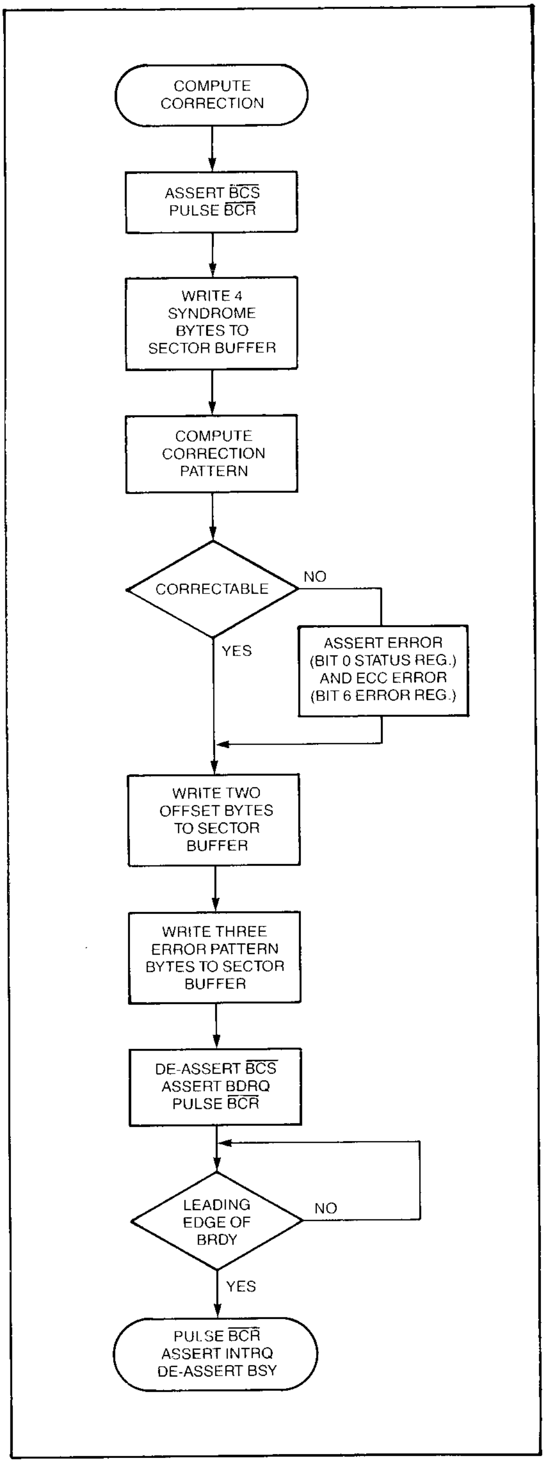
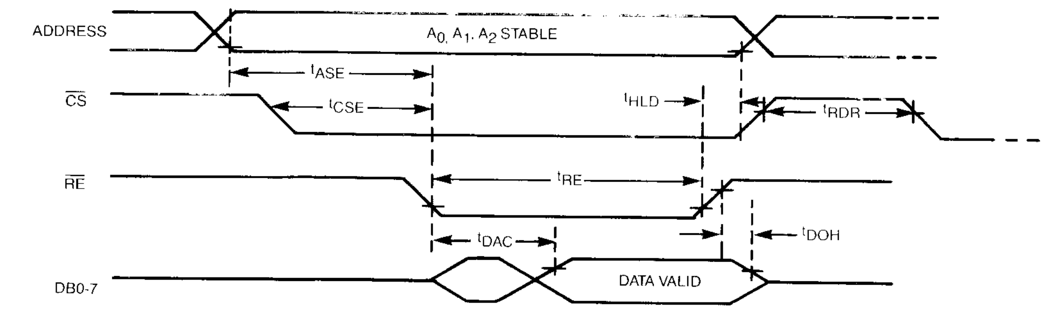

COMPUTE CORRECTION
ASSERT $\overline{BCS}$ PULSE $\overline{BCR}$
WRITE 4 SYNDROME BYTES TO SECTOR BUFFER
COMPUTE CORRECTION PATTERN
CORRECTABLE
NO
YES
ASSERT ERROR (BIT 0 STATUS REG.) AND ECC ERROR (BIT 6 ERROR REG.)
WRITE TWO OFFSET BYTES TO SECTOR BUFFER
WRITE THREE ERROR PATTERN BYTES TO SECTOR BUFFER
DE-ASSERT $\overline{BCS}$ ASSERT BDRQ PULSE $\overline{BCR}$
LEADING EDGE OF BRDY
NO
YES
PULSE $\overline{BCR}$ ASSERT INTRQ DE-ASSERT BSY

FIGURE 15. COMPUTE CORRECTION COMMAND

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating characteristics.

DC Operating Characteristics T_A = 0°C (32°F) to 70°C (158°F); V_{SS} = 0V, V_{CC} = +5V ± .25V

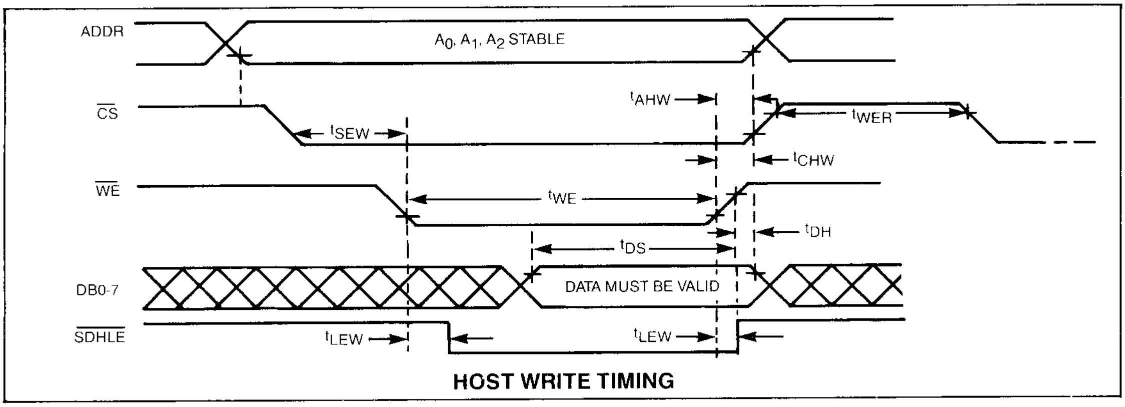
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		± 10	μA	V_{IN} = .4 to V_{CC}
I_{OL}	Output Leakage (Tristate & Open Drain)		± 10	μA	V_{OUT} = .4 to V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_O = −100μA
V_{OL}	Output Low Voltage		0.4	V	I_O = 1.6 mA
V_{OL}	Output Low Voltage (Pins 21-23)		0.45	V	I_O = 6.0 mA See Note 10
I_{CC}	Supply Current		220	mA	All Outputs Open
	For Pins 25, 34, 37, 39:				
V_{IH}	Input High Voltage	4.6		V	
V_{IL}	Input Low Voltage		0.5	V	
TRS	Rise and Fall Time		30	nsec	.9V to 4.2V
C_{IN}	Input Capacitance		15	pF	



HOST READ TIMING

HOST READ TIMING WD2010-05 WC = 5 MHz

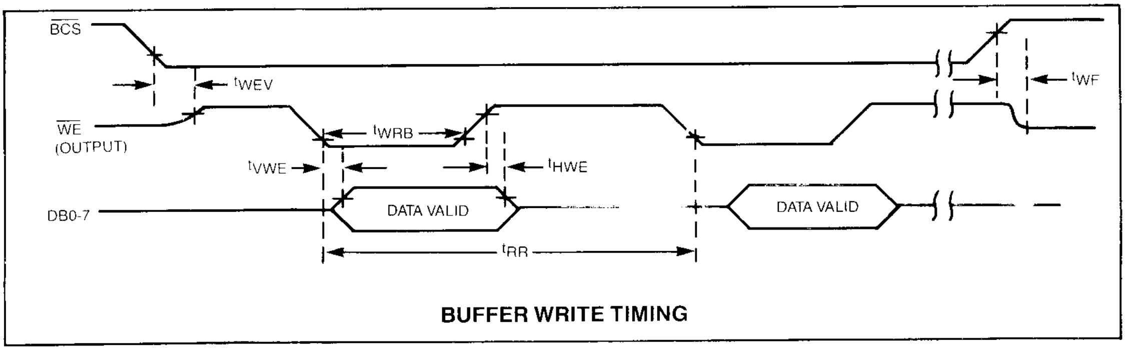
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{ASE}	Address Setup to $\overline{\text{RE}}$	100		nsec	
t_{DAC}	Data Valid from $\overline{\text{RE}}$		350	nsec	
t_{RE}	Read Enable Pulse Width	.4	10	μsec	
t_{DOH}	Data Hold from $\overline{\text{RE}}$	20	200	nsec	
t_{HLD}	Address $\overline{\text{CS}}$ hold from $\overline{\text{RE}}$	0		nsec	
t_{RDR}	Read Recovery Time	300		nsec	
t_{CSE}	$\overline{\text{CS}}$ Setup to $\overline{\text{RE}}$	0		nsec	See Note 8



HOST WRITE TIMING

HOST WRITE TIMING WD2010-05

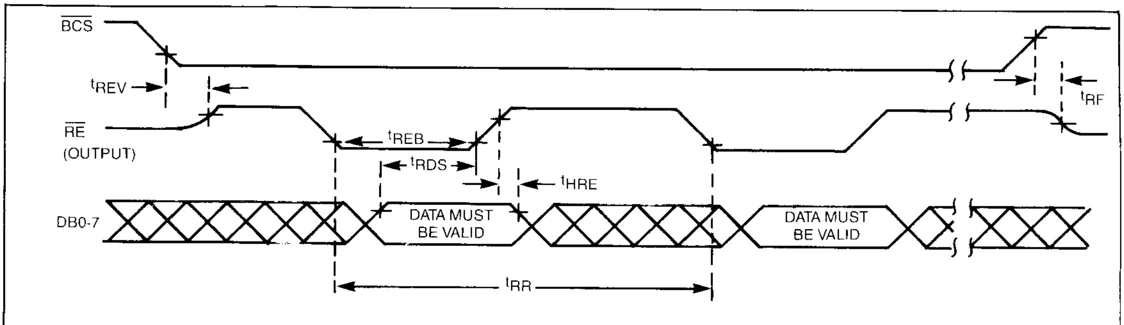
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{SEW}	Address $\overline{CS}$ Setup to $\overline{WE}$	0	10	μsec	
t_{DS}	Data Bus Setup to $\overline{WE}$	.2	10	μsec	
t_{WE}	Write Enable Pulse Width	.2	10	μsec	
t_{DH}	Data Bus Hold from $\overline{WE}$	10		nsec	
t_{AHW}	Address Hold from $\overline{WE}$	30		nsec	
t_{WER}	Write Recovery Time	1.0		μsec	See Note 1
t_{CHW}	$\overline{CS}$ Hold Time from $\overline{WE}$	0			See Note 9
t_{LEW}	$\overline{SDHLE}$ Propagation Delay	20	150	nsec	



BUFFER WRITE TIMING

BUFFER WRITE TIMING (READ SECTOR CMD) WD2010-05 WC = 5 MHz

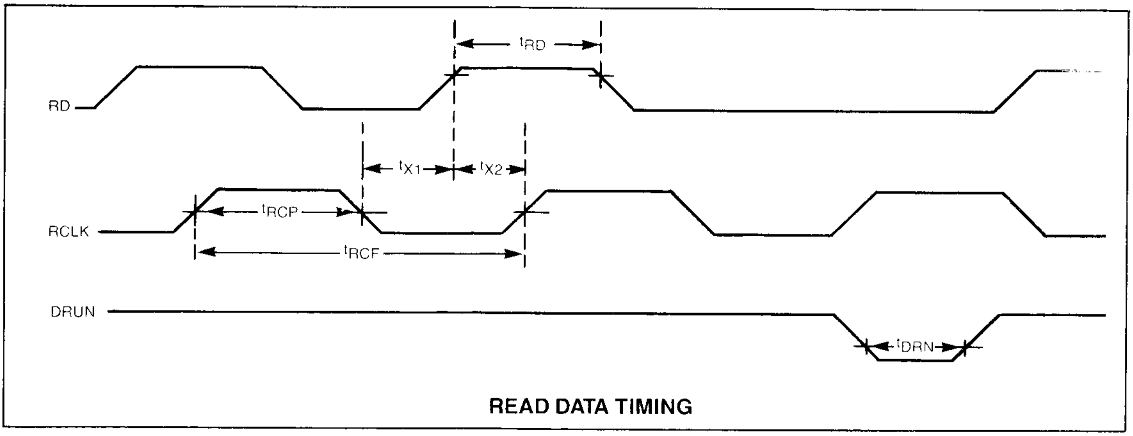
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{WEV}	$\overline{WE}$ Float to $\overline{WE}$ Valid	0		100	nsec	$C_L = 50$ pf
t_{WRB}	$\overline{WE}$ Output Pulse Width	300	400	500	nsec	See Note 4
t_{VWE}	Data Valid from $\overline{WE}$			150	nsec	
t_{HWE}	Data Hold from $\overline{WE}$	60		200	nsec	
t_{RR}	$\overline{WE}$ Repetition Rate	1.2	1.6	2.0	μsec	
t_{WF}	$\overline{WE}$ Float from $\overline{BCS}$	0		100	nsec	$C_L = 50$ pf



BUFFER READ TIMING

BUFFER READ TIMING (WRITE SECTOR CMD) **WD2010-05 WC = 5 MHz**

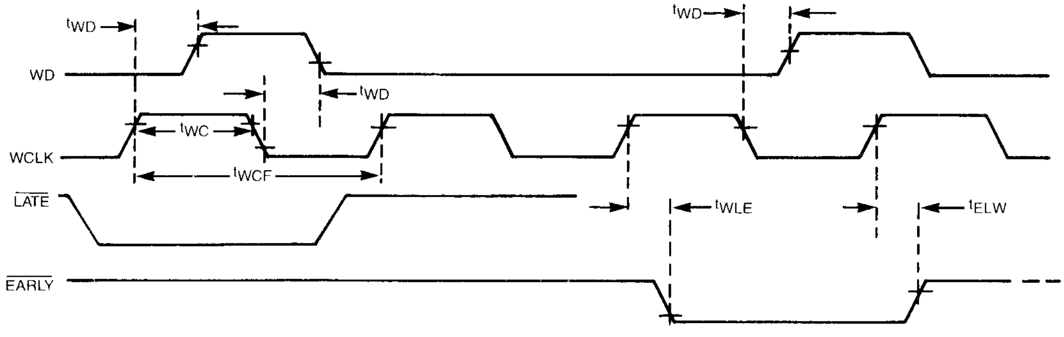
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{REV}	$\overline{\text{RE}}$ Float to $\overline{\text{RE}}$ Valid	0		100	nsec	C_L = 50 pf
t_{REB}	$\overline{\text{RE}}$ Output Pulse Width	300	400	500	nsec	See Note 4
t_{RDS}	Data Setup to $\overline{\text{RE}}$	140			nsec	
t_{RR}	$\overline{\text{RE}}$ Repetition Rate	1.2	1.6	2.0	μsec	
t_{RF}	$\overline{\text{RE}}$ Float from $\overline{\text{BCS}}$			100	nsec	C_L = 50 pf
t_{HRE}	Data Hold from $\overline{\text{RE}}$	0			nsec	



READ DATA TIMING

READ DATA TIMING **WD2010-05 WC = 5 MHz**

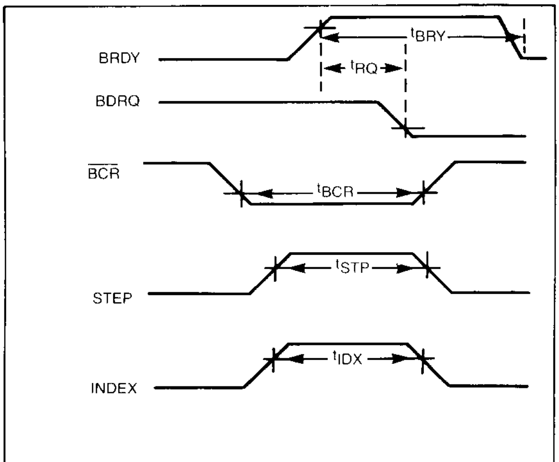
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{RCP}	RCLK Pulse Width	95		2000	nsec	50% Duty Cycle
t_{X1}	RD from RCLK Transition	0		t_{RCP}	nsec	
t_{X2}	RD to RCLK Transition	20		t_{RCP}	nsec	
t_{RD}	RD Pulse Width	40		t_{RCP}	nsec	
t_{DRN}	DRUN Pulse Width	30			nsec	
t_{RCF}	RCLK Frequency	.250	5	5.25	MHz	See Note 6



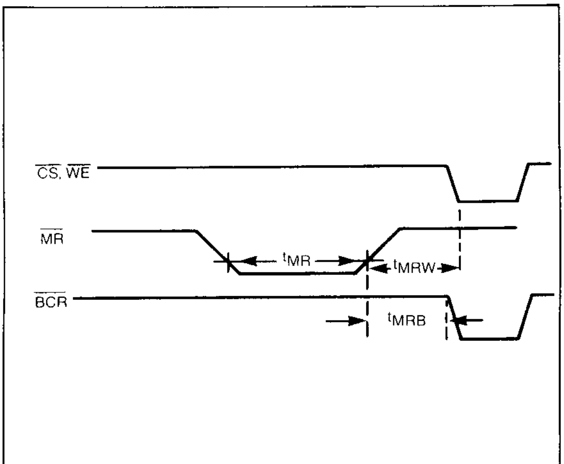
WRITE DATA TIMING

WRITE DATA TIMING WD2010-05 WC = 5 MHz

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{WC}	WCLK Pulse Width	95		2000	nsec	50% Duty Cycle
t_{WD}	Propagation Delay WCLK to WD	10		65	nsec	
t_{WLE}	WCLK to Leading $\overline{EARLY}/\overline{LATE}$	10		65	nsec	
t_{ELW}	WCLK to Trailing $\overline{EARLY}/\overline{LATE}$	10		65	nsec	
t_{WCF}	WCLK Frequency	.250	5	5.25	MHz	See Note 6



MISCELLANEOUS TIMING



MISCELLANEOUS TIMING

MISCELLANEOUS TIMING WD2010-05

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{RQ}	BDRQ Reset from BRDY	20		200	nsec	
t_{BCR}	$\overline{\text{Buffer Counter Reset}}$ Pulse Width	1.4	1.6	1.8	µsec	
t_{STP}	Step Pulse Width	1.4 7.8	1.6 8.0	8.2 8.2	µsec	See Note 2
t_{IDX}	Index Pulse Width	500			nsec	
t_{MR}	Master Reset Pulse Width	24			WC	See Note 3
t_{BRY}	BRDY Pulse Width	400			nsec	See Note 5
t_{MRB}	$\overline{\text{MR}}$ Trailing To $\overline{\text{BCR}}$	0	3.2	6.4	µsec	
t_{MRW}	$\overline{\text{MR}}$ Trailing To Host Write	6.4			µsec	

NOTES:

1. AC timing measured at V_{OH} = 2.0V, V_{OL} = 0.8V, C_L = 50 pf.
2. 1.6 µsec. is typical pulse for a step rate of 32 µsec/step. 8.0 µsec typical pulse for all other step rates. Last step pulse at 3.2 µsec/step rate up to 8.2 µsec.
3. 24 WCLK periods (4.8 µsec at 5.0 MHz).
4. 2 WCLK ± 100 ns.
5. The true to false transition of BRDY should not come sooner than 2 WCLK from true to false transition of BDRQ.
6. t_{RCF} = t_{WCF} ± 15%.
7. 2 WCLK ± 50 ns.
8. $\overline{RE}$ may precede $\overline{CS}$ if $\overline{CS}$ plus $\overline{RE}$ meets the t_{RE} width.
9. $\overline{WE}$ may precede $\overline{CS}$ if $\overline{CS}$ plus $\overline{RE}$ meets the t_{WE} width.
10. It may be desirable to connect a 1K Ω pullup resistor to pins 21-23.