EXAR

XR-16C450

T-75-37-05

Asynchronous Receiver and Transmitter (UART)

GENERAL DESCRIPTION

The XR-16C450 is an universal asynchronous receiver and transmitter with modem control signals. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 56KHz, The XR-16C450 is fabricated in an advanced 2μ CMOS process to achieve low power, and high speed requirements.

FEATURES

Pin to pin and functionally compatible to INS8250, NS16C450
Modem control signals (CTS~,RTS~, DSR~, DTR~, R1~, DCD~)
Programmable character lengths (5, 6, 7, 8)
Even, odd, or no parity bit generation and detection
Status report register
Independent transmit and receive control
TTL compatible inputs, outputs

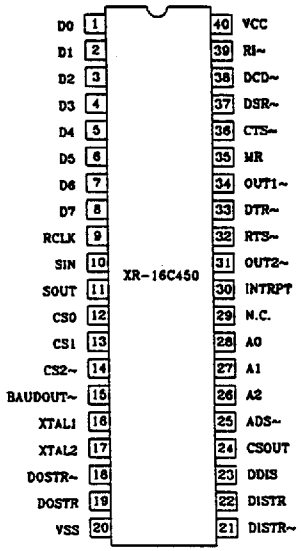
APPLICATIONS

RS232 receiver or transmitter
Serial to parallel / parallel to serial converter
Modem hand-shaking

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	7V
Voltage at any Pin	V_{SS} -0.3V to V_{CC} +0.3V
Storage Temperature	-55°C to +150°C
Power Dissipation	80 mW

PIN ASSIGNMENT



For other pin assignments, refer to the end of this datasheet

ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-16C450CP	Plastic DIP	0°C to +70°C
XR-16C450CJ	PLCC	0°C to +70°C

SYSTEM DESCRIPTION

The XR-16C450 is an improved version of the INS8250/NS16C450 UART with higher speed operating access time. The XR-16C450 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The on-board status registers will provide the error conditions, as well as type and status of the transfer operations being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the users requirements to minimize the computing required to handle the communications link. The XR- 16C450 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability.

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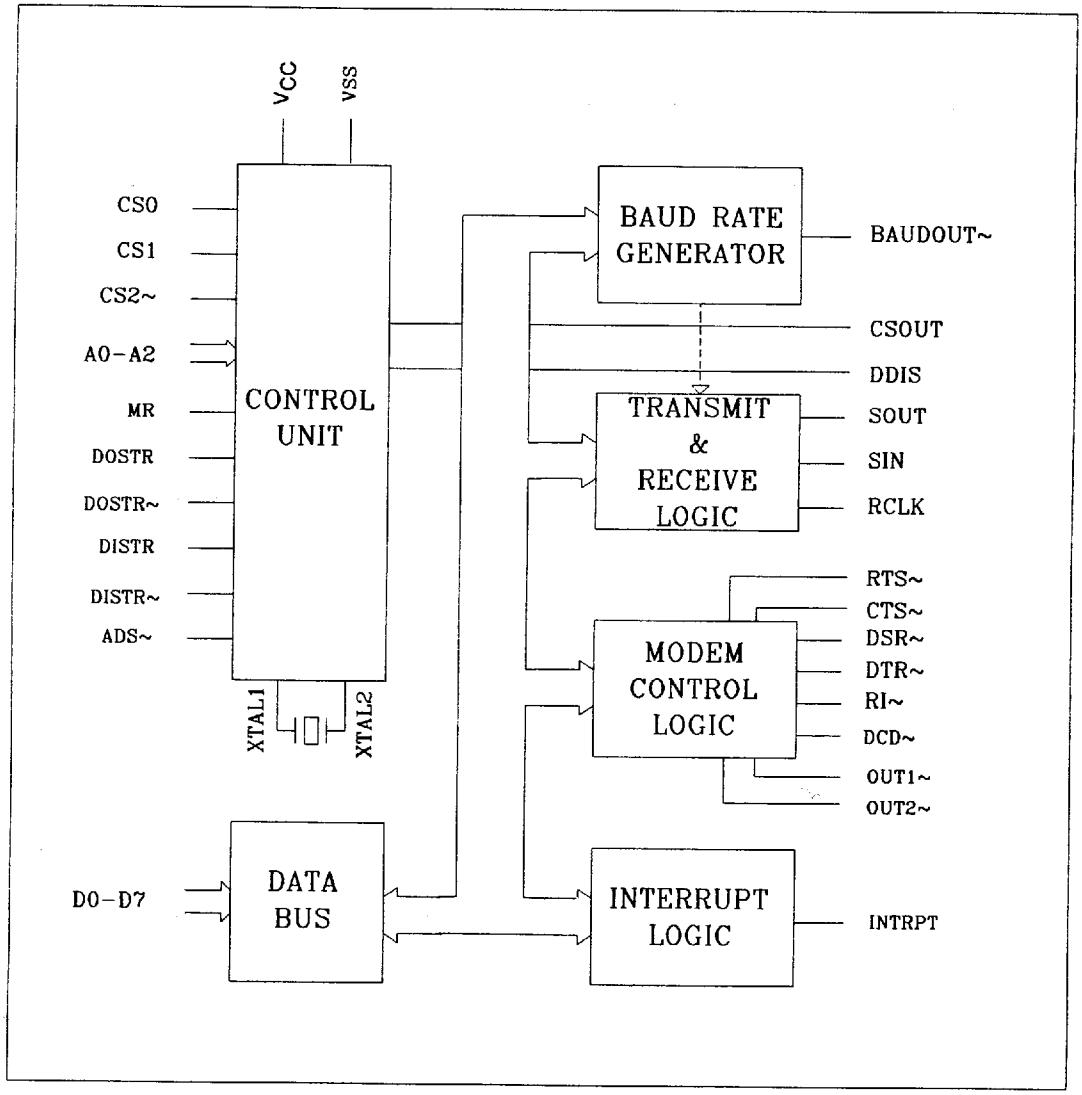
BLOCK DIAGRAM



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PIN DESCRIPTION

SYMBOL	PIN	TYPE	DESCRIPTION
D0-D7	1-8	I/O	**Bidirectional data I/0.** Eight bit, three-state data bus to transfer information to or from the CPU. D0 Is the least significant bit (LSB) of the data bus and is the first serial data bit to be received or transmitted.
RCLK	9	I	**Receive clock input.** The external clock input to the XR-16C450 receive section, as well as baud rate divisor input.
SIN	10	I	**Serial data input.** The serial Information (data) received from MODEM or RS232 to XR-16C450 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the SIN input is disabled from external connection and connected to the SOUT output internally.
SOUT	11	O	**Serial data output.** The serial data is transmitted via this pin with additional start, stop and parity bits. The SOUT will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	I	**Chip select 1 (active high).** A high at this pin (while CS1 = 1 and CS2 ~ = 0) will enable the UART / CPU data transfer operation.
CS1	13	I	**Chip select 2 (active high).** A high at this pin (while CSO = 1 and CS2 ~ = 0) will enable the UART / CPU data transfer operation.
CS2~	14	I	**Chip select 3 (active low).** A low at this pin (while CSO = 1 and CS1 = 1) will enable the UART / CPU data transfer operation.
BAUDOUT~	15	I	**Baud rate generator clock output.** This output provides the 16x clock of the internal selected baud rate.
XTAL1	16	I	**Crystal input 1 or external clock input.** A crystal (parallel resonant) can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock the internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	I	**Crystal input** 2. See XTAL1.
DOSTR~	18	I	**I/O write strobe (active low).** A low on this pin will transfer the contents of the CPU data bus to the UART.
DOSTR	19	I	**I/O write strobe.** (active high) Same as DOSTR~, but uses active high input. Note that only an active DOSTR ~ or DOSTR input is required to transfer data from CPU to XR-16C450 during write operation (while CS0 = 1, CS1 = 1 and CS2~ = 0). The unused pin should be tied to VCC or VSS(DOSTR ~ =VCC or DOSTR =VSS).
VSS	20	O	**Signal and power ground.**
DISTR~	21	I	**I/O read strobe (active low).** A low level on this pin (while CS0 = 1, CS1 = 1 and CS2 ~ = 0) will transfer the contents of the XR-16C450 data bus to the CPU.

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PIN DESCRIPTION

SYMBOL	PIN	TYPE	DESCRIPTION
DISTR	22	I	**I/O read strobe (active high).** Same as DISTR~, but uses active high input. Note that only an active DISTR~ or DISTR input is required to transfer data from XR-16C450 to CPU during read operation (while CSO = 1, CS1 = 1 and CS2 ~ = 0). The unused pin should be tied to V_{CC} or V_{SS} (DISTR ~ = V_{CC} or DISTR = V_{SS}).
DDIS~	23	O	**Drive disable (active low).** This pin goes low when CPU is reading data from XR-16C450 to disable the external transceiver or logic.
CSOUT	24	O	**Chip select out.** A high on this pin indicates that the chip has been selected by the chip select input pins.
ADS~	25	I	**Address strobe (active low).** A low on this pin will latch the state of the chip selects and addressed register. A rising edge is required if register and chip select pins are not stable during read and write operation.
A2	26	I	**Address line 2.** To select internal registers.
A1	27	I	**Address line 1.** To select internal registers.
A0	28	I	**Address line 0.** To select Internal registers.
INTRPT	30	O	**Interrupt output (active high).** This pin goes high (when enabled by the Interrupt enable register) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
OUT2~	31	O	**General purpose output (active low).** User defined output. See bit-3 of the modem control register (BIT-3 = 1 makes OUT2 ~ = 0).
RTS~	32	O	**Request to send (active low).** To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset, this pin will be set to high.
DTR~	33	O	**Data terminal ready (active low).** To indicate that XR-16C450 is ready to receive data. This pin can be controlled via the modem control regis ter (MCR bit-0). Writing a "1" to the MCR bit-0 will set the DTR~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
OUT1~	34	O	**General purpose output (active low).** User defined output. See bit-2 of modem control register (BIT-2 = 1 makes OUT1 ~ = 0).
MR	35	I	**Master reset (active high).** A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.

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PIN DESCRIPTION

SYMBOL	PIN	TYPE	DESCRIPTION
CTS~	36	I	**Clear to send (active low).** The CTS~ is a modem control input. It's startup can be tested by reading the MSR Bit-4. CTS~has no effect on the transmitter output.
DSR~	37	1	**Data set ready(active low).** A low on this pin indicates that MODEM is ready to exchange data with UART.
DCD~	38	1	**Carrier detect (active low).** A low on this pin indicates that carrier has been detected by the modem.
RI~	39	1	**Ring detect indicator (active low).** A low on this pin indicates that the modem has received a ringing signal from the telephone line.
V_{CC}	40	1	**Positive power supply input.**

PROGRAMMING TABLE

DLAB	A2	A1	A0	READ MODE	WRITE MODE
0	0	0	0	Receive Holding Register	Transmit Holding Register
0	0	0	1		Interrupt Enable Register
X	0	1	0	Interrupt Status Register	
X	0	1	1		Line Control Register
X	1	0	0		Modem Control Register
X	1	0	1	Line Status Register	
X	1	1	0	Modem Status Register	
X	1	1	1	Scratch-pad Register	Scratch-pad Register
1	0	0	0		LSB of Divisor Latch
1	0	0	1		MSB of Divisor Latch

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AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC}= 5.0V 110%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
T_1	Address strobe width	30			ns	
T_2	Address setup time	30			ns	
T_3	Address hold time	5			ns	
T_4	Chip select setup time	25			ns	
T_5	Chip select hold time	0			ns	
T_6	DISTR/DISTR ~ strobe width	75			ns	
T_7	Read cycle delay	50			ns	
T_8	Read cycle = $T_{20} + T_6 + T_7$	135			ns	
T_9	DISTR/DISTR ~ to drive to disable delay			35	ns	100 pF load
T_{10}	Delay from DISTR/DISTR ~ to data			75	ns	100 pF load
T_{11}	DISTR/DISTR ~ to floating data delay	0		50	ns	100 pF load
T_{12}	DOSTR/DOSTR ~ strobe width	50			ns	
T_{13}	Write cycle delay	55			ns	
T_{14}	Write cycle = $T_1 + T_{12} + T_{13}$	135			ns	
T_{15}	Data setup time	10			ns	
T_{16}	Data hold time	25			ns	
T_{17}	Chip select output delay from select			50	ns	100 pF load
T_{18}	Address hold time from DISTR/DISTR ~	0			ns	Note: 1
T_{19}	Chip select hold time from DISTR/DISTR ~	0			ns	Note: 1
T_{20}	DISTR/DISTR ~ delay from address	10			ns	Note: 1
T_{21}	DISTR/DISTR ~ delay from chip select	10			ns	Note: 1
T_{22}	Address hold time from DOSTR/DOSTR ~	5			ns	Note: 1
T_{23}	Chip select hold time from DOSTR/DOSTR ~	5			ns	Note: 1
T_{24}	DOSTR/DOSTR ~ delay from address	25			ns	Note: 1
T_{25}	DOSTR/DOSTR ~ delay from select	10			ns	Note: 1
T_{26}	Reset pulse width	5			ns	
T_{27}	Clock high pulse duration	140				
T_{28}	Clock low pulse duration	140				External clock
TRANSMITTER						
T_{29}	Delay from rising edge of DOSTR/DOSTR ~ to reset interrupt			75	ns	100 pF load

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SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
T_{30}	Delay from initial INT reset to transmit start	24		40	*	
T_{31}	Delay from initial Write to interrupt	16		24	*	
T_{32}	Delay from stop to next start			100	ns	
T_{33}	Delay from start bit low to interrupt high			8	*	
T_{34}	Delay from DISTR/DISTR ~ to reset interrupt			75	ns	100 pF load
MODEM CONTROL						
T_{35}	Delay from DOSTR/ DOSTR ~ to output			50	ns	100 pF load
T_{36}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{37}	Delay to reset interrupt from DISTR/DISTR~			70	ns	100 pF load
BAUD RATE GENERATOR						
N	Baud rate devisor	1		$2^{16}-1$		
T_{38}	Baud out negative edge delay			100	ns	100 pF load
T_{39}	Baud out positive edge delay			100	ns	100 pF load
T_{40}	Baud out down time	425			ns	100 pF load, Note: 2
T_{41}	Baud out up time	250			ns	100 pF load, Note: 2
RECEIVER						
T_{42}	Delay from RCLK to sample time			500	ns	
T_{43}	Delay from stop to set interrupt			1Rclk	ns	100 pF load
T_{44}	Delay from DISTR/DISTR ~ to reset interrupt			200	ns	100 pF load

Note 1: Applicable only when ADS ~ is tied low
Note 2: Fx = 3.1 MHz clock
* Baudout ~ cycle

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DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC}= 5.0V ±10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		V_{CC}	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		V_{CC}	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH} = -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	uA	
I_{CL}	Clock leakage			±10	uA	

REGISTER FUNCTIONAL DESCRIPTIONS
TRANSMIT AND RECEIVE HOLDING REGISTER (THR & RHR)

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register. Writing to this register will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set. On the falling edge of the start bit,the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input. Receiver status codes will be posted in the Line Status Register.

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XR-16C450 ACCESSIBLE REGISTERS

Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
MCR	0	0	0	loop back	OP2~	OPI~	RTS~	DTR~
LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
MSR	CD~	RI~	DSR~	CTS~	delta CD~	delta RI~	delta DSR~	delta CTS~
SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

INTERRUPT ENABLE REGISTER (IER)
The Interrupt enable register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0 = disable the receiver ready interrupt
1 = enable receiver ready interrupt

IER BIT-1:
0 = disable transmitter empty interrupt
1 = enable transmitter empty interrupt

IER BIT-2:
0 = disable receiver line status interrupt
1 = enable receiver line status interrupt

IER BIT-3:
0 = disable the modem status register interrupt
1 = enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero

INTERRUPT STATUS REGISTER (ISR)
The XR-16C450 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle, the XR-16C450 provides the highest interrupt level to be serviced by CPU, no other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level	Source of the interrupts
1	ISR (Receiver Line Status Register)
2	RXRDY (Received Data Ready)
3	TXRDY (Transmitter holding register empty)
4	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero.

LINE CONTROL REGISTER (LCR)
The Line Control Register is used to specify the asynchronous data communication format. The word length and number of the stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00=5 bits word length
01=6 bits word length
10=7 bits word length
11=8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.
0=1 stop bit, when word length=5, 6, 7, 8 bits
1=1 and 1 /2 stop bit, when word length=5 bits
1=2 stop bits, word length=6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=odd parity is generated by calculating odd number of 1's in the transmitted data, receiver also checks for same format.
1=an even parity bit is generated by calculating the number of even 1's in the transmitted or received data.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the stick parity format.
0=parity bit is forced to "1" in the transmitted and received data.
1=parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1=forces the transmitter output (SOUT) to go low to alert the communication terminal.
0=normal operating condition.

LCR BIT-7:
The internal baud rate counter latch enable(DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR ~ output to high.
1=force DTR ~ output to low.

MCR BIT-1:
0=force RTS ~ output to high.
1=force RTS ~ output to low.

MCR BIT-2:
0=set OUT1 output to high.
1=set OUT1 output to low.

MCR BIT -3:
0=set OUT2~ output to high.
1=set OUT2~ output to low.

MCR BIT -4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (SOUT) is set high (mark condition), the Receiver input (SIN), CTS~, DSR~, DCD~, and RI~ are disabled. Internally the transmitter output is connected to the receiver input and DTR~, RTS~, OUT1~ and OUT2~ are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupt are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)
This register provides the status of data transfer to the CPU.

LSR BIT-0:
0=no data in receive holding register.
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received data did not have a valid stop bit.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (SIN was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. XR-16C450 will not accept any data for transmission.
1 =transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to zero permanently.

MODEM STATUS REGISTER (MSR)
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the XR-16C450 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the XR-16C450 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the XR-16C450 has changed from a low to a high state.

MSR BIT-3:
Indicates that the DCD~ input to the XR-16C450 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS~ in the MCR during loop mode. It is the compliment of the CTS~ input.

MSR BIT-5:
This bit is equivalent to DTR~ the MCR during loop mode. It is the compliment of the DSR~ input.

MSR BIT-6:
This bit is equivalent to OUT1~ in the MCR during loop mode. It is the compliment of the RI~ input.

MSR BIT-7:
This bit is equivalent to OUT2~ in the MCR during loop mode. It is the compliment to the DCD~ input.

SCRATCH-PAD REGISTER (SR)
XR-16C450 provides a temporary data register to store 8 bits of information for variable use.

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BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86

XR-16C450 EXTERNAL RESET CONDITION TABLE:

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1, LSR BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals

SIGNALS	RESET STATE
SOUT	High
OUT1~	High
OUT2~	High
RTS~	High
DTR~	High
INT	BITS 0-3=low

TIMING DIAGRAM

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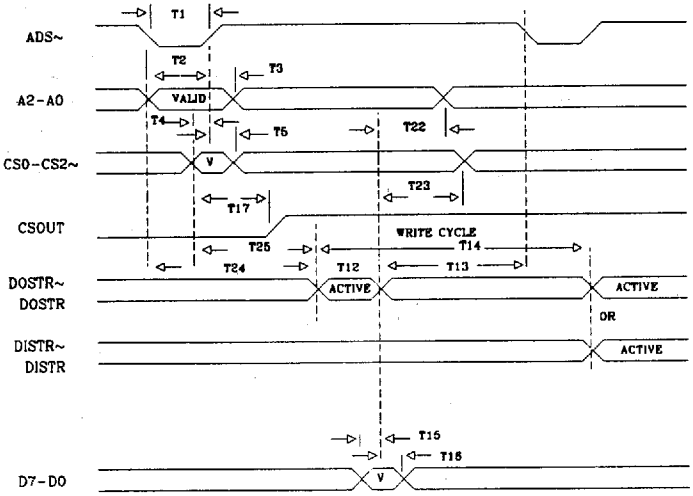
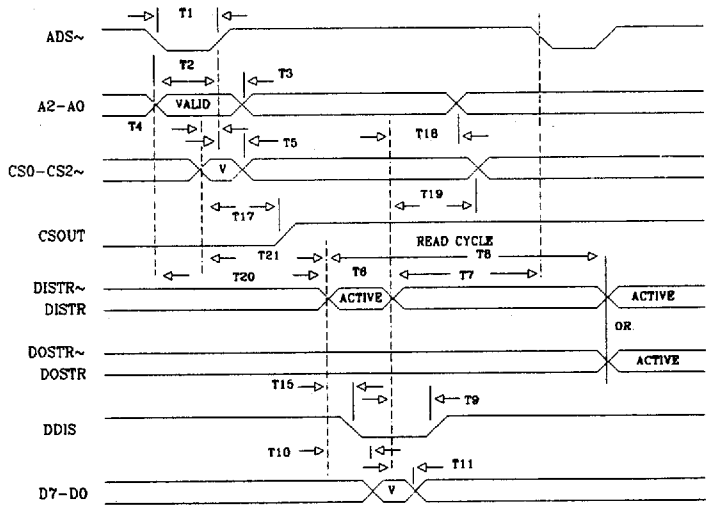
WRITE CYCLE TIMING



V = VALID
A = ACTIVE
P = PARITY

READ CYCLE TIMING



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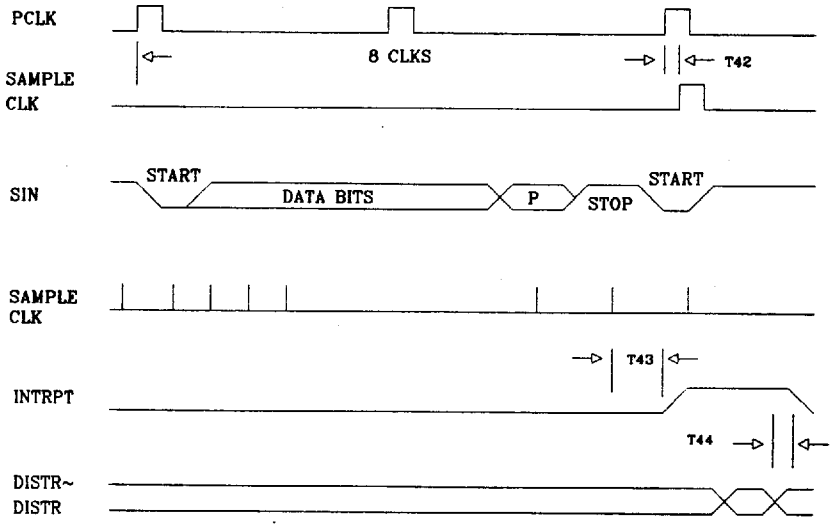
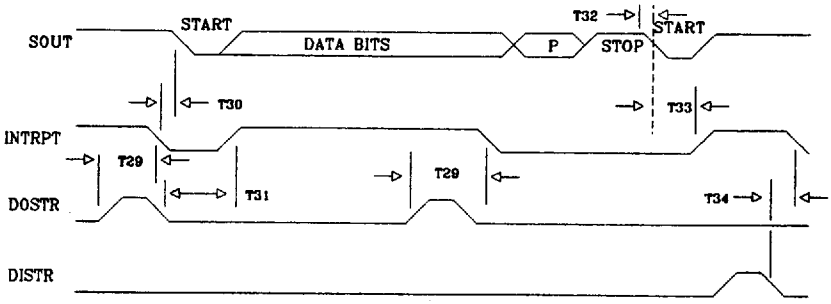
TIMING DIAGRAM

RECEIVER TIMING



TRANSMITTER TIMING



TIMING DIAGRAM

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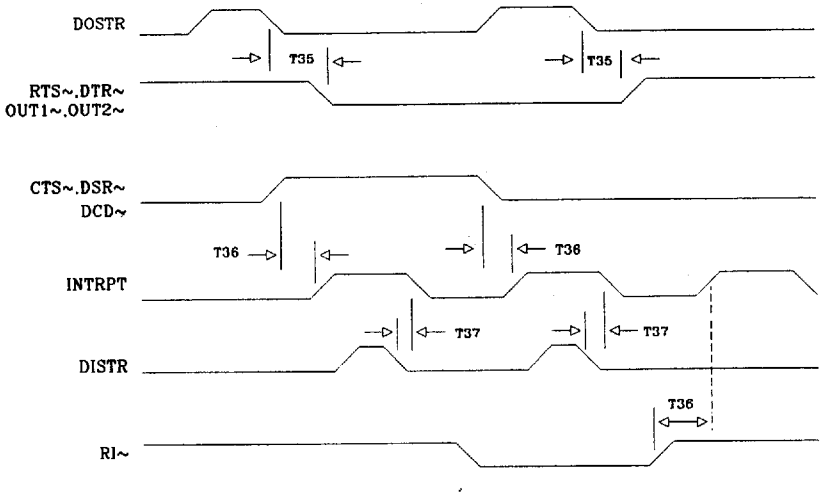
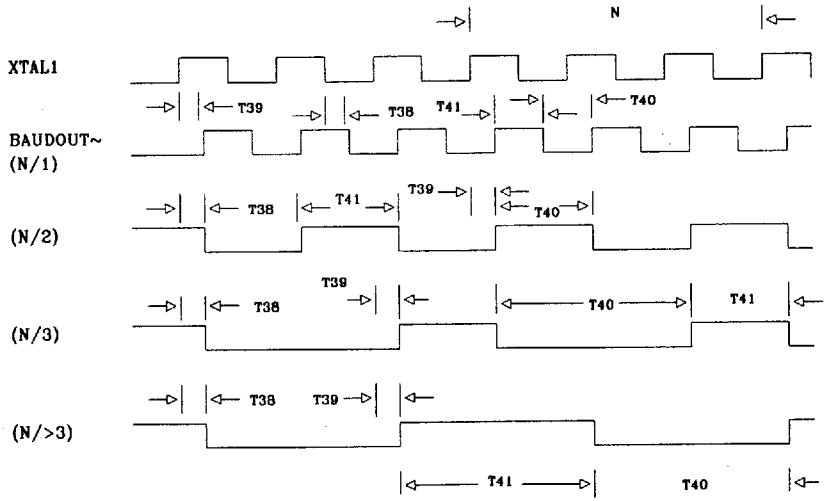
MODEM TIMING



BAUDOUT~ TIMING



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