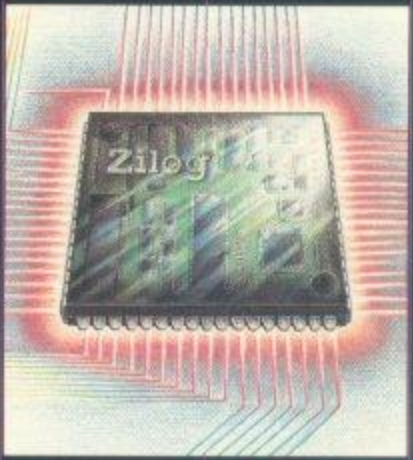
ZiLOG



COMPONENTS SHORTFORM 1989

ZiLOG Table of Contents

Introduction 1

Evolution of Product Families 1
Applications 2
Advancements in Technology 2
Peripheral Family 2

Z8 Product Family 3

Z8600 Z8 Microcomputer 5
Z8601/Z8603/Z8611/Z8613 Z8 Microcomputer 6
Z86C08 CMOS Z8 Microcontroller 7
Z86C00/C10/C20 CMOS Z8 MCU 8
Z86C11 CMOS Z8 4K ROM MCU 9
Z86C21 CMOS Z8 8K ROM MCU 10
Z86E21 CMOS One-Time-Programmable MCU 11
Z86C27 CMOS DTC Z8 Digital Television Controller 12
Z8671 Z8 MCU with Basic/Debug Interpreter 13
Z8681/82 Z8 ROMless MCU 14
Z8691 Z8 ROMless Microcomputer 15
Z86C91 CMOS ROMless Z8 Microcomputer 16
Super8 MCU ROMless, ROM, and Prototyping Device with EPROM Interface 17

Z80 Product Family 19

Z8400/Z84C00 NMOS/CMOS Z80 CPU Central Processing Unit 21
Z84C01 Z80 CPU with Clock Generator/Controller 22
Z8410/Z84C10 NMOS/CMOS Z80 DMA Direct Memory Access Controller 23
Z8420/Z84C20 NMOS/CMOS Z80 PIO Parallel Input/Output 24
Z8430/Z84C30 NMOS/CMOS Z80 CTC Counter/Timer Circuit 25
Z80440/1/2/4, Z84C40/1/2/3/4 NMOS/CMOS Z80 SIO Serial Input/Output Controller 26
Z84C50 Z80 RAM 80 Z80 CPU/2K SRAM 27
Z8470 Z80 DART Dual Asynchronous Receiver/Transmitter 28
Z84C90 CMOS Z80 KIO Serial/Parallel/Counter/Timer 29
Z80180 Z180 MPU 30
Z80280 Z80 MPU 31

Z8000 Product Family 33

Z160 CPU Central Processing Unit 35
Z765A FDC Floppy Disk Controller 36
Z16C20 CMOS Z-BUS GLU General Logic Unit 37
Z16C30 CMOS USC Universal Serial Controller 38
Z5380 SCSI Small Computer System Interface Controller 39
Z7220A A High-Performance Graphics Display Controller 40
Z8001/Z8002/Z8000 CPU Central Processing Unit 41
Z8010/Z8000 MMU Memory Management Unit 42
Z8016/Z8000 Z-DTC Direct Memory Access Transfer Controller 43
Z8030/Z8530 Z-BUS SCC/SCC Serial Communications Controller 44
Z80C30/Z85C30 Z-BUS SCC/SCC Serial Communications Controller 45
Z8036/Z8000 CIO Counter/Timer and Parallel I/O Unit 46
Z8038/Z8538 FIO FIFO Input/Output Interface Unit 47
Z8060/Z8560 FIFO Buffer Unit 48
Z8068/Z9518 Z-DCP Data Ciphering Processor 49
Z8516/Z9516 DMA Transfer Controller 50
Z8536 CIO Counter/Timer and Parallel I/O Unit 51
Z8581 Clock Generator and Controller 52

Zilog Quality and Reliability 53

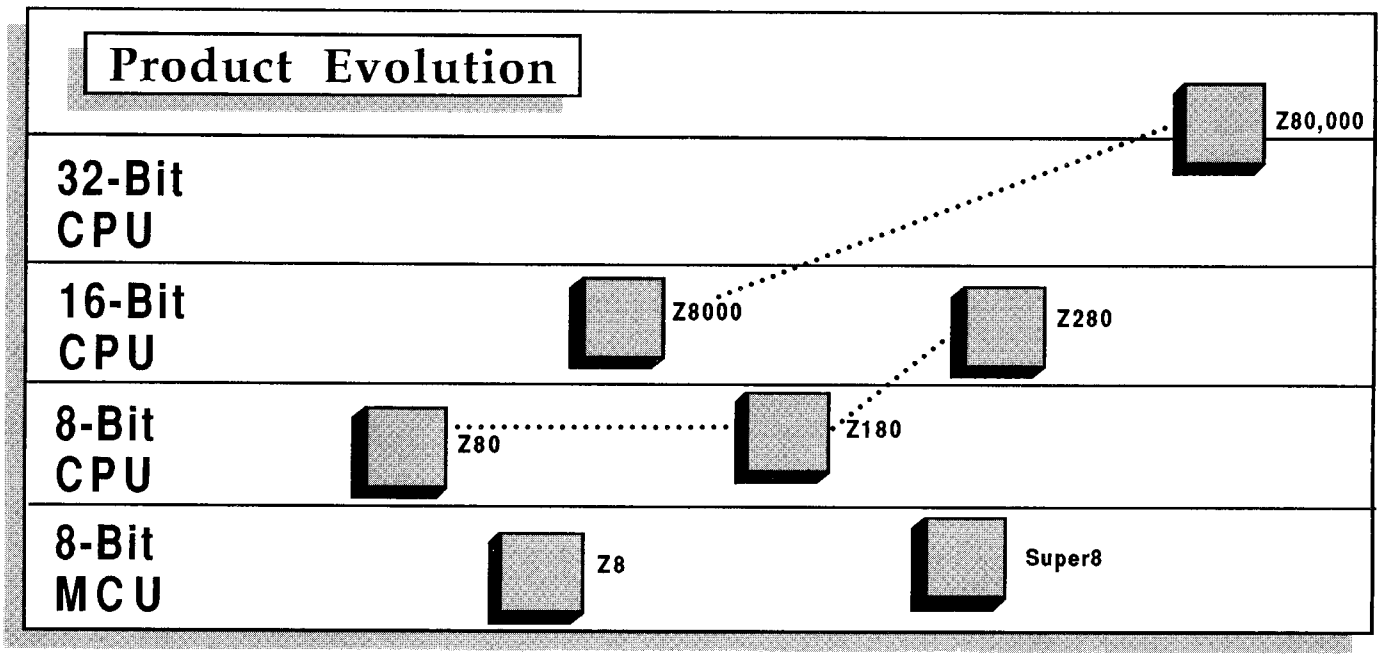
Zilog Sales Representatives and Distributors 57

Zilog Literature Guide 63

Trademarks

Z8 ® MCU	Z8002 ® CPU	Z180 ™ MPU
Z80 ® CPU	Z-BUS ® Bus	Z280 ™ MPU
Z8000 ® CPU	Super8 ™	Z80,000 ™ CPU
Z8001 ® CPU	Superintegration™	

ZiLOG Components Shortform



Introduction

Zilog was founded in 1974, and within its first year brought to market the most popular and best selling microprocessor in the world, the Z80® 8-bit microprocessor.

With the unparalleled success of the Z80 CPU, the name Zilog became synonomous with quality, design integrity, and complete company support elements that remain integral to Zilog today.

Headquartered in Campbell, California, Zilog draws upon the services and skills of the most talented high technology minds in the industry. Zilog's Nampa, Idaho manufacturing facility and assembly plant in the Philippines are the best of their size today. They provide Zilog customers with a total solution, from engineering, to production, to worldwide on-time delivery of the growing family of Zilog microprocessor and peripheral products.

Evolution of Product Families

Following on the success of the Z80 CPU, Zilog continued its record of excellence with the Z8® MCU 8-bit microcontroller, the Z8000® MPU 16-bit microprocessor, the Super8™ enhanced high-performance 8-bit microcontroller, the Z80,000™ MPU, and Z280™ 8/16-bit microprocessor that is software compatible with the Z80 CPU.

A complete line of peripheral products complement the processor families. Included in the peripheral line are such industry standards as the Z8030/8530 Serial Communications Controller, the Z8038 FIFO I/O Interface Unit (dual-port), and the Z8036/8536 CIO Counter/Timer and Parallel I/O Unit. Add to that a series of Zilog products obtained through various partnership agreements and Zilog is able to provide a stable of products unmatched in the industry. All of these fine products are supported via a network of sales offices around the world - ready to provide customers with the most complete offerings at attractive prices, and backed by Zilog's high quality and support.

Applications

Zilog offers products that meet customer needs in a wide variety of industries - in military applications such as missile guidance, communications, avionics, and artillery; in office automation with microprocessors in typewriters, copiers and facsimile machines. And, both embedded and visible reprogrammable markets for Zilog products keep expanding, with applications in industrial controllers (robotics, process control), telecommunications (modems, switching networks), automotive (dashboard displays), and consumer electronics (VCR's, cable television) markets.

Zilog Peripheral Families

	Z80	Z8000	Z8500
Z8/SUPER8		X	X
Z80	X		X
Z8000		X	
OTHER CPUs		X	X

Advancements in Technology

Zilog technology continues to pace the industry. All products are moving to CMOS with the Z280 MPU and the Z85C30 SCC, as an example of a few that are leading the way. In addition, Zilog is at the forefront of the industry in the design and manufacturing of a line of Superintegration™ products. Zilog's technology library in - cludes megacells from the industry standard Z80 CPU family, the Z8 microcontroller family and several industry standard peripherals. OTP (one-time programmable) technology was recently intro - duced. All are manufactured in Zilog's reliable n-Well 1.5-2u CMOS technology.

Support Products

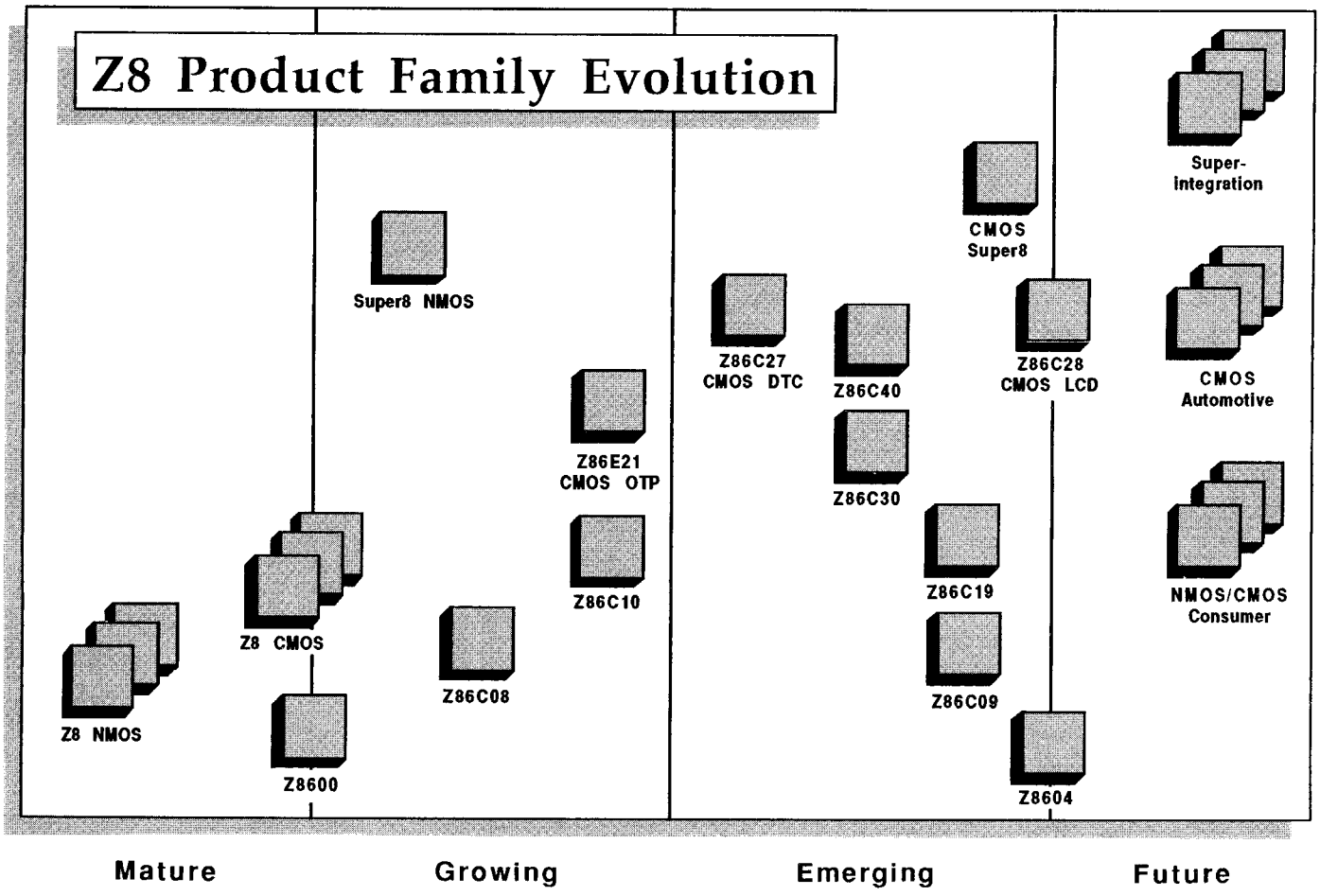
The efficient hardware and software design of a microprocessor-based application is accomplished through the use of advanced development tools. Zilog's partnerships with the industry leaders in the microprocessor development system business, ensure timely, optimal support for microprocessor and microcontrollers on a variety of host machines from IBM PC through DEC VAX.

Peripheral Functions

Functions	Device No.
Parallel I/O	Z8X36, Z8038, Z8420
Counter/Timers, Interrupt Ctrls	Z8430, Z8X36
Clock Generators	Z8581
DMA Controllers	Z8X16, Z8410
Floppy Controller	Z765A
CRT Controller	Z7220A
SCSI Interface	Z5380
Z8000 GLU	Z16C20
Serial/Parallel I/O(KIO)	Z84C90
Serial Communi- cations Ctrls	Z8X30, Z8XC30, Z16C30, Z844X

Summary

The following pages summarize our present product offering with basic features and functional block diagrams. Further details can be obtained from your nearest Zilog sales office.


Z8 Product Family Evolution
Super8 NMOS
Z86E21
CMOS OTP
Z86C10
Z8 CMOS
Z8 NMOS
Z8600
Z86C08
Z86C27
CMOS DTC
Z86C40
Z86C30
CMOS
Super8
Z86C28
CMOS LCD
Z86C19
Z86C09
Z8604
Super-
Integration
CMOS
Automotive
NMOS/CMOS
Consumer
Mature
Growing
Emerging
Future

Z8 Reference chart

Product	Pin Count	QFP	Dip	PLCC	Cerdip	Speed	Temp	Ceramic Dip	LCC	Speed	SMD	JAN
NMOS												
Z8600 MCU	28	-	X	-	-	8	S,E	-	-	-	-	-
Z8601 MCU												
2K ROM	40,44	-	X	X	X	8,12.5	S,E	-	-	-	-	-
Z8603												
PROTOPACK	40	-	X	-	-	8,12	S	-	-	-	-	-
Z8610 MCU												
4K ROM	28	-	X	-	-	8,12	S,E	-	-	-	-	-
Z8611 MCU												
4K ROM	40,44	-	X	X	-	8,12.5	S,E,M	X	-	8	-	-
Z8612 MCU												
ICU [2]	64,68	-	X	X	-	12	S	-	-	-	-	-

Cont. on next page

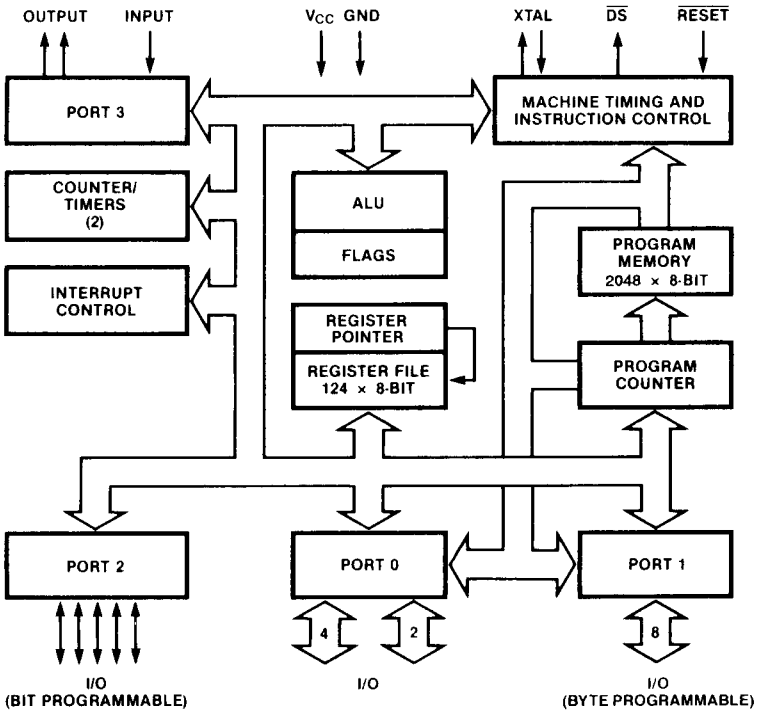
S = 0°C to +70°C E = -40°C TO 100°C
M = -55°C to 125°C

Z8 Reference chart (Continued)

Product	Pin Count	QFP	Dip	PLCC	Cerdip	Speed	Temp	Ceramic Dip	LCC	Speed	SMD	JAN
Commercial								**Military**				
Z8613 PROTOPACK	40	-	X	-	-	8,12	S	-	-	-	-	-
Z8671 MCU BASIC DEBUG	40	-	X	-	-	8	E	-	-	-	-	-
Z8680 MCU	40	-	X	-	-	4	S	-	-	-	-	-
Z8681 MCU ROMless	40,44	-	X	X	X	8,12,16	S,E,M	X	-	8	-	-
Z8682/84 MCU ROMless	40	-	X	-	-	8	S	-	-	-	-	-
Z8691 MCU ROMless	40,44	-	X	X	-	8,12	S,E	-	-	-	-	-
Z8800 SUPER8 ROMless	48,68	-	X	X	-	20	S	-	-	-	-	-
Z8801 SUPER8	44	-	-	X	-	20	S	-	-	-	-	-
Z8820 SUPER8 8K ROM	48,68	-	X	X	-	20	S	-	-	-	-	-
Z8821 SUPER8 8K ROM	44	-	-	X	-	20	S	-	-	-	-	-
Z8874 FORTH	48,68	-	X	X	-	20	S	-	-	-	-	-
Z8884 SUPER8 ICE [1]	84	-	-	-	-	20	S	-	-	-	-	-
CMOS												
Z86C00 MCU 2K ROM	28	-	X	-	-	12	S	-	-	-	-	-
Z86C08 MCU	18	-	X	-	-	8,12	S,E	-	-	-	-	-
Z86C10 MCU	28	-	X	-	-	12	S	-	-	-	-	-
Z86C11 MCU	40,44	X	X	X	-	12,16,20	S,E	-	-	-	-	-
Z86C12 MCU [1]	84	-	-	-	-	16	S	-	-	-	-	-
Z86C20 MCU	28	-	X	-	-	8,12	S	-	-	-	-	-
Z86C21 MCU	40,44	X	X	X	-	12,16,20	S,E	-	-	-	-	-
Z86E21 MCU	40,44	-	X	X	-	12,16	S	-	-	-	-	-
Z86C91 MCU	40,44	X	X	X	-	12,16,20	S,E	-	-	-	-	-

[1] Available in 84-pin PGA only
[2] Available in 64-pin Ceramic DIP

S = 0°C to +70°C E = -40°C TO 100°C
M = -55°C to 125°C



FEATURES

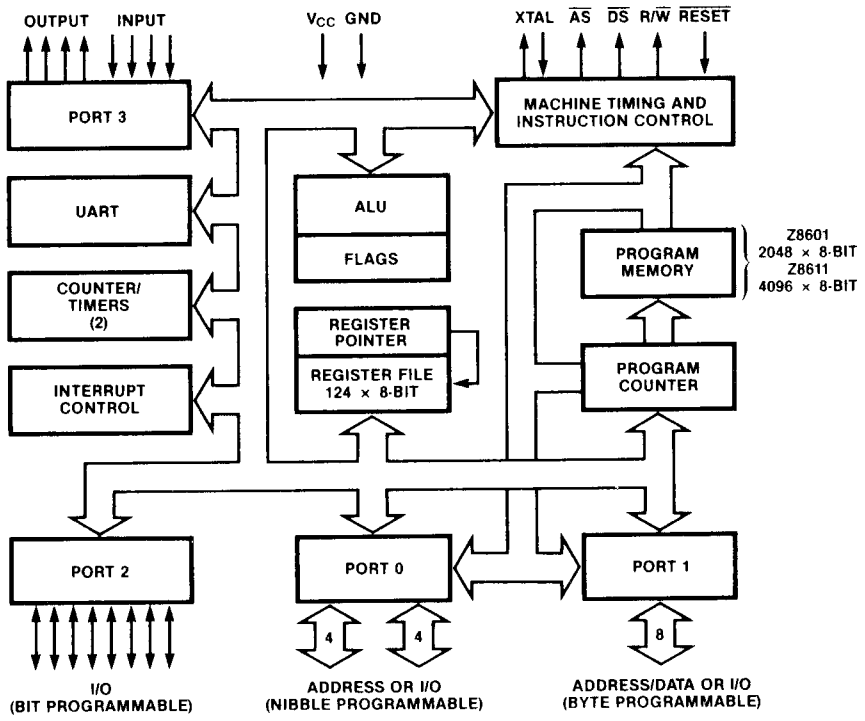
- Complete microcomputer, 2K bytes of ROM, 124 bytes of RAM, and 22 I/O lines.
- 142-byte register file, including 124 general purpose registers, four I/O port registers, and 14 status and control registers.
- Vectored, priority interrupts for I/O and counter/timers.
- Two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
- Register Pointer so that short, fast instuctions can access any one of the nine working register groups.
- On-chip oscillator that accepts crystal or external clock drive.
- 8 MHz.
- Single +5V power supply, all pins TTL-compatible.
- Average instruction execution time of 2.2 μ, minimum 1.5 μ.

GENERAL DESCRIPTION

The Z8600 microcomputer introduces a new level of sophistication to single-chip architecture. Compared to earlier single-chip microcmputers, the Z8600 offers faster execution, more efficient use of memory, more sophisticated interrupt, input/output, and bit manipulation capabilities, and easier system expansion.

Under program control, the MCU can be tailored to the needs of its user. It can be configured as a stand-alone microcomputer with 2K bytes of internal ROM. In all configurations, a large number of pins remain available for I/O. The MCU is offered in a 28-pin Dual-In-Line Package(DIP).

Z8601/Z8603/Z8611/Z8613 Z8® Microcomputer



FEATURES

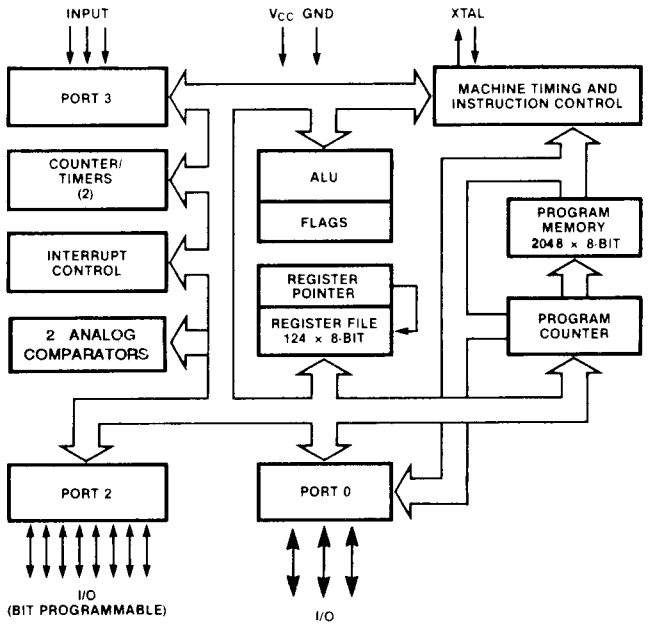
- Complete microcomputer, 2K (8601) or 4K (8611) bytes of ROM, 124 bytes of RAM, 32 I/O lines, and up to 62K (8601) or 60K (8611) bytes addressable external space each for program and data memory.
- 144-byte register file, including 124 general purpose registers, four I/O port registers, and 16 status and control registers.
- Average instruction execution time of 1.5 μs, maximum of 1 μs.
- Vectored, priority interrupts for I/O, counter/timers, and UART.
- Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
- Register Pointer so that short, fast instructions can access any of nine working register groups in 1 μs.
- On-chip oscillator which accepts crystal or external clock drive.
- Single +5V power supply, all pins TTL compatible.
- 8 and 12.5 MHz.

GENERAL DESCRIPTION

The Z8 microcomputer introduces a new level of sophistication to single-chip architecture. Compared to earlier single-chip microcomputers, the Z8 offers faster execution, more efficent use of memory, more sohisticated interrupt, input/output, and bit-manipulation capabilites, and easier system expansion.

Under program control, the Z8 can be tailored to the needs of its user. It can be configured as a stand-alone microcomputer with 2K or 4K bytes of internal ROM, a traditional microprocessor that manages up to 124K bytes of external memory, or a parallel-processing element in a system with other processors and peripheral controllers linked by the Z-BUS®. In all configurations, a large number of pins remain available for I/O.

The Z8603 and Z8613 protopacks are used for prototype development and production of mask-programmed applications. The protopacks are ROMless versions of the Z8601 (Z8603) and Z8611 (Z8613) housed in a pin compatible 40-pin piggyback package.



FEATURES

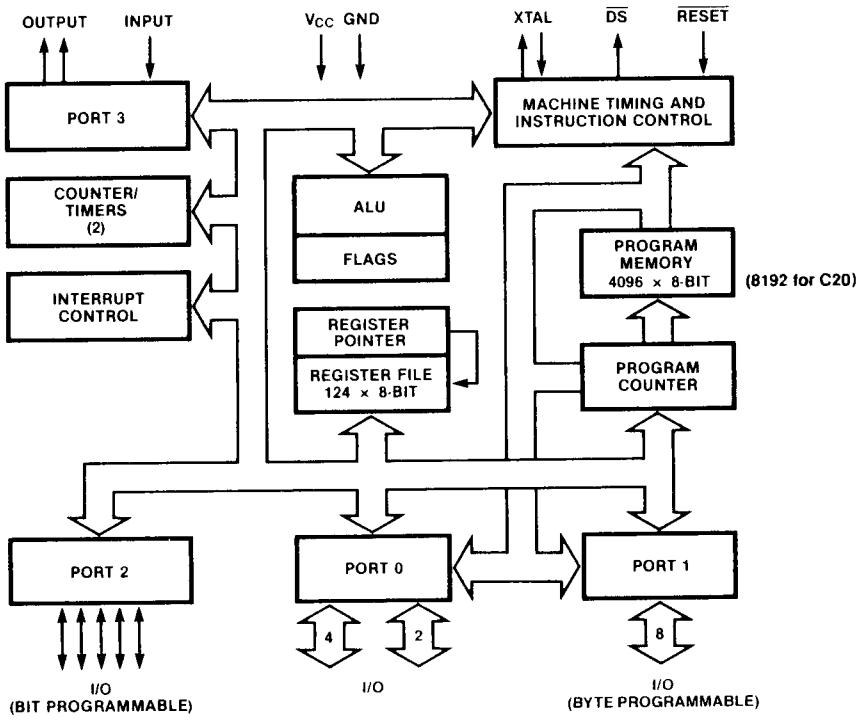
- Complete microcomputer with 18-pin package, 14 I/O lines, and 2K bytes of on-chip ROM.
- 141-byte register file, including 124 general purpose 8-bit registers, 3 I/O port registers, and 14 status and control registers.
- Two programmable 8-bit counter/timers, each with a 6-bit programmble prescaler.
- On-chip oscillator that accepts a crystal or external clock drive.
- 2 Volt "BROWN OUT" protection.
- Two analog comparators.
- Register pointer so that short,fast instructions access any one of the eight working register groups.
- Internal power on reset.
- Standby modes: Halt and Stop.
- 8,12 MHz.
- CMOS process.
- 3 Volt Operation.

GENERAL DESCRIPTION

The 86C08 is a 2K ROM version of the Z8 single-chip microcomputer housed in a 18-pin DIP. It offers all the outstanding features of the Z8 family architecture in a low cost plastic DIP for price and size sensitive designs.

Flexible I/O with low power (15mA max, 5mA Halt, 10µA STOP operation make this an ideal microcomputer for hand-held and consumer applications. It has instruction compatibility with the entire Z8 family for easy software migration.

Z86C00/C10/C20 CMOS Z8® MCU

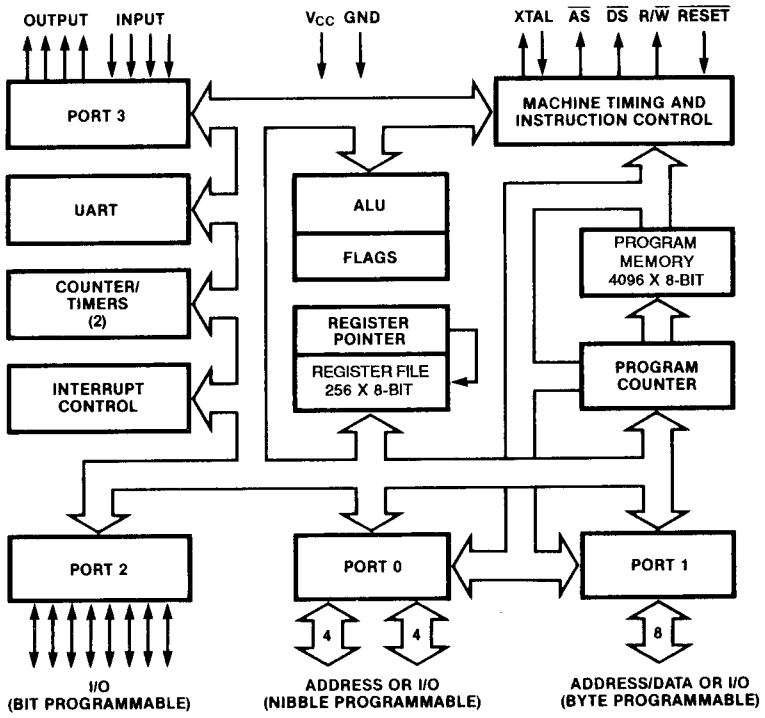


FEATURES

- Complete microcomputer, 2K (86C00), 4K (86C10), or 8K (86C20), bytes of ROM, 124 bytes of RAM, and 22 I/O lines.
- 142-byte register file, including 124 general-purpose registers, four I/O port registers, and 14 status and control registers.
- Average instruction execution time of 1.5 μs, maximum of 2.8 μs.
- Vectored, priority interrupts for I/O and counter/timers.
- Two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
- Register Pointer so that short, fast instuctions can access any of nine working-register groups in 1.0 us.
- On-chip oscillator which accepts crystal, external clock drive, or ceramic resonator.
- Standby modes: Halt and Stop.
- Single + 5V power supply, all pins TTL-compatible.
- 12 MHz.
- CMOS process.

GENERAL DESCRIPTION

Z86C00/C10/C20 microcomputers introduce a new level of sophistication to single-chip architecture. Compared to earlier single-chip microcomputers, the 86C10/C20 offers faster execution, more efficient use of memory, more sophisticated interrupt, input/output, and bit manipulation capabilities, and easier system expansion.



FEATURES

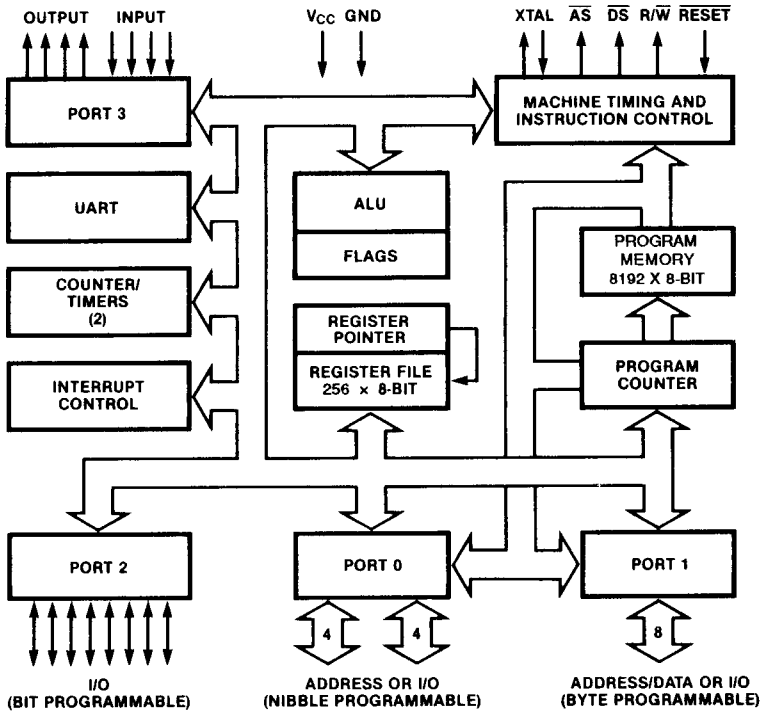
- Complete microcomputer, 4K bytes of ROM, 236 bytes of RAM, 32 I/O lines, and up to 60K bytes addressable external space each for program and data memory.
- 256-byte register file, including 236 general purpose registers, four I/O port registers, and 16 status and control registers.
- Vectored, priority interrupts for I/O, counter/timers, and UART.
- Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
- Register Pointer so that short, fast instructions can access any of 16 working-register groups in 1.5 μs.
- On-chip oscillator which accepts crystal, or external clock drive, or ceramic resonator.
- Standby modes: Halt and Stop.
- Single + 5V power supply, all pins TTL-compatible.
- 12, 16, and 20 MHz.
- CMOS process.

GENERAL DESCRIPTION

The Z86C11 microcomputer introduces a new level of sophistication to single-chip architecture. Compared to earlier single-chip microcomputers, the Z86C11 offers faster execution; more efficient use of memory, more sophisticated interrupt, input/output, and bit-manipulation capabilities; and easier system expansion.

Under program control, the Z86C11 can be tailored to the needs of its user. It can be configured as a stand-alone microcomputer with 4K bytes of internal ROM, a traditional microprocessor that manages up to 120K bytes of external memory, or a parallel-processing element in a system with other processors and peripheral controllers linked by the Z-BUS®. In all configurations, a large number of pins remain available for I/O.

Z86C21 CMOS Z8® 8K ROM MCU



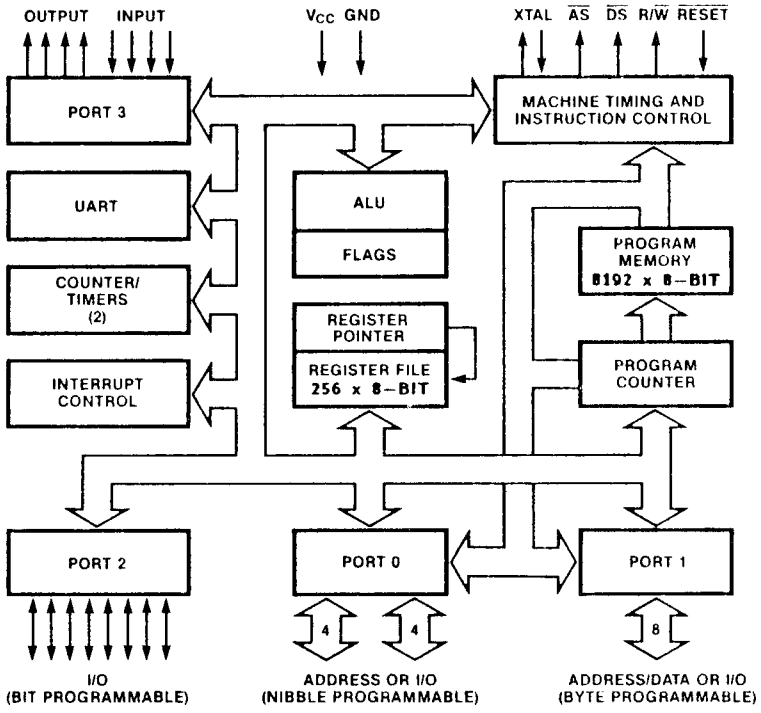
FEATURES

- Complete microcomputer, 8K bytes of ROM, 236 bytes of RAM, 32 I/O lines, and up to 56K bytes addressable external space each for program and data memory.
- 256-byte register file, including 236 general purpose registers, 4 I/O port registers, and 16 status and control registers.
- Minimum instruction execution time of 0.6 μs, average of 1.0 μs.
- Vectored, priority interrupts for I/O, counter/timers, and UART.
- Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
- Register Pointer so that short, fast instructions can access any of 16 working-register groups in .6 μs.
- On-chip oscillator which accepts crystal or external clock drive.
- Standby modes: Halt and Stop.
- Single +5V power supply, all pins TTL-compatible.
- 12, 16, and 20 MHz.
- CMOS process.

GENERAL DESCRIPTION

The Z86C21 microcomputer introduces a new level of sophistication to single-chip architecture. Compared to earlier single-chip microcomputers, the Z86C21 offers faster execution, more efficient use of memory, more sophisticated interrupt, input/output, and bit manipulation capabilities, and easier system expansion.

Under program control, the Z86C21 can be tailored to the needs of its user. It can be configured as a stand-alone microcomputer with 8K bytes of internal ROM, a traditional microprocessor that manages up to 120K bytes of external memory, or a parallel-processing element in a system with other processors and peripheral controllers linked by the Z-BUS ®. In all configurations, a large number of pins remain available for I/O.



FEATURES

- Complete microcomputer, 8K bytes of OTP memory, 236 bytes of RAM, 32 I/O lines, and up to 56K bytes addressable external space each for program and data memory.
- 256-byte register file, including 236 general purpose registers, 4 I/O port registers, and 16 status and control registers.
- Minimum instruction execution time of 0.6 μs, average of 1.0 μs.
- Vectored, priority interrupts for I/O, counter/timers, and UART.
- Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
- Register Pointer so that short, fast instructions can access any of 16 working-register groups in .6 μs.
- On-chip oscillator which accepts crystal, ceramic resonator, or external clock drive.
- Standby modes: Halt and Stop.
- Single +5V power supply, all pins TTL-compatible.
- 12,16 MHz.
- CMOS process.
- ROM/RAM protect.

GENERAL DESCRIPTION

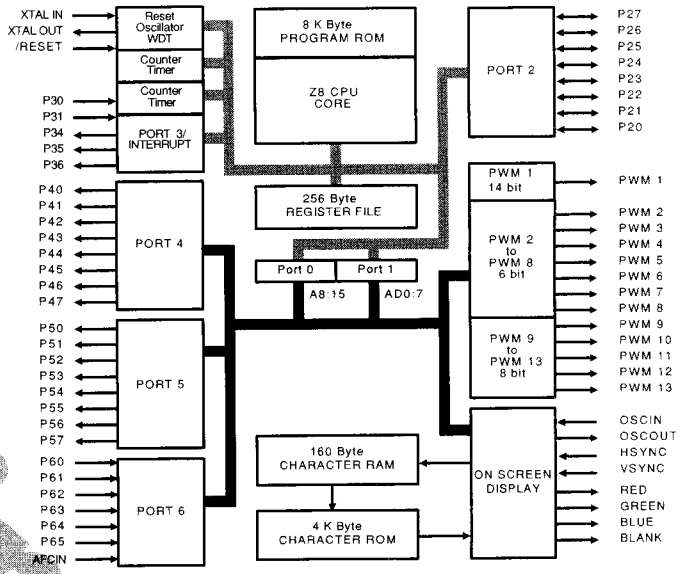
The Z86E21 microcomputer introduces a new level of sophistication to single-chip architecture. Compared to earlier single-chip microcomputers, the Z86E21 offers faster execution, more efficient use of memory, more sophisticated interrupt, input/output, and bit manipulation capabilities, and easier system expansion.

Under program control, the Z86E21 can be tailored to the needs of its user. It can be configured as a stand-alone microcomputer with 8K bytes of internal ROM, a traditional microprocessor that manages up to 120K bytes of external memory, or a parallel-processing element in a system with other processors and peripheral controllers linked by the Z-BUS ®. In all configurations, a large number of pins remain available for I/O.

Z86C27 CMOS DTC Z8 Digital Television Controller

FEATURES

- Z8 core-based CMOS 64 SDIP controller for consumer television applications.
- Internal Reset/Low Voltage Detection.
- Port5 (8 bit LED drive output) and Port6 (6-bit input and 3 state comparator AFC input) memory mapped I/O ports.
- ON Screen Display Controller.
- Programmable row character color, row background color, row fringe color, frame background color, frame position and character size.
- 128 character set displayed as 8 rows by 20 columns capable of supporting Roman, Chinese, Korean and Japanese high resolution characters.
- 160 x 7 bit video RAM.
- 4K x 6 bit character generator ROM.
- 5 to 7 Mhz on chip L-C oscillator for character dot clock.
- 1 Pulse Width Modulator (14 bit resolution) for voltage synthesis tuner control.



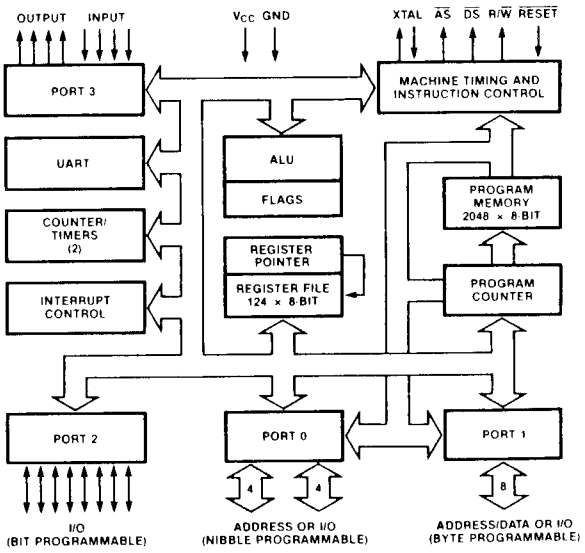
- 5 Pulse Width Modulators (8-bit resolution) for picture control.
- 7 Pulse Width Modulators (6-bit resolution) for audio control.

GENERAL DESCRIPTION

The Z86C27 and Z86C97 are CMOS Application Specific Standard Product microcomputers that integrate specialized peripheral functions (normally provided by external components) for the control of color television related products. Utilizing Zilog's advanced Superintegration™ design methodology, these devices provide an ideal cost, performance and reliability solution for consumer and industrial television applications.

The devices have an 8 bit internal data path controlled by a Z8 microcontroller core with 256 bytes of register space. On-chip peripherals include a two channel Counter/Timer, an On-Screen Display video controller, a 13 channel Digital-to-Analog converter and comprehensive Input/Output ports. The Z86C27 is the mask-ROM high volume production device embedded with a custom (customer supplied) program of up to 8 K bytes in size. The Z86C97 is the ROM-less version for prototyping and low volume production.

Z8® MCU with BASIC/Debug Interpreter Z8671



FEATURES

- The Z8671 MCU is a complete microcomputer preprogrammed with a BASIC/Debug interpreter. Interaction between the interpreter and its user is provided through an on-board UART.
- BASIC/Debug can directly address the Z8671's internal registers and all external memory. It provides quick examination and modification of any external memory location or I/O port.
- The BASIC/Debug interpreter can call machine language subroutines to increase execution speed.
- The Z8671's auto start-up capability allows a program to be executed on power-up or Reset without operator intervention.
- Single +5V power supply, all I/O pins TTL-compatible.
- 8 MHz.

GENERAL DESCRIPTION

The Z8671 Single-Chip Microcomputer (MCU) is one of a line of preprogrammed chips—in this case with a BASIC/Debug interpreter in ROM—offered by Zilog. As a member of the Z8 Family of microcomputers, it offers the same abundance of resources as the other Z8 microcomputers.

Because the BASIC/Debug interpreter is already part of the chip circuit, programming is made much easier. The Z8671 MCU thus offers a combination of software and hardware that is ideal for many industrial control applications. The Z8671 MCU allows fast hardware tests and bit-by-bit examination and modification of memory location, I/O ports, or registers. It also allows bit manipulation and logical operations. A self-contained line editor supports interactive debugging, further speeding up program development.

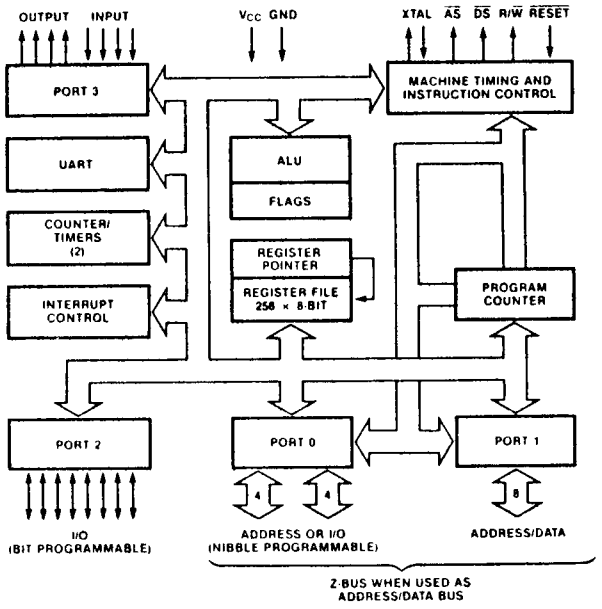
The BASIC/Debug interpreter, a subset of Dartmouth BASIC, operates with three kinds of memory: on-chip registers and external ROM or RAM. The BASIC/Debug interpreter is located in the 2K bytes of on-chip ROM.

Additional features of the Z8671 MCU include the ability to call machine language subroutines to increase execution speed and the ability to have a program execute on power-up or Reset, without operator intervention.

Maximum memory addressing capabilities include 62K bytes of external program memory and 62K bytes of data memory with program storage beginning at location 800_H. This provides up to 124K bytes of useable memory space. Very few 8-bit microcomputers can directly access this amount of memory.

Each Z8671 Microcomputer has 32 I/O lines, a 144-byte register file, an on-board UART, and two counter/timers.

Z8681/82 Z8® ROMless MCU



FEATURES

- Complete microcomputer, 24 I/O lines, and up to 64K bytes of addressable external space each for program and data memory.
- 143-byte register file, including 124 general purpose registers, 3 I/O port registers, and 16 status and control registers.
- Vectored, priority interrupts for I/O, counter/timers, and UART.
- On-chip oscillator that accepts crystal or external clock drive.
- Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
- Register Pointer so that short, fast instructions can access any one of the nine working-register groups.
- Single +5V power supply, all I/O pins TTL compatible.
- Z8681/82 available in 8 MHz. Z8681 also available in 12 and 16 MHz.

GENERAL DESCRIPTION

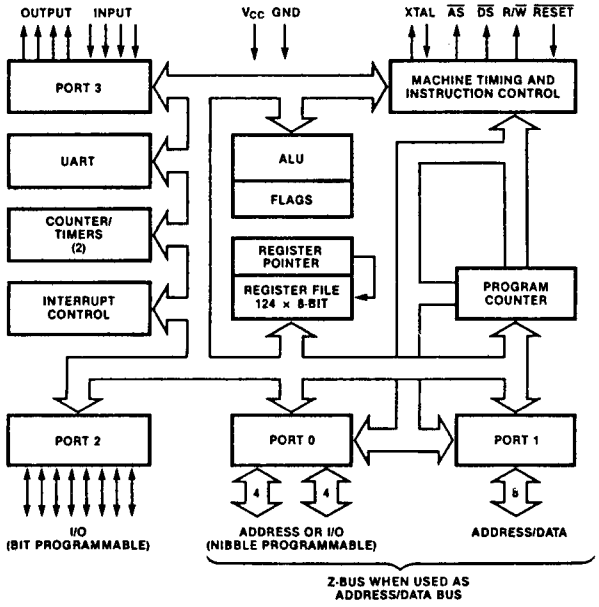
The Z8681 and Z8682 are ROMless versions of the Z8 single-chip microcomputer. These products differ only slightly and can be used interchangeably with proper system design to provide maximum flexibility in meeting price and delivery needs.

The Z8681/82 offers all the outstanding features of the Z8 family architecture except an on-chip program ROM. Use of external memory rather than a preprogrammed ROM enables this Z8 microcomputer to be used in low volume applications or where code flexibility is required.

The Z8681/82 can provide up to 16 output address lines, thus permitting an address space of up to 64K bytes of data or program memory. Eight address outputs (AD0-AD7) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A8-A15.

Available address space can be doubled (up to 128K bytes for the Z8681 and 124K bytes for the Z8682) by programming bit 4 of Port 3 (P34) to act as a data memory select output ($\overline{DM}$). The two states of $\overline{DM}$ together with the 16 address outputs can define separate data and memory address spaces of up to 64K/62K bytes each.

There are 143 registers located on-chip organized as 124 general purpose registers, 16 control and status registers, and three I/O port registers. This register file can be divided into nine groups of 16 working registers each. Configuring the register file in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly.



FEATURES

- Complete microcomputer, 24 I/O lines, and up to 64K bytes of addressable external space each for program and data memory.
- 143-byte register file, including 124 general purpose registers, 3 I/O port registers, and 16 status and control registers.
- Vectored, priority interrupts for I/O, counter/timers, and UART.
- On-chip oscillator that accepts crystal or external clock drive.
- Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
- Register Pointer so that short, fast instructions can access any one of the nine working-register groups.
- Single + 5V power supply, all I/O pins TTL compatible.
- **8 MHz and 12 MHz versions.**

GENERAL DESCRIPTION

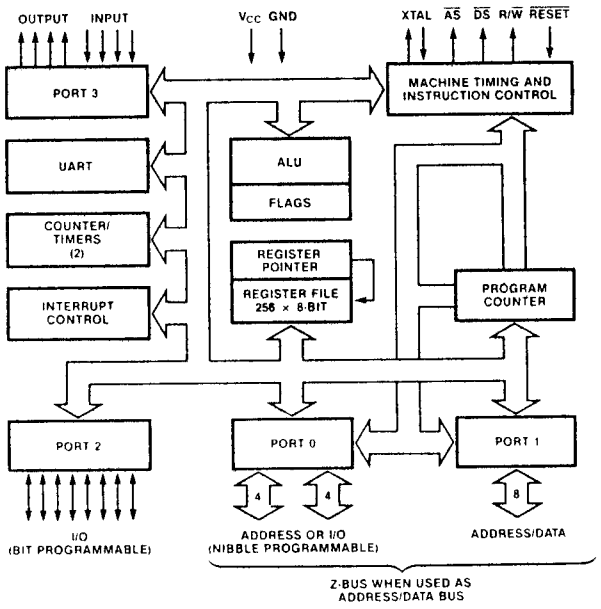
The Z8691 is a ROMless version of the Z8 single-chip microcomputer. The Z8691 offers all the outstanding features of the Z8 family architecture except an on-chip program ROM. Use of external memory rather than a preprogrammed ROM enables this Z8 microcomputer to be used in low volume applications or where code flexibility is required.

The Z8691 can provide up to 16 output address lines, thus permitting an address space of up to 64K bytes of data or program memory. Eight address outputs (AD_0-AD_7) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A_8-A_{15}.

Available address space can be doubled (up to 128K bytes) by programming bit 4 of Port 3 ($P3_4$) to act as a data memory select output ($\overline{DM}$). The two states of $\overline{DM}$ together with the 16 address outputs can define separate data and memory address spaces of up to 64K bytes each.

There are 143 registers located on-chip organized as 124 general purpose registers, 16 control and status registers, and three I/O port registers. This register file can be divided into nine groups of 16 working registers each. Configuring the register file in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly.

Z86C91 CMOS ROMless Z8®Microcomputer



FEATURES

- Complete microcomputer, 24 I/O lines, and up to 64K bytes of addressable external space each for program and data memory.
- 256-byte register file, including 236 general purpose registers, 3 I/O port registers, and 16 status and control registers.
- Vectored, priority interrupts for I/O, counter/timers, and UART.
- On-chip oscillator that accepts crystal or external clock drive.
- Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
- Register Pointer so that short, fast instructions can access any one of the sixteen working-register groups.
- Single +5V power supply, all I/O pins TTL compatible.
- **12, 16, and 20 MHz.**
- CMOS process.
- **Two Low-power Standby Modes, STOP and Halt.**

GENERAL DESCRIPTION

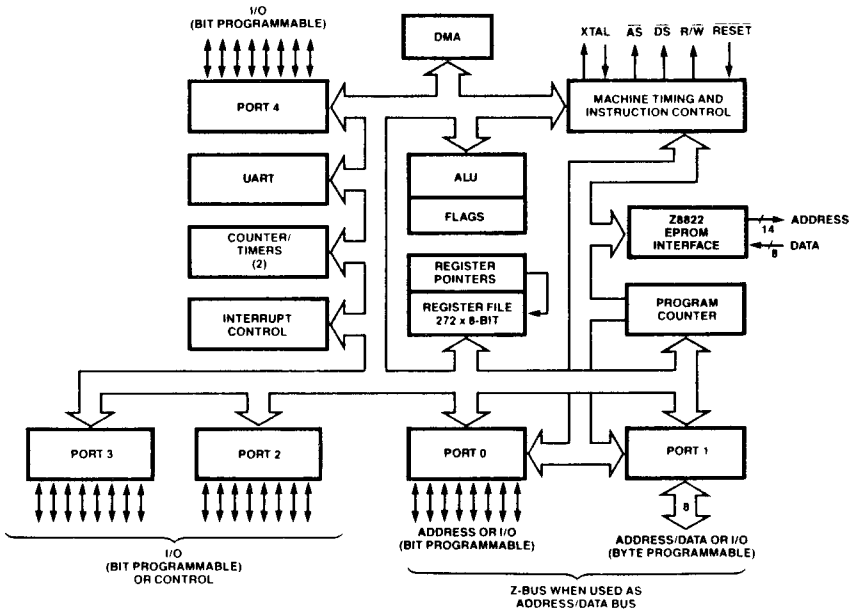
The Z86C91 is a CMOS ROMless version of the Z8 single-chip microcomputer. It offers all the outstanding features of the Z8 family architecture except an on-chip program ROM. Use of external memory rather than a preprogrammed ROM enables this Z8 microcomputer to be used in applications where code flexibility is required.

The Z86C91 can provide up to 16 output address lines, thus permitting an address space of up to 64K bytes of data or program memory. Eight address outputs (AD_0-AD_7) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A_8-A_{15}.

Available address space can be doubled (up to 128K bytes) by programming bit 4 of Port 3 ($P3_4$) to act as a data memory select output ($\overline{DM}$). The two states of $\overline{DM}$ together with the 16 address outputs can define separate data and memory address spaces of up to 64K bytes each.

There are 256 registers located on-chip organized as 236 general purpose registers, 16 control and status registers, and three I/O port registers. This register file can be divided into sixteen groups of 16 working registers each. Configuring the register file in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly.

MCU ROMless, ROM, and Prototyping Device with EPROM Interface **Super8**



FEATURES

- Improved Z8® instruction set includes multiply and divide instructions, Boolean and BCD operations.
- Additional instructions support threaded-code languages, such as "Forth."
- **352 byte registers, including 272 general purpose registers, and 80 mode and control registers.**
- Addressing of up to 128K bytes of memory **(Z8800 ROMless).**
- Two register pointers allow use of short and fast instructions to access register groups within 600 nsec.
- Direct Memory Access controller (DMA).
- Two 16-bit counter/timers.
- Up to 32 bit-programmable and 8 byte-programmable I/O lines, with 2 handshake channels.
- Interrupt structure supports:
  - 27 interrupt sources
  - 16 interrupt vectors (2 reserved for future versions)
  - 8 interrupt levels
  - Servicing in 600 nsec. (1 level only)
- Full-duplex UART with special features.
- On-chip oscillator.
- 20 MHz clock.
- 8K byte ROM for Z8820.

GENERAL DESCRIPTION

The Zilog Super8 single-chip MCU can be used for development and production. It can be used as an I/O or memory-Intensive computer, or configured to address external memory while still supporting many I/O lines.

The Super8 features a full-duplex universal asynchronous receiver/transmitter (UART) with on-chip baud rate generator, two programmable counter/timers, a direct memory access (DMA) controller, and an on-chip oscillator.

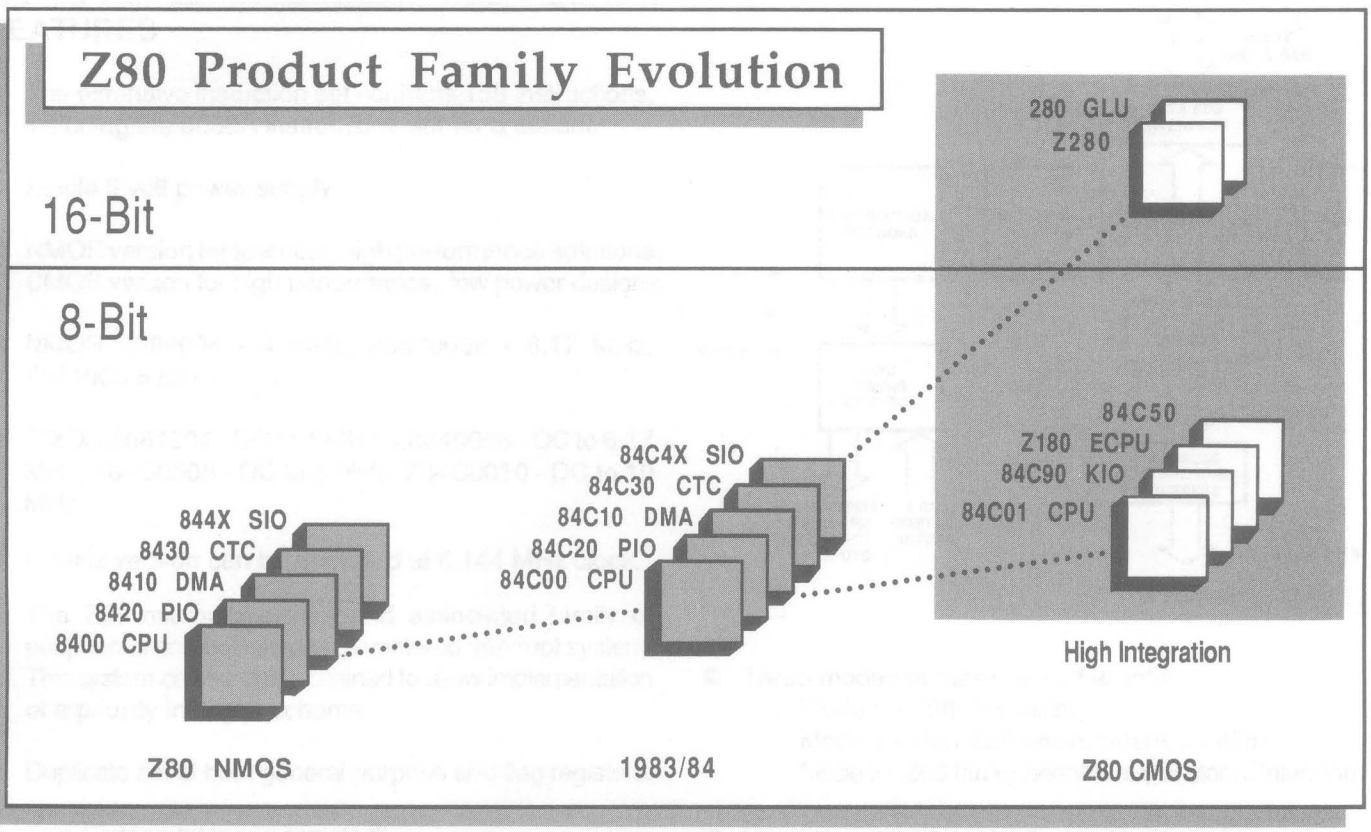
The Super8 is also available as a 48-pin and 68-pin ROMless microcomputer with four byte-wide I/O ports plus a byte-wide address/data bus. Additional address bits can be configured, up to a total of 16.

Protopack

This part functions as an emulator for the basic microcomputer. It uses the same package and pin-out as the basic microcomputer but also has a 28-pin "piggy back" socket on the top into which a ROM or EPROM can be installed. The socket is designed to accept a type 2764 EPROM.

This package permits the protopack to be used in prototype and final PC boards while still permitting user program development. When a final program is developed, it can be mask-programmed into the production microcomputer device, directly replacing the emulator. The protopack part is also useful in situations where the cost of mask-programming is prohibitive or where program flexibility is desired.

Z80 Product Family Evolution



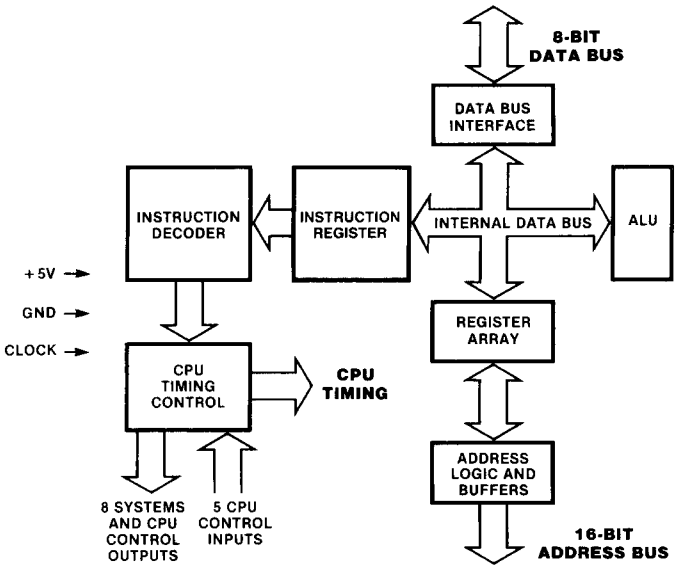
Z80 Reference Chart

Product	Pin Count	Commercial QFP	Dip	PLCC	Cerdip	Speed	Temp	Military Ceramic Dip	LCC	PGA	Speed	SMD	JAN
NMOS		-	X	X	X	4,6,8	S,M	X	X	-	2.5,4	-	X
Z8400 CPU	40,44	-	X	X	X	4	S	-	-	-	-	-	-
Z8410 DMA	40,44	-	X	X	X	4,6	S,M	X	-	-	2.5,4	X	-
Z8420 PIO	40,44	-	X	X	X	4,6	S,M	X	-	-	2.5,4	X	-
Z8430 CTC	28,44	-	X	X	X	4,6	S,M	X	-	-	2.5,4	X	-
Z8440/1/2/4 SIO	40,44	-	X	X	X	4,6	S	-	-	-	-	-	-
Z8470 DART	40,44												
CMOS													
Z84C00 CPU	40,44	X	X	X	X	4,6,8,10	E,M	X	-	-	6	-	X**
Z84C01	44	X	-	X	-	10	E	-	-	-	-	-	-
Z84C10 DMA	40,44	X	X	X	X	4,6,8	E,M**	X**	-	-	-	-	-
Z84C20 PIO	40,44	X	X	X	X	4,6,8,10	E*,M	X	-	-	6	X	-
Z84C30 CTC	28,44	X	X	X	X	4,6,8,10	E,M	X	-	-	6	X	-
Z84C40/1/2/3/4 SIO	40,44	X	X	X	X	4,6,8,10	E,M	X	-	-	6	X	-
Z84C50 RAM 80	40,44	X	X	X	-	10	E	-	-	-	-	-	-
Z80180 MPU	64,68	X	X	X	-	6,8,10	S,E,M**	-	-	X**	8	-	-
Z80280 MPU	68	-	-	X	-	10	S	-	-	-	-	-	-
Z84C90 KIO	80,84	X	-	X	-	8,10	S,E,M**	-	-	X**	8	-	-

S=0°C to +70°C
E=-40°C to +100°C
*Sampling
**Available in Q4 '89
M=(military temp.)
-55°C to +125°C
**Available in Q489

FEATURES

- The extensive instuction set contains 158 instructions, including the 8080A instructions set as a subset.
- Single 5 volt power supply.
- NMOS version for low cost, high performance solutions; CMOS version for high performance, low power designs.
- NMOS Z084004 - 4 MHz, Z0840006 - 6.17 MHz, Z084008 8 MHz.
- CMOS Z084004 - DC to 4 MHz, Z0840006 - DC to 6.17 MHz, Z84C0008 - DC to 8 MHz, Z84C0010 - DC to 10 MHz.
- 6 MHz version can be operated at 6.144 MHz clock.
- The Z80 microprocessors and associated family of peripherals can be linked by a vectored interrupt system. This system can be daisy-chained to allow implementation of a priority interrupt scheme.
- Duplicate set of both general purpose and flag registers.
- Two Sixteen bit index registers.



- Three modes of maskable interrupts:
  Mode 0 - 8080A similiar;
  Mode 1 - Non-Z80 environment, location 38H;
  Mode 2 - Z80 family peripherals, vectored interrupts.
- On-chip dynamic memory refresh counter.

GENERAL DESCRIPTION

The CPUs are fourth-generation enhanced microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable second- and third-generation microprocessors. The internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulater and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may be reserved for very fast interrupt response.

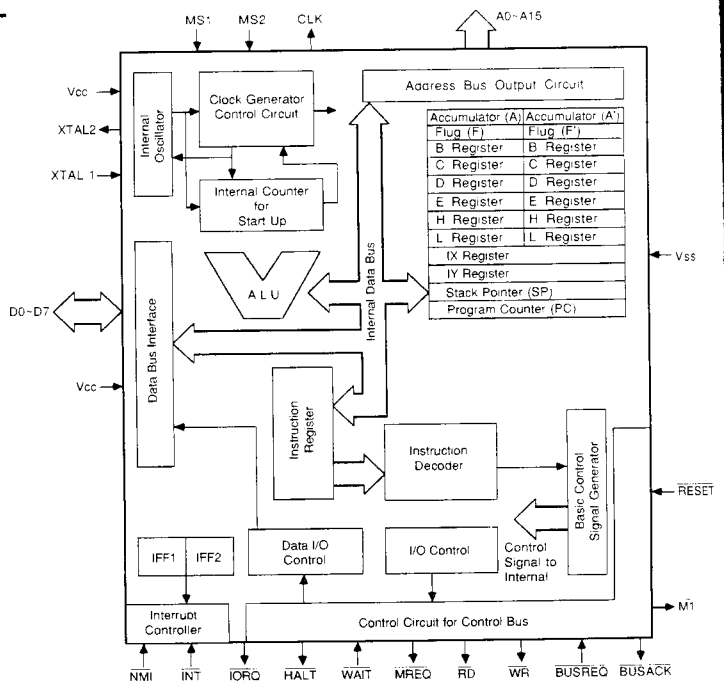
The CPU also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5V power source. All output signals are fully decoded and timed to control standard memory or peripheral circuits; the CPU is supported by an extensive family of peripheral controllers.

Z84C01 Z80®CPU with Clock Generator/Controller

FEATURES:

- Commands compatible with the Zilog Z80 MPU.
- Low power consumption:
  - 40mA Typ (5V, 10 MHz under RUN mode)
  - 2mA Typ (5V, 10 MHz under IDLE1 mode)
  - 10mA Typ (5V, 10 MHz under IDLE2 mode)
  - .5μ A Typ (5V under STOP mode)
- DC to 6, 10 MHz operation (at 5V+10%).
- Single 5V power supply (at 5V±10%).
- Operating temperature (-40°C to 100°C).
- On-chip clock generator.
- In the HALT state, the following 4 modes are selectable:
  - RUN mode
  - IDLE 1 mode
  - IDLE 2 mode
  - STOP mode
- Powerful set of 158 instructions.
- Powerful interrupt function:
  - Non-maskable interrupt terminal ($\overline{NMI}$)
  - Maskable interrrupt terminal ($\overline{INT}$)

  The following three modes are selectable:
  - 8080 compatible interrupt mode (interrupt by Non-Z80 family peripheral LSI) (Mode 0).
  - Restart interrupt (Mode 1).
  - Daisy-chain structure interrupt using Z80 family peripheral LSI (Mode 2).



- An auxiliary register provided to each of the general purpose registers.
- 2 index registers.
- 10 addressing modes.
- Built-in refresh circuit for dynamic memory.
- Molded in 44-pin PLCC package.

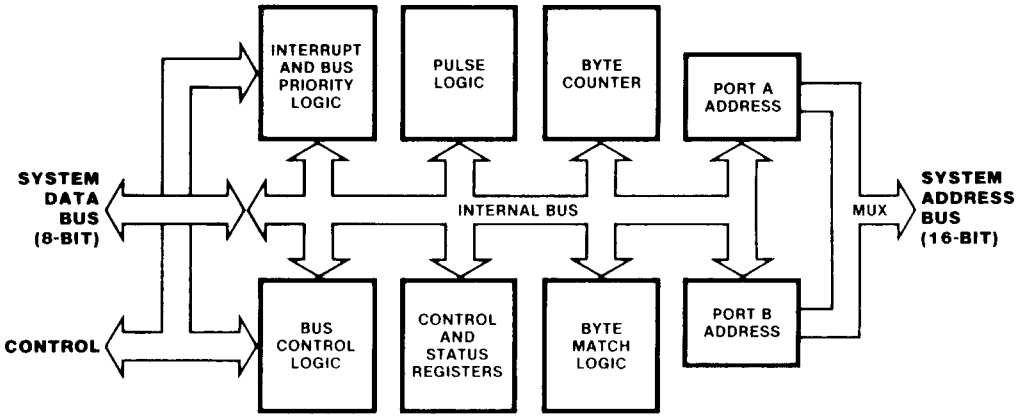
GENERAL DESCRIPTION:

The Z84C01 is an 8-bit microprocessor with a built-in clock generator/controller, which provides low power operation and high performance.

Built into the Z84C01 is a control function and clock generator for the standby function in addition to: six paired general purpose registers, accumulator, flag registers, an arithmetic-and-logic unit, bus control, memory control and timing control circuits.

The Z84C01 is fabricated with Zilog CMOS technology and molded in a 44-pin PLCC or QFP package.

NMOS/CMOS Z80 DMA Direct Memory Access Controller Z8410/Z84C10



FEATURES

- Transfers, searches, and search/transfers in Byte-at-a-Time, Burst, or Continuous modes. Cycle length and edge timing can be programmed to match the speed of any port.
- Dual-port addresses (source and destination) generated for memory-to-I/O, memory-to-memory, or I/O-to-I/O operations. Addresses may be fixed or automatically incremented/decremented.
- Next-operation loading without disturbing current operations via buffered starting-address registers. An entire previous sequence can be repeated automatically.
- Extensive programmability of functions. CPU can read complete channel status.
- NMOS version for high cost performance solutions.
- CMOS version for the designs requires low power consumption.
- NMOS Z0841004 - 4 MHz.
- CMOS Z84C1006 - DC 4 MHz to 6.17 MHz, Z84C1008 - DC to 8 MHz.
- 6 MHz version supports 6.144 MHz CPU clock operation.
- Standard Z80 Family bus-request and prioritized interrupt-request daisy-chains implemented without external logic. Sophisticated, internally modifiable interrupt vectoring.
- Direct interfacing to system buses without external logic.

GENERAL DESCRIPTION

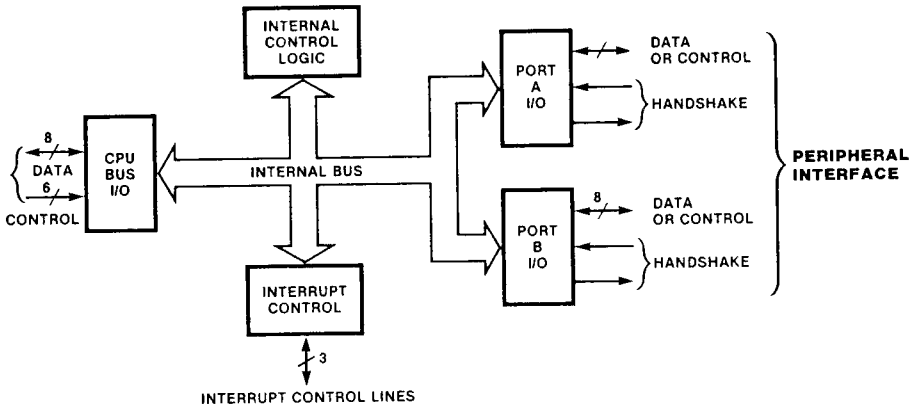
The Z80 DMA (Direct Memory Access), hereinafter referred to as Z80 DMA or DMA, is a powerful and versatile device for controlling and processing transfers of data. Its basic function of managing CPU-independent transfers between two ports is augmented by an array of features that optimize transfer speed and control with little or no external logic in systems using an 8- or 16-bit data bus and a 16-bit address bus.

Transfers can be done between any two ports (source and destination), including memory-to-I/O, memory-to-memory, and I/O-to-I/O. Dual port addresses are automatically generated for each transaction and may be either fixed or incrementing/decrementing. In addition, bit-maskable byte searches can be performed either concurrently with transfers or as an operation in itself.

The Z80 DMA contains direct interfacing to, and independent control of, system buses, as well as sophisticated bus and interrupt controls. Many programmable features, including variable cycle timing and auto-restart, minimize CPU software overhead. They are especially useful in adapting this special-purpose transfer processor to a broad variety of memory, I/O and CPU environments.

The Z80 DMA is packaged in a 40-pin plastic or Cerdip DIP, or 44-pin PLCC. It uses a single +5V power supply and the standard Z80 Family single-phase clock.

Z8420/Z84C20 NMOS/CMOS Z80®PIO Parallel Input/Output



FEATURES

- Provides a direct interface between Z80 microcomputer systems and peripheral devices.
- Two 8-bit ports with handshake, and four programmable operating modes: Output, Input, Bidirectional (Port A only), and Bit Control.
- Programmable interrupts on peripheral status conditions.
- NMOS version for high cost performance solutions.
- CMOS version for the designs requiring low power consumption.
- NMOS Z0842004 - 4 MHz, Z0842006 - 6.17 MHz.
- CMOS Z84C2004 - DC to 4 MHz, Z84C2006 - DC to 6.17 MHz, Z84C2008 - DC to 8 MHz, Z84C2010 - DC to 10 MHz.
- Standard Z80 Family bus-request and prioritized interrupt-request daisy-chains implemented without external logic.
- The eight Port B outputs can drive Darlington transistors (1.5 mA at 1.5 V).
- 6 MHz version supports 6.144 MHz CPU clock operation.

GENERAL DESCRIPTION

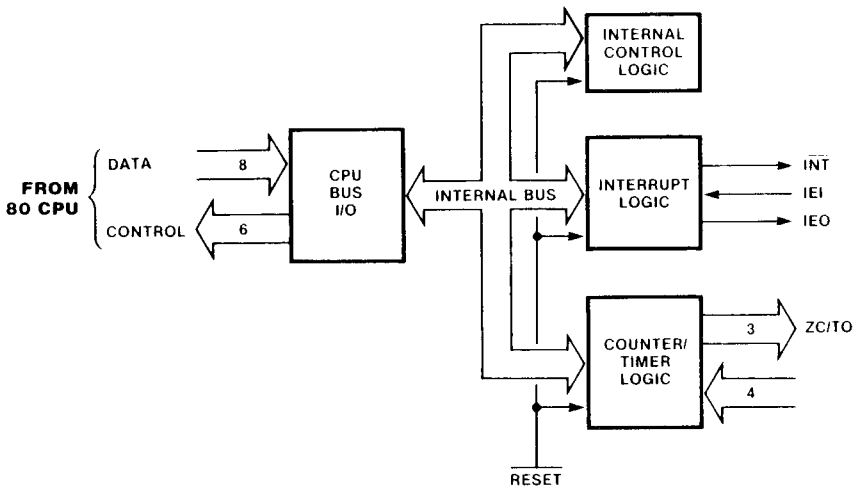
The Z80 PIO Parallel I/O Circuit (hereinafter referred to as the Z80 PIO or PIO) is programmable, dual-portdevice that provides a TTL-compatible interface between peripheral devices and the Z80 CPU. Note the QFP package is only available in CMOS version. The CPU configures the Z80 PIO to interface with a wide range of peripheral devices that are compatible with the Z80 PIO including most keyboards, paper tape reads and punches, printers, and PROM programmers.

One characteristic of the Z80 peripheral controllers that separates them from other interface controllers is that all data transfer between the peripheral device and the CPU is accomplished under interrupt control. Thus, the interrupt logic of the PIO permits full use of the efficient interrupt capabilities of the Z80 CPU during I/O transfers. All logic necessary to implement a fully nested interrupt structure is included in the PIO.

Another feature of the PIO is the ability to interrupt the CPU upon occurrence of specified status conditions in the peripheral device. For example, the PIO can be programmed to interrupt if any specified peripheral alarm conditions should occur. This interrupt capability reduces the time the processor must spend in polling peripheral status.

The Z80 PIO interfaces to peripherals via two independent general purpose I/O ports, designated Port A and Port B. Each port has eight data bits and two handshake signals, Ready and Strobe, which control data transfer. The Ready output indicates to the peripheral that the port is ready for a data transfer. Strobe is an input from the peripheral that indicates when a data transfer has occurred.

Operating Modes. The Z80 PIO ports can be programmed to operate in four modes; Output (Mode 0), Input (Mode 1), Bidirectional (Mode 2) and Bit Control (Mode 3).



FEATURES

- Four independently programmable counter/timer channels, each with a readable downcounter and a selectable 16 or 256 prescaler. Downcounters are reloaded automatically at zero count.
- Selectable positive or negative trigger initiates timer operation.
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors.
- NMOS version for high cost perfomance solutions.
- CMOS version for the designs requires low power consumption.
- NMOS Z0843004 - 4 MHz, Z0843006 - 6.17 MHz.
- CMOS Z84C3004 - DC to 4 MHz, Z84C3006 - DC to 6.17 MHz, Z84C3008 - DC to 8 MHz, Z84C3010 - DC to 10 MHz.
- Interfaces directly to the Z80 CPU, or for baud rate generation to the Z80 SIO.
- Standard Z80 Family Daisy-chain interrupt structure provides fully vectored, prioritized interrupts without external logic. The CTC may also be used as an interrupt controller.
- 6 MHz version supports 6.144 MHz CPU clock operation.

GENERAL DESCRIPTION

The Z80 CTC, hereinafter referred to as Z80 CTC or CTC, four-channel/timer can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the Z80 CTC satisfy common microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.

System design is simplified because the CTC connects directly to both the Z80 CPU and the Z80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

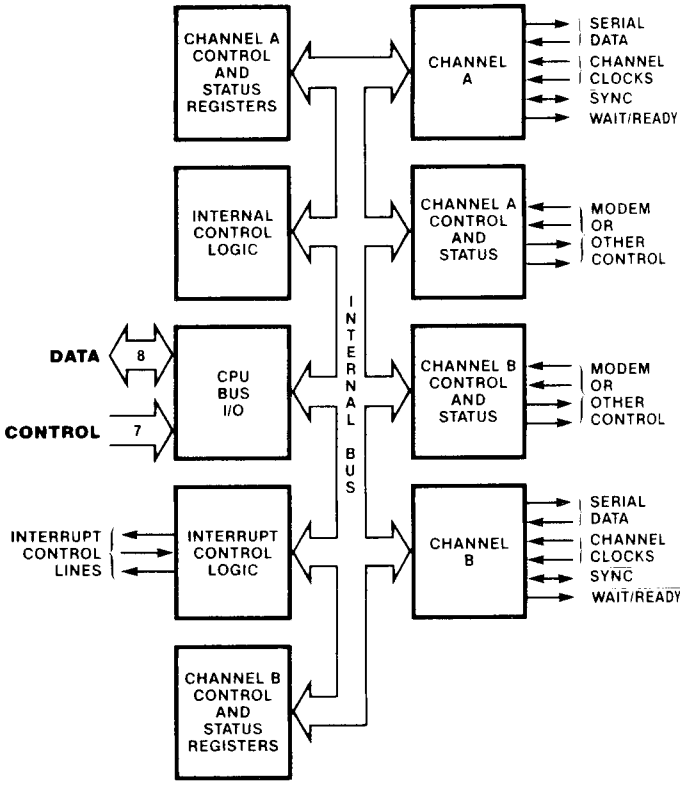
Programming the CTC is straight forward: each channel is programmed with two bytes; a third is necessary when interrupts are enabled. Once started, the CTC counts down, automatically reloads its time constant, and resumes counting. Software timing loops are completely eliminated. Interrupt processing is simplified because only one vector need be specified; the CTC internally generates a unique vector for each channel.

The Z80 CTC requires a single +5V power supply and the standard Z80 single-phase system clock. It is packaged in 28-pin DIPs, a 44-pin plastic chip carrier, and a 44-pin Quad Flat Pack. Note that the QFP package is only available for CMOS versions.

Z440/1/2/4,Z84C40/1/2/3/4 NMOS/CMOS Z80® SIO Serial Input/Output Controller

FEATURES

- Two independent full-duplex channels, with separate control and status lines for modems or other devices.
- Data rate in the x1 clock mode or 0 to 1.6M bits/second with a 8.0 MHz clock.
- NMOS version for high cost performance solutions; CMOS version for the designs requires low power consumption.
- NMOS Z0844x04 - 4 MHz Z0844x06 - 6.17 MHz (Where x is the designator for the bonding option; 0,1,2 or 4). CMOS Z84C4x04 - DC 4 MHz Z84C4x06 - DC to 6.7 MHz Z84C4x08 - DC to 8 MHz (Where x is the designator for the bonding option; 0,1,2 or 3,4).
- 6 MHz version supports 6.144 MHz CPU clock operation.
- Asynchronous protocols: everything necessary for complete messages in 5, 6, 7 or 8 bits/character. Includes variable stop bits and several clock-rate multipliers, break gereration and detection, parity, overrun and framing error detection.
- Synchronous protocols: everything necessary for complete bit- or byte-oriented messages in 5, 6, 7 or 8 bits/character, including IBM Bisync, SDLC, HDLC, CCITT-X.25 and others. Automatic CRC generation/checking, sync character and zero insertion/deletion, abort generation/detection, and flag insertion.



- Receiver data registers quadruply buffered, transmitter registers doubly buffered.
- Highly sophisticated and flexible daisy-chain interrupt vectoring for interrupts without external logic.

GENERAL DESCRIPTION

The Z80 SIO (hereinafter referred to as the Z80 SIO or SIO) Serial Input/Output Controller is a dual-channel data communication interface with extraordinary versatility and capability. Its basic functions as a serial-to-parallel, parallel-to-serial converter/controller can be programmed by a CPU for a broad range of serial communication applications.

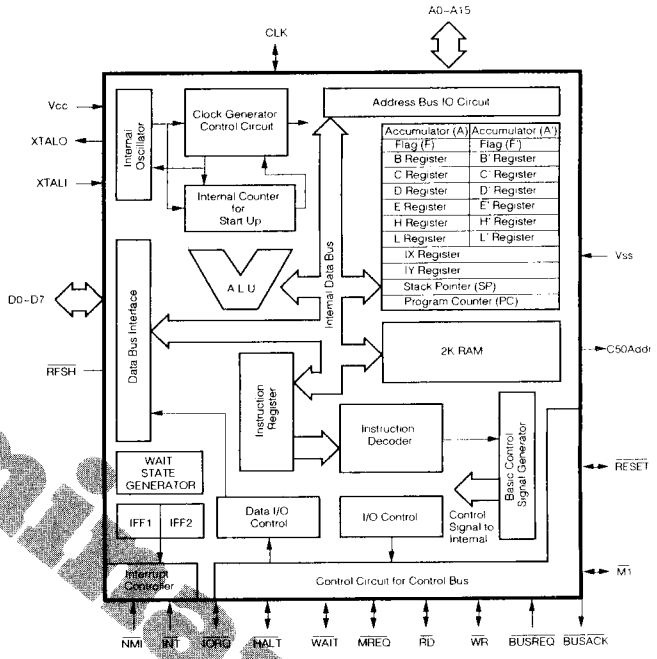
The device supports all common asynchronous and synchronous protocols, byte- or bit-orientied, and performs all of the functions traditionally done by UARTs, USARTs, and synchronous communication controllers combined. Also, additional functions traditionally performed by the CPU. Moreover, it does this on two fully-independent channels, with an exceptionally sophisticated interrupt structure that allows very fast transfers.

Full interfacing is provided for CPU or DMA control. In addition to data communication, the circuit can handle virtually all types of serial I/O with fast, or slow, peripheral devices. While designed primarily as a member of the Z80 family, its versatility makes it well suited to many other CPUs.

The Z80 SIO uses a single +5V power supply and the standard Z80 family single-phase clock. The SIO/0, SIO/1, and SIO/2 are packaged in a 40-pin PCC and the SIO/3 is packaged in a 44-pin QFP. Note that SIO/3 is only available in CMOS and in QFP package.

FEATURES

- Z80 CPU 2K Static RAM.
- Wait State Generator for external memory.
- Low power consumption
  (TBD) Typ (5V,10 MHz under RUN mode)
  (TBD) Typ (5V, 10 MHz under IDLE1 mode)
  (TBD) Typ (5V, 10 MHz under IDLE2 mode)
  (TBD) Typ (5V under STOP mode)
- DC to 10 MHz operation (at 5V ± 10%).
- Single 5V power supply (at 5V ± 10%).
- Operating Temperature (0° C to 70° C).
- On-chip clock generator.
- In the HALT state, the following 4 modes are selectable:
  RUN mode
  IDLE 1 mode
  IDLE 2 mode
  STOP mode
- Powerful set of 158 instructions.
- The following three modes are selectable:
  - 8080 compatible interrupt mode (interrupt by Non-Z80 family peripheral LSI-Mode 0).
  - Restart Interrupt (Mode 1).
  - Daisy-chain structure interrupt using Z80 family peripheral LSI (Mode 2).



- Power Interrupt function:
  Non-Maskable Interrupt terminal (NMI)
  Maskable Interrupt terminal (INT)
- Built-in refresh circuit for dynamic memory.
- Available in 40-pin DIP, 44-pin PLCC, and 44-pin QFP packages.

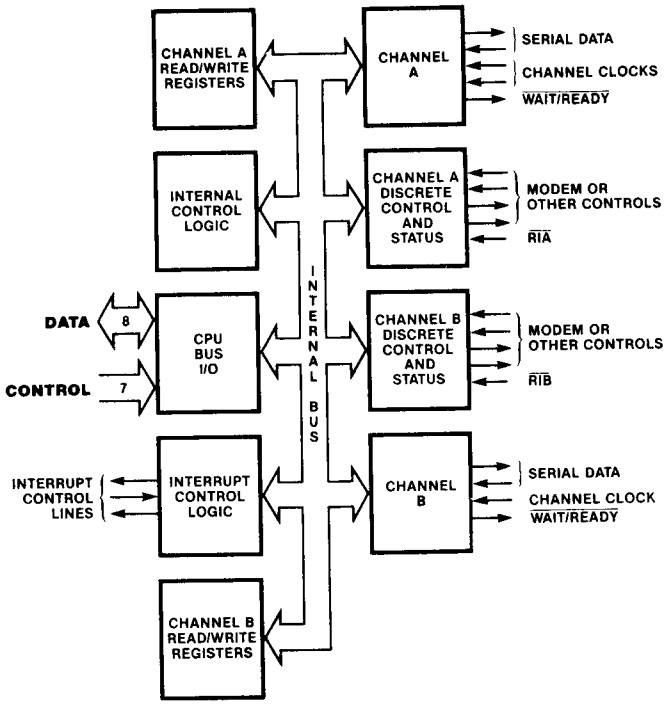
GENERAL DESCRIPTION

The Z84C50 is an 8-bit microprocessor integrated with 2K bytes of static memory and a clock generator/controller. The Z84C50 is targeted for a broad range of applications requiring a small amount of RAM. Additionally, the on-chip RAM can be accessed at a much higher rate than the external memory. This will significantly enhance performance, as the most commonly used and time critical software can be placed in on-chip memory.

Built into the Z84C50 is a control function and clock generator for the standby function in addition to: six paired general purpose registers, accumulator, flag registers, an arithmetic-and-logic unit, bus control, memory control and timing control circuits. Also, an on-chip wait state generator can be used for automatically inserting wait states for external memory accesses.

The Z84C50 is fabricated with Zilog CMOS technology and molded in 40-pin DIP, 44-pin PLCC, and 44-pin QFP packages.

Z8470 Z80® DART Dual Asynchronous Receiver/Transmitter



FEATURES

- Two independent full-duplex channels with separate modem controls. Modem status can be monitored.
- In x1 clock mode; data rates are 0 to 800K bits/second with a 4.0 MHz clock or 0 to 1.2 M bits/second with a 6.0 MHz clock.
- Receiver data registers are quadruply buffered; the transmitter is doubly buffered.
- Programmable options include 1, 1 1/2, or 2 stop bits; even, odd, or no parity; and x1, x16, x32, and x64 clock modes.
- Break generation and detection as well as parity-, overrun-, and framing-error detection are available.
- Interrupt features include a programmable interrupt vector, a "status affects vector" mode for fast interrupt processing, and the standard Z80 peripheral daisy-chain interrupt structure that provides automatic interrupt vectoring with no external logic.
- On-chip logic for ring indication and carrier-detect status.

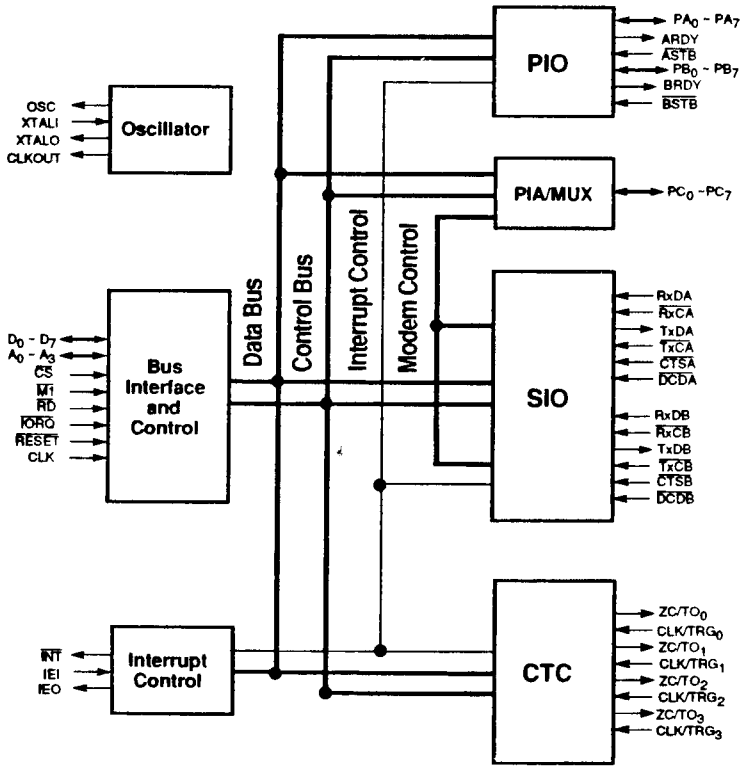
GENERAL DESCRIPTION

The Z80 DART (Dual-Channel Asynchronous Receiver/Transmitter) is a dual-channel multifunction peripheral component that satisfies a wide variety of asynchronous serial data communications requirements in microcomputer systems. The Z80 DART is used as a serial-to-parallel, parallel-to-serial converter/controller with asynchronous applications. In addition, the device also provides modem controls for both channels. In applications where modem controls are not needed, these lines can be used for general purpose I/O.

Zilog also offers the Z80 SIO, a more versatile device that provides synchronous (Bisync, HDLC, and SDLC) as well as asynchronous operation.

The Z80 DART is fabricated with n-channel silicon-gate depletion-load technology, and is packaged in a 40-pin plastic or ceramic DIP.

CMOS Z80®KIO Serial/Parallel/Counter/Timer Z84C90



FEATURES:

- Two independent synchronous/asynchronous serial channels.
- Three 8-bit parallel ports.
- Four independent counter/timer channels.
- On-chip clock oscillator/driver.
- Software/Hardware Resets.
- Designed in CMOS for low power operations.
- Supports Z80 Family interrupt daisy-chain.
- Programmable interrupt priorities.
- 8 and 10 MHz bus clock frequency.
- Single +5 Volt Power Supply.

GENERAL DESCRIPTION:

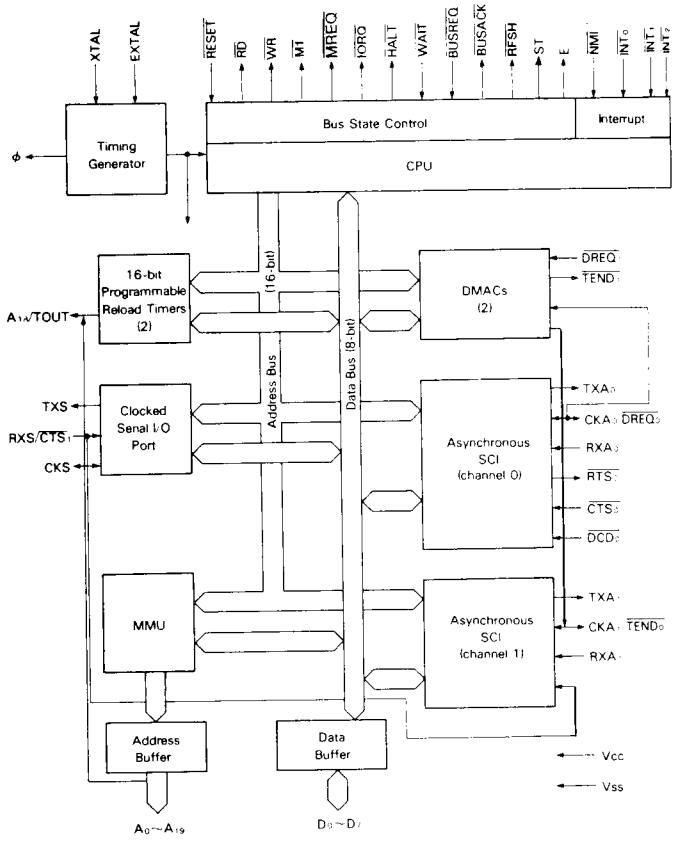
Zilog's new Z84C90 Serial/Parallel/Counter/Timer (KIO) is a multi-channel, multi-purpose I/O device designed to provide the end-user with a cost effective and powerful solution to meet his peripheral needs. The Z84C90 combines the features of one Z84C30 CTC, one Z84C4xSIO, one Z84C20 PIO, a byte-wide bit-programmable I/O port, and a crystal oscillator into a single 84-pin PLCC package.

Utilizing fifteen internal registers for data and programming information, the KIO can easily be configured to any given system environment. Although the optimum performance is obtained with a Z84C00 CPU, the KIO can just as easily be used with any other CPU.

Z80180 Z180 MPU

FEATURES

- Operating Frequency to 10 MHz.
- On-Chip MMU supports extended address space.
- Two DMA channels.
- On-Chip wait state generators.
- Two UART channels.
- Two 16-bit timer channels.
- On-Chip interrupt controller.
- On-Chip clock oscillator/generator.
- Clocked serial I/O port.
- Code compatible with Zilog Z80 CPU.
- Extended instructions.
- 6 MHz version supports 6.144 MHz CPU clock.



GENERAL DESCRIPTION:

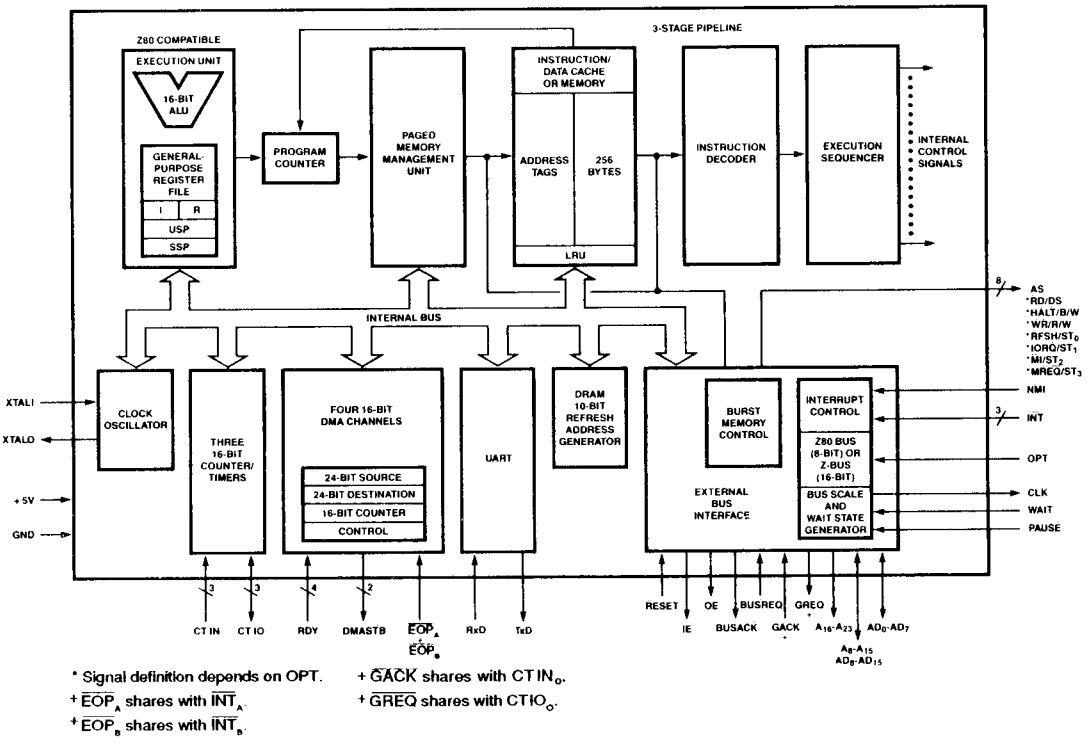
Based on a microcoded execution unit and an advanced CMOS manufacturing technology, the Z80180 is an 8-bit MPU which provides the benefits of reduced system costs and low power operation while offering higher performance and maintaining compatibility with a large base of industry standard software written around the Zilog Z80 CPU.

Higher performance is obtained by virtue of higher operating frequencies, reduced instruction execution times, an enhanced instruction set, and an on-chip memory management unit (MMU) with the capability of addressing up to 1 Mbyte of memory.

Reduced system costs are obtained by incorporating several key system functions on-chip with the CPU. These key functions include I/O devices such as DMA, UART, and timer channels. Also included on-chip are several "glue" functions such as dynamic RAM refresh control, wait state generators, clock oscillator, and interrupt controller.

Not only does the Z80180 consume a low amount of power during normal operation, but it also provides two operating modes that are designed to drastically reduce the power consumption even further. The SLEEP mode reduces power by placing the CPU into a "stopped" state, thereby consuming less current, while the on-chip I/O device is still operating. The SYSTEM STOP mode places both the CPU and the on-chip peripherals into a "stopped" mode, thereby reducing power consumption even further.

When combined with other CMOS VLSI devices and memories, the Z80180 provides an excellent solution to system applications requiring high performance and low power operation. Available in 64-pin DIP, 68-pin PLCC and 80-pin QFP.



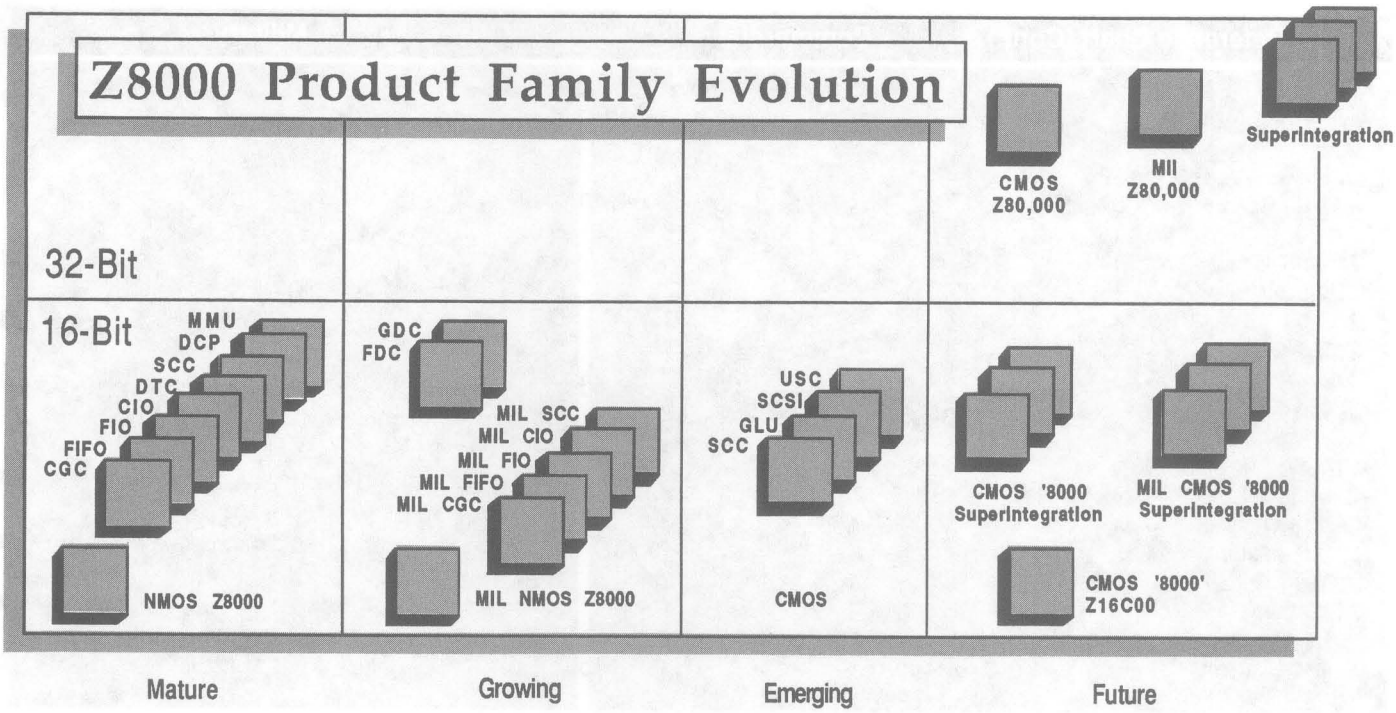
* Signal definition depends on OPT.
+ $\overline{EOP}_A$ shares with $\overline{INT}_A$.
+ $\overline{EOP}_B$ shares with $\overline{INT}_B$.
+ $\overline{GACK}$ shares with $CTIN_0$.
+ $\overline{GREQ}$ shares with $CTIO_0$.

FEATURES

- Designed in CMOS for low power operations.
- Enhanced Z80 CPU instruction set that maintains object-code compatibility with Z80 microprocessor.
- Three-stage pipelined, 16-bit CPU architecture with user and system modes.
- Direct coprocessor and multiprocessor interface support.
- On-chip Memory Management Unit (MMU) addresses up to 16 Mbytes.
- On-chip 256-byte instruction and data associative cache memory with burst load.
- High performance 16-bit Z-BUS interface or 8-bit Z80 CPU compatible bus interface.
- Three on-chip 16-bit counter/timers.
- Four on-chip DMA channels.
- On-chip full duplex UART.
- Refresh controller for dynamic RAMs.
- On-chip oscillator or direct input clock options.
- 20 MHz oscillator clock frequency.

GENERAL DESCRIPTION

The Z80280 brings 16-bit CPU and sophisticated features required by complex, high performance applications to the Z80 architecture. Z280 maintains complete object code compatibility with the Z80. One of the unique features of the Z280 is its bus size. By strapping a single pin on the chip, the designer can select 8 or 16-bit bus widths. Thus to use existing designs, an 8-bit Z80 compatible bus can be used. Higher performance systems can be designed using the Z280's 16 bit mode, in which all memory references use true 16 bit accesses. A single processor can be used in both medium and high performance products, without changing the software. The Z280 includes a Memory Management Unit (MMU), which gives the processor access to 16 MB of memory. Other features of the Z280 include on-chip instruction and cache memory, 3-stage pipeline, dual operating modes, four channel DMA Controller, three 16 bit counter/timers, programmable refresh and wait state generation, and a serial port with on-chip baud rate generation.



Z8000 Reference Chart

Commercial

Product	Pin Count	QFP	Dip	PCC	Cerdip	Speed
NMOS						
Z8001 CPU	48	-	X	-	CERAM	6,10
Z8002 CPU	40,44	-	X	X	X	6,10
Z8160 CPU	44	-	-	X	-	6,10
Z-BUS Peripherals						
Z8016 Z-DTC	48,68	-	X	X	CERAM	6
Z8030 Z-SCC	40,44	X	X	X	X	6,8
Z8036 Z-CIO	40,44	-	X	X	X	6
Z8038 Z-FIO	40,44	-	X	X	X	6
Z8060 FIFO	28	-	X	-	CERAM	1MB/S
Z8068 DCP	40	-	X	-	-	4
Z8581 CGC	18	-	X	-	CERAM	10

Cont. on next page

S=0°C to +70°C E=-40°C to +100°C

Military

Ceramic Temp	Dip	LCC	Speed	SMD	JAN
S,E,M	X	X	4,6,10	X	-
S,E,M	X	X	4,6,10	X	X
S	-	-	-	-	-
S	-	-	-	-	-
S,E,M	X	X	4,6	X	-
S,E,M	X	X	4,6	X	-
S,E,M	X	X	6	-	-
S	-	-	-	-	-
S	-	-	-	-	-
S,E,M	X	X	6,10	X	-

M=(military temp.)
-55°C to =125°C

® Z8000 Product Family

Z8000 Reference Chart (Cont.)

Product	Pin Count	QFP	Dip	PCC	Cerdip	Speed	Ceramic Temp	Dip	LCC	Speed	SMD	JAN
Universal Peripherals												
Z8516 DTC	48,68	-	X	X	CERAM	6	S	-	-	-	-	-
Z8530 SCC	40,44	X	X	X	X	6,8	S,M	X	X	4,6	X	-
Z8536 CIO	40,44	-	X	X	X	6	S,E,M	X	X	4,6	X	-
Z8538 FIO	40	-	X	-	-	6	S,M	X	X	6	-	-
Z8560 FIFO	40,44	-	X	-	-	1MB/S	S	-	-	-	-	-
Z8581 CGC	18	-	X	-	CERAM	10	S,E,M	X	X	6,10	X	-
Z7220A GDC	40,44	-	X	X	CERAM	6,8	S	-	-	-	-	-
Z765A FDC	40,44	-	X	X	CERAM	6,8	S	-	-	-	-	-
CMOS												
Z80C30 Z-SCC	40,44	X	X	X	-	8,10	S,E,M	X	X*	6,8	-	-
Z85C30 SCC	40,44	X	X	X	-	8,10	S,E,M	X	X*	6,8	X	X*
Z16C20 Z-GLU	84	-	-	X	-	10,16	S	-	-	-	-	-
Z085380 SCSI	40,44	-	X	X	-	20	S,E	-	-	-	-	-
Z16C30	68	-	-	X	-	10	S	-	-	-	-	-

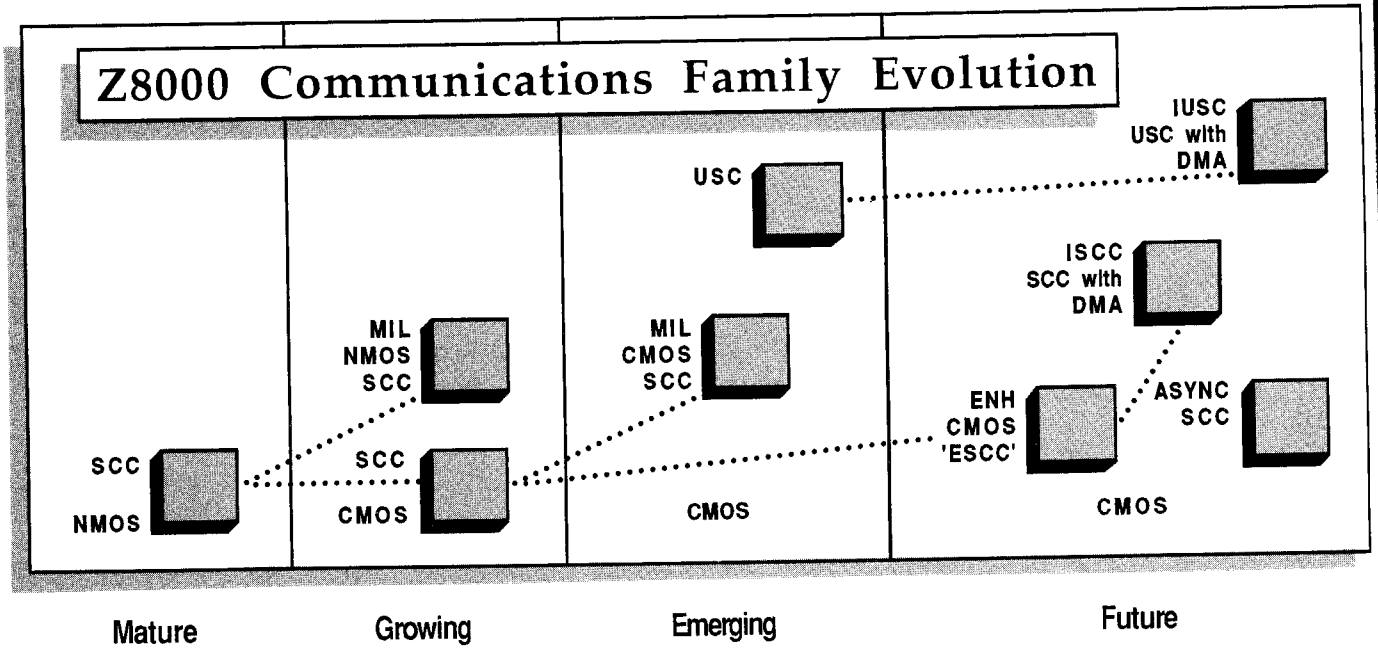
Commercial

Military

S=0°C to +70°C E=-40°C to +100°C

M=(military temp.) -55°C to =125°C

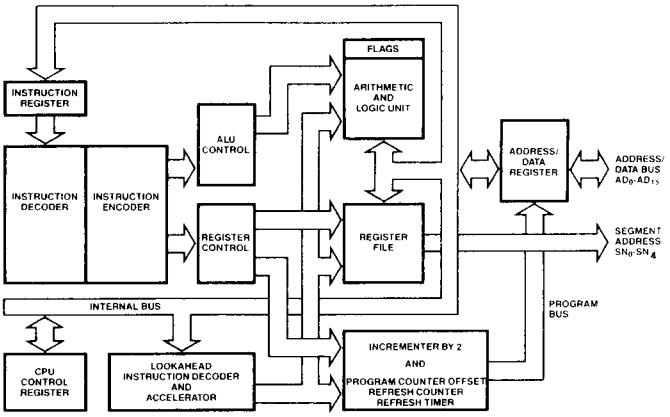
*Available Q489


Z8000 Communications Family Evolution
SCC
NMOS
SCC
CMOS
MIL
NMOS
SCC
MIL
CMOS
SCC
CMOS
USC
ENH
CMOS
'ESCC'
ISCC
SCC with
DMA
IUSC
USC with
DMA
ASYNC
SCC
CMOS
Mature
Growing
Emerging
Future

CPU Central Processing Unit Z160™

FEATURES

- Fully software compatible member of the Z8000® architecture.
- Instruction set more powerful than many minicomputers.
- Directly addresses 2 Mbytes in 32 segments.
- Eight user-selectable addressing modes.
- Seven data types that range from bits to 32-bit long words and byte and word strings.
- System and Normal operating modes.
- Separate code, data, and stack spaces.
- Sophisticated interrupt structure.
- Resource-shaping capabilities for multiprocessing systems.
- Multi-programming support.



- Compiler support.
- 32-bit operations, including signed multiply and divide.
- Z-BUS compatible.
- 6 and 10 MHz clock rate.
- Small, low-cost 44-pin PLCC package for surface mount applications.

GENERAL DESCRIPTION

The Z8000 is an advanced high-end 16-bit microprocessor that spans a wide variety of applications ranging from simple stand-alone computers to complex parallel-processing systems. Essentially a monolithic minicomputer central processing unit, the Z8000 CPU is characterized by an instruction set more powerful than many minicomputers; abundant resources in registers, data types, addressing modes and addressing range, and a regular architecture that enhances throughput by avoiding critical bottlenecks such as implied or dedicated registers.

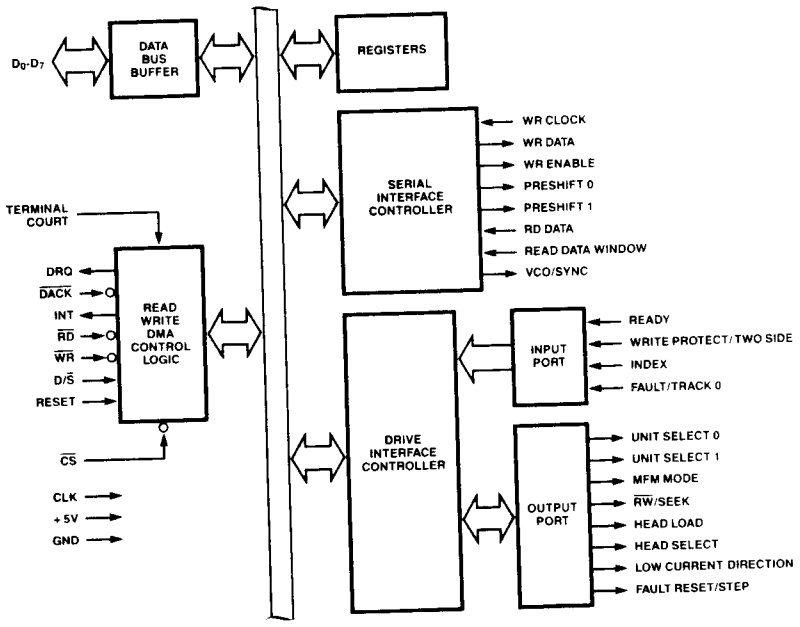
CPU resources include sixteen 16-bit general purpose registers, seven data types that range from bits to 32-bit long words and byte and word strings, and eight user-selectable addressing modes. The 110 distinct instruction types can be combined with the various data types and addressing modes to form a powerful set of 414 instructions. Moreover, the instruction set is regular; most instructions can use any of the five main addressing modes and can operate on byte, word, and long-word data types.

The CPU can operate in either the system or normal mode. The distinction between these two modes permits privileged operations, thereby improving operating system organization and implementation. Multi-programming is supported by the "atomic" Test and Set instuction; multiprocessing by a combination of instruction and hardware features; and compliers by multiple stacks, special instructions, and addressing modes.

The Z160 is a segmented CPU. It can directly address 2 megabytes of memory. The two operating modes - system and normal - and the distinction between code, data, and stack spaces within each mode allows memory extension up to 12 megabytes.

The Z160 is fabricated with high-density, high-performance scaled n-channel silicon-gate depletion-load technology, and is housed in leadless chip carriers(LCC).

Z765A FDC Floppy Disk Controller



FEATURES

Address Mark detection circuitry internal to the FDC simplifies the phase-locked loop and read electronics. The track stepping rate, head load time, and head unloaded time are user-programmable.

Z765A-features are:

- IBM-compatible format, Single and Double Density.
- Multisector and multitrack transfer capability.
- Data scan capability, scans a single sector or an entire cylinder comparing byte-for-byte host memory and disk data.
- Drives up to 4 floppy-disk drives (FDD).
- Data transfers in DMA or non-DMA mode.
- Parallel seek operations on up to four drives.
- Compatible with most general purpose microprocessors.
- Single phase 8 MHz clock.
- +5V Only.
- 40-Pin Dual-In-Line (DIP) package, 44-pin plastic chip carrier (PLCC) package.

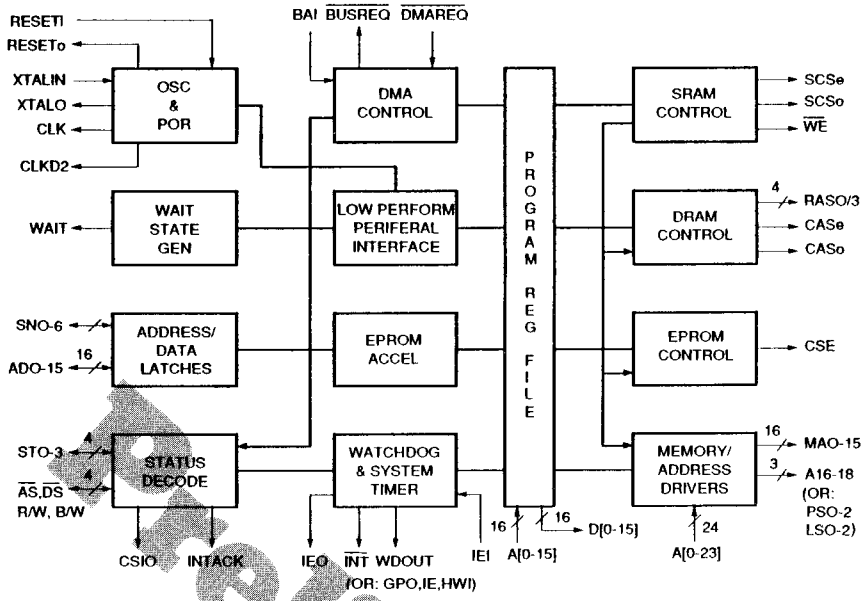
GENERAL DESCRIPTION

The Z765A is an LSI Floppy Disk Controller (FDC) chip which contains the circuitry and control fuctions for interfacing a processor to four floppy disk drives. It supports IBM System 3740 Single Density format (FM) and IBM System 34 Double Density format (MFM) including double-sided recording. The Z765A provides control signals which simlpify the design of an external phase locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy disk interface

Handshaking signals make DMA operation easily incorporated with the aid of an external DMA Controller chip, such as the Z80 DMA. The FDC operates in either the DMA o non-DMA mode. In the non-DMA mode the FDC generate interrupts to the processor every time a data byte is to b transferred. In the DMA mode, the processor need only loa the command into the FDC and all data transfers occu under control to the FDC and DMA controllers.

The Z765A executes 15 commands; each command re quires multiple 8-bit bytes to fully specify the operatio which the processor wishes the FDC to perform.

CMOS Z-BUS® GLU General Logic Unit Z16C20



FEATURES:

- Directly Interfaces Z8000 CPU's To Their Peripherals.
- 8M Byte Address Range.
- Eprom Interface.
- Static RAM Interface.
- Dynamic RAM Interface / Timing.
- Eprom Address Accelerator.
- DMA Controller.
- Clock Generator.
- Reset Circuitry.
- Programmable Wait State Generators.
- Input/Output Latch Controls.
- General Purpose Timers.
- Watchdog Timer.
- Prioritized Interrupts.
- Fully Programmable.
- 10 MHz and 16 MHz Versions.

GENERAL DESCRIPTION:

The Z16C20 CMOS GLU integrates into a single device the SSI and MSI logic typically required to interface a 16-bit Z8000 or Z16C00 CPU in a system environment.. It provides the user with an optimum system design solution in the following areas;cost, parts count, board area, reliability, and performance. This is achieved while simplifying hardware design and shortening design cycles.

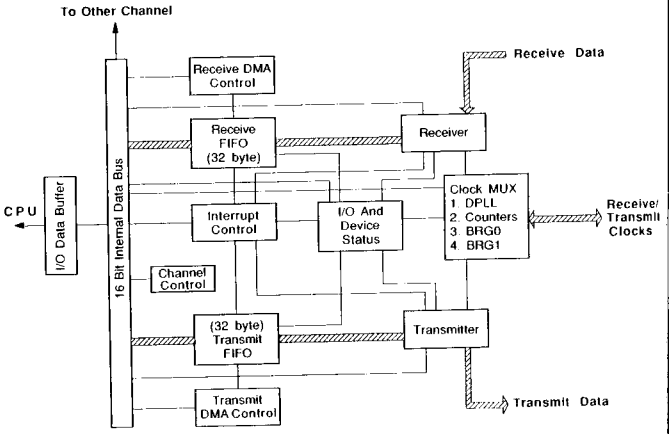
The Z16C20GLU supports up to 8M bytes of address space. It interfaces directly and simultaneously to EPROMs, SRAMs, and DRAMs. By programming in their individual address space boundaries, the Z16C20 recognizes the type of memory being accessed and generates the appropriate controls and handshake signals required.

By anticipating code fetches, EPROM addresses are generated by the GLU ahead of time. This allows the use of slower and less expensive EPROMs while maintaining high performance within the system. A DMA channel is provided for easy bootstrapping on power-up as well as for other DMA applications. In addition, the GLU has elaborate timing circuitry: on-chip clock generator with system clock and 1/2 system clock outputs (for slow peripherals) and two general purpose, fully programmable 16-bit timers (timer B can be used as a watchdog timer). It is also capable of automatically inserting wait-states when needed, prioritizing the interrupts and issuing synchronized resets.

Z16C30 CMOS USC Universal Serial Controller

FEATURES

- Two independent, 0 to 10 Mbit/sec, full duplex channels,each with two baud rate generators and digital phase-locked loop for clock recovery.
- Multi-protocol operation under program control with independent mode selection for receiver and transmitter.
- Async mode with one to eight bits/character, 1/16 to 2 stop bits/character in 1/16 bit increments; programmable clock factor; break detect and generation; odd, even, mark, space or no parity and framing error detection. Supports an Address/Data bit and MIL STD 1553B.
- Byte oriented synchronous mode with one to eight bits/character; programmable idle line condition; optional receive sync stripping; optional preamble transmission; 16 or 32 bit CRC and transmit-to-receive slaving (for X.21).
- External character sync mode for receive.
- HDLC/SDLC mode with eight bit address compare; extended address field option; 16 or 32 bit CRC; programmable idle line condtion; optional; preamble transmission and loop mode.
- DMA interface with separate request and acknowledge for each receiver and transmitter.



- Channel load command for DMA controlled initialization.
- Flexible bus interface for direct connection to most microprocessors; use programmable for 8- or 16-bits wide.
- 12.5 MByte/sec (16 bit) data bus bandwidth.
- 32 byte data FIFO's for each receiver and transmitter.
- Low power CMOS.
- 68 pin PLCC package.

GENERAL DESCRIPTION

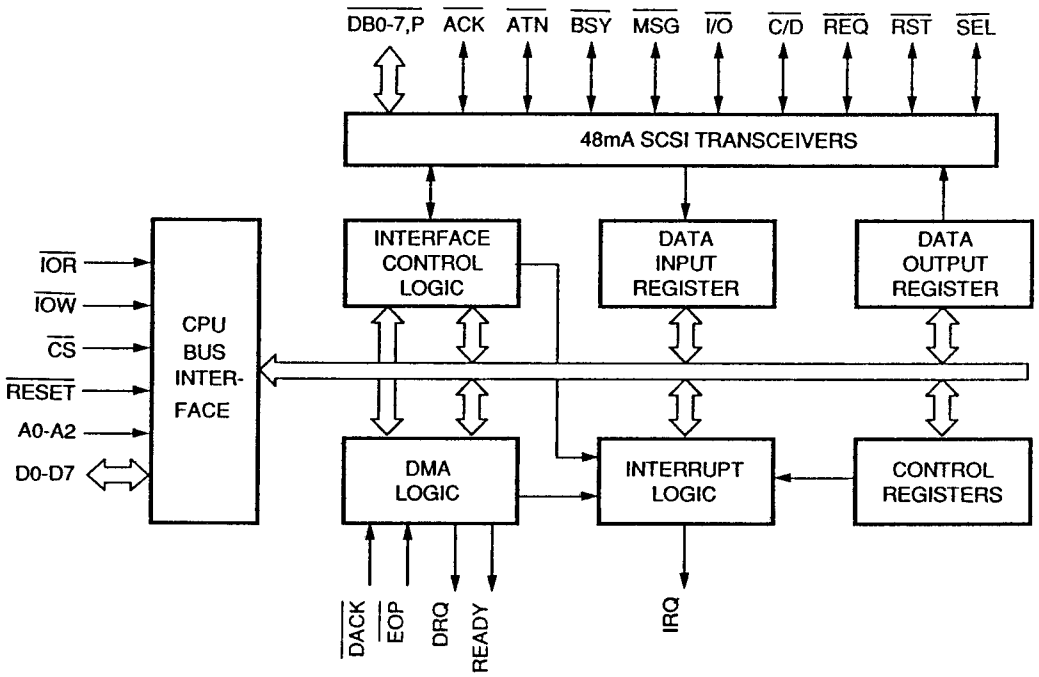
The USC Universal Serial Controller is a dual-channel multi-protocol data communications peripheral designed for use with any conventional multiplexed or non-multiplexed bus. The device contains a variety of new, sophisticated internal functions including character counters for both receive and transmit in each channel and 32 byte data FIFO's for each receiver and transmitter.

The USC handles asynchronous formats, synchronous byte-oriented formats such as BISYNC and synchronous bit-oriented formats such as HDLC. This device supports virtually any serial data transfer application.

The device can generate and check CRC in any synchronous mode and can be programmed to check data integrity in various modes. The USC also has facilites for modem controls in both channels.

Interrupts are supported with a daisy-chain hierarchy, with the two channels having completely separate interrupt structures.

High-speed data transfers via DMA are supported by a Request/Acknowledge signal pair for each receiver and transmitter. The device supports automatic status transfer via DMA and allows device initialization under DMA control also.



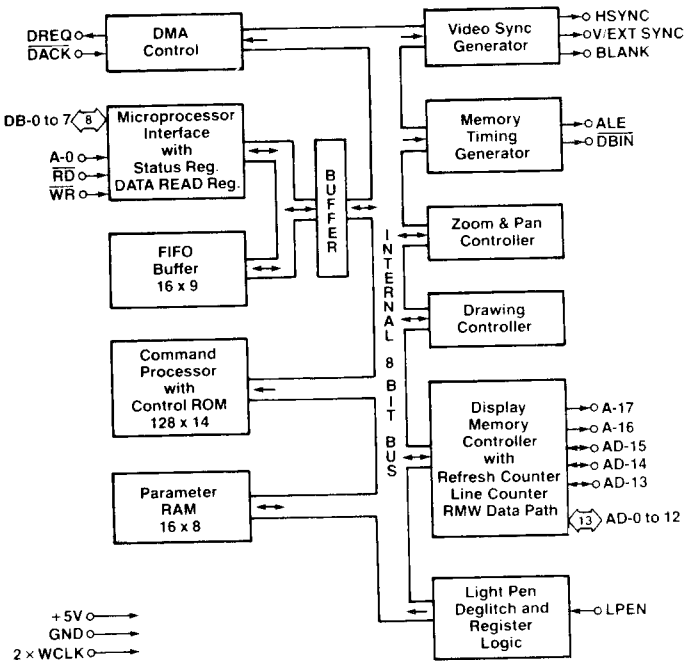
FEATURES:

- Compatible 5380 Pinout
- CMOS - Typical Icc 2.5 mA
- Asynchronous Interface, Supports 1.5 MB/s
- Direct SCSI Bus Interface with On-Board 48 mA Drivers
- Supports Target and Initiator Roles
- Arbitration Support
- DMA or Programmed I/O Data Transfers
- Supports Normal or Block Mode DMA
- Memory or I/O Mapped CPU Interface

GENERAL DESCRIPTION:

Zilog's Z5380 SCSI (Small Computer System Interface) controller, is a 40 pin DIP or 44 pin PLCC CMOS device. It was designed to implement the SCSI protocol as defined by the ANSI X3T9.2 Committee, and is a plug-in replacement of the industry standard, the NMOS 5380. The Z5380 is capable of operating both as a Target and an Initiator. This enables the Z5380 to find its use in Bus Host Adaptors, Formatters, and Host Port designs. Special high-current open-drain outputs enable it to directly interface to, and drive, the SCSI bus. These drivers are capable of sinking 48 mA at 0.5V. The Z5380 has the necessary interface hook-ups so the system CPU can communicate with it, like with any other peripheral device. The CPU can read from, or write to the SCSI registers which may be addressed as standard or memory-mapped I/O's. The Z5380 increases the system performance by minimizing the CPU intervention in DMA operations which the Z5380 controls. The CPU will be interrupted by the Z5380 when it detects a bus condition that requires that attention. It also supports arbitration and reselection. The Z5380 has the proper handshake signals to support normal and block mode DMA operations with most of the popular DMA controllers available.

Z7220A High-Performance Graphics Display Controller



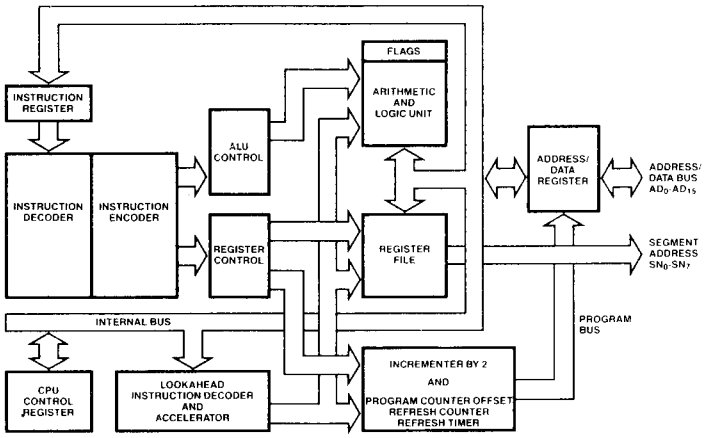
FEATURES

- Microprocessor Interface, DMA transfers, FIFO Command Buffering.
- Display Memory Interface, Up to 256K words of 16 bits, Read-Modify-Write (RMW) Display Memory cycles as fast as 500ns, Dynamic RAM refresh cycles for nonaccessed memory.
- Light Pen Input.
- Drawing Hold Input.
- External video synchronization mode.
- Graphics Mode, Four megabit, bit-mapped display memory.
- Character Mode, 8K character code and attributes display memory.
- Mixed Graphics and character Mode, 64K if all characters, 1 megapixel if all graphics.
- Graphics capabilities, Figure drawing of lines, arc/ circles, rectangles, and graphics characters om 500ns per pixel, Display 1024-by-1024 pixels with 4 planes of color or gray-scale,Two independently scrollable areas.
- Character capabilities, Auto cursor advance, Four independently scrollable areas, Programmable cursor height, Characters per row: up to 256, Characters per row: up to 100.
- Video Display Format, Zoom Magnification factors of to 16, Panning, Command-settable video raster parameters.
- Technology; Single +5V, NMOS, 40-pin DIP.
- DMA Capability, Byte or word transfers, 4 clock periods per byte transferred.
- On-chip pull-up resistor for VSYNC/EXT, HSYNC and $\overline{DACK}$, and a pull-down resistor for LPEN/DH.

GENERAL DESCRIPTION

The Z7220A High-performance Graphics Display Controller (HGDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance rasterscan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the HGDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the HGDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the HGDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the HGDC is ideal for advanced computer graphics applications.

CPU Central Processing Unit Z8001®/Z8002®/Z8000®



FEATURES

- Regular, easy-to-use architecture.
- Instruction set more powerful than many minicomputers.
- Directly addresses 8 Mbytes.
- Eight user-selectable addressing modes.
- Seven data types that range from bits to 32-bit long words and byte and word strings.
- System and Normal operating modes.
- Separate code, data, and stack spaces.
- Sophisticated interrupt structure.
- Resource-shaping capabilties for multiprocessing systems.
- Multi-programming support.
- Compiler support.
- Memory management and protection provided by Z8010 Memory Management Unit.
- 32-bit operations, including signed multiply and divide.
- Z-BUS compatible.
- 6 and 10 MHz clock rate.

GENERAL DESCRIPTION

The Z8000 is an advanced high-end 16-bit microprocessor that spans a wide variety of applications ranging from simple stand-alone computers to complex parallel-processing systems. Essentially a monolithic minicomputer central processing unit, the Z8000 CPU is characterized by an instruction set more powerful than many minicomputers; abundant resources on register, data types, addressing modes and addressing range, and a regular architecture that enhances throughtput by avoiding critical bottlenecks such as implied or dedicated registers.

The Z8000 CPU is offered in three versions: The Z8001/Z160 segmented CPUs and the Z8002 nonsegmented CPU. The main difference is in addressing range. The Z8001 can directly address 8 megabytes of memory; the Z160 directly addresses 2 megabytes; the Z8002 directly addresses 64 kilobytes. The two operation modes - system and normal - and the distinction between code, data, and stack spaces within each mode allows memory extension up to 48 megabytes for the Z8001, 12 megabytes for the Z160 and 384 kilobytes for the Z8002.

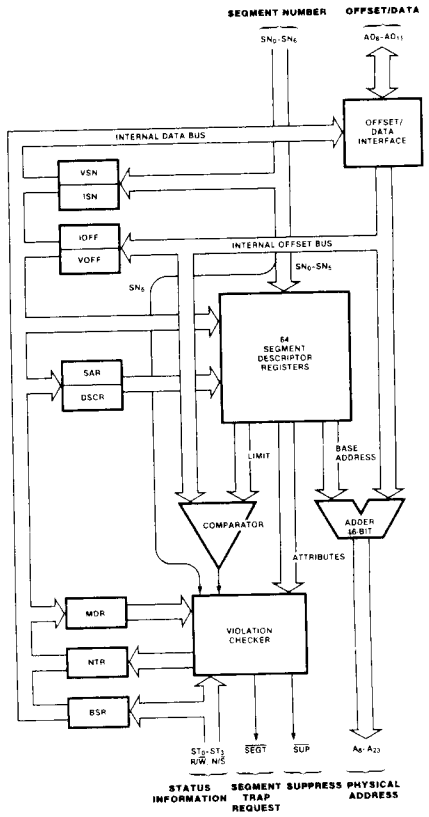
To meet the requirements of complex, memory-intensive applications, a companion memory management device is offered for the Z8001. The Z8010 Memory Management Unit manages the large address space by providing features such as a segment relocation and memory protection. The Z8001 can be used with or without the Z8010. If used by itself, the Z8001 still provides an 8 megabyte direct addressing range, extendable to 48 megabytes.

The Z8001, Z8002 and Z8010 are fabricated with high-density, high-performance scaled n-channel silicon-gate depletion-load technology, and are housed in Dual-In-Line packages (DIPs) and Leadless Chip Carriers (LCC).

Z8010 Z8000® MMU Memory Management Unit

Features

- Dynamic segment relocation makes software addresses independent of physical memory addresses.
- Sophisticated memory-management features include access validation that protects memory areas from unauthorized or unintentional access, and a write-warning indicator that predicts stack overflow.
- For use with both Z8001 and Z8003 CPU.
- 64 variable-sized segments from 256 to 65,536 bytes can be mapped into a total physical address space of 16M bytes; all 64 segments are randomly accessible.
- Multiple MMUs can support several translation tables for each Z8001 address space.
- MMU architecture supports multi-programming systems and virtual memory implementations.



General Description

The Z8010 Memory Management Unit (MMU) manages the large 8M byte addressing spaces of the Z8001 CPU. The MMU provides dynamic segment relocation as well as numerous memory protection features.

Dynamic segment relocation makes user software addresses independent of the physical memory addresses, thereby freeing the user from specifying where information is actually located in the physical memory. It also provides a flexible, efficient method for supporting multi-programming systems. The MMU uses a translation table to transform the 23-bit logical address output from the Z8001 CPU into a 24-bit address for the physical memory. (Only logical memory addresses go to an MMU for translation; I/O addresses and data, in general, must by pass this component.)

Memory segments are variable in size from 256 bytes to 64K bytes, in increments of 256 bytes. Pairs of MMUs support the 128 segment numbers available for the various Z8001 CPU address spaces. Within an address space, any number of MMUs can be used to accommodate multiple translation tables for System and Normal operating modes, or to support more sophisticated memory-management systems.

MMU memory protection features safeguard memory areas from unauthorized or unintended access by associating special access restrictions with each segment. A segment is assigned a number of attributes when its descriptor is entered into the MMU. When a memory reference is made, these attributes are checked against the status information supplied by the Z8001 CPU. If a mismatch occurs, a trap is generated and the CPU is interrupted. The CPU can then check the status registers of the MMU to determine the cause.

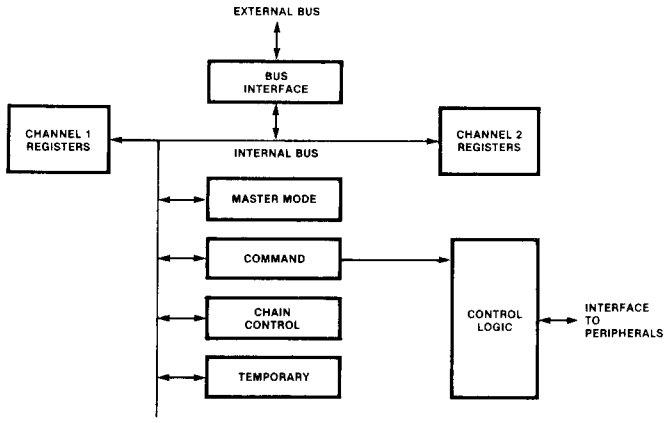
Segments are protected by modes of permitted use, such as read only, system only, execute only and CPU access only. Other segment management features include a write-warning zone useful for stack operations and status flags that record read or write accesses to each segment.

The MMU is controlled via 22 Special I/O instructions from the Z8000 CPU in System mode. With these instructions, system software can assign program segments to arbitrary memory locations, restrict the use of segments and monitor whether segments have been read or written.

Direct Memory Access Transfer Controller Z8016 Z8000® Z-DTC

FEATURES

- Memory-to-peripheral transfers up to 2.66M bytes per second at 4 MHz.
- Memory-to-memory transfers up to 1.33M bytes per second at 4 MHz.
- Two fully independent, multi-function channels.
- Masked data pattern matching for Search and Transfer-and-Search operations.
- Funneling option that permits mixing of byte and word data during transfer operations.
- Can operate in logical address space with Zilog Memory Management Units, providing an 8M byte logical addressing range and 16M byte physical addressing range.
- Programmable chaining operation provides automatic loading of control parameters from memory into each channel.
- Software- or hardware-controlled Wait state insertion.
- Z-BUS daisy-chain interrupt hierarchy and bus-request structure.



GENERAL DESCRIPTION

The Z8016 DMA Transfer Controller (DTC) is a high performance data transfer device designed to match the power and addressing capability of the Z8000 CPUs. In addition to providing block data transfer capability between memory and peripherals, each of the two DTC channels can perform peripheral-to-peripheral and memory-to-memory transfers. A special Search mode of operation compares data read from memory or peripherals with the contents of a pattern register. A search can be performed concurrently with transfers or as an operation in itself.

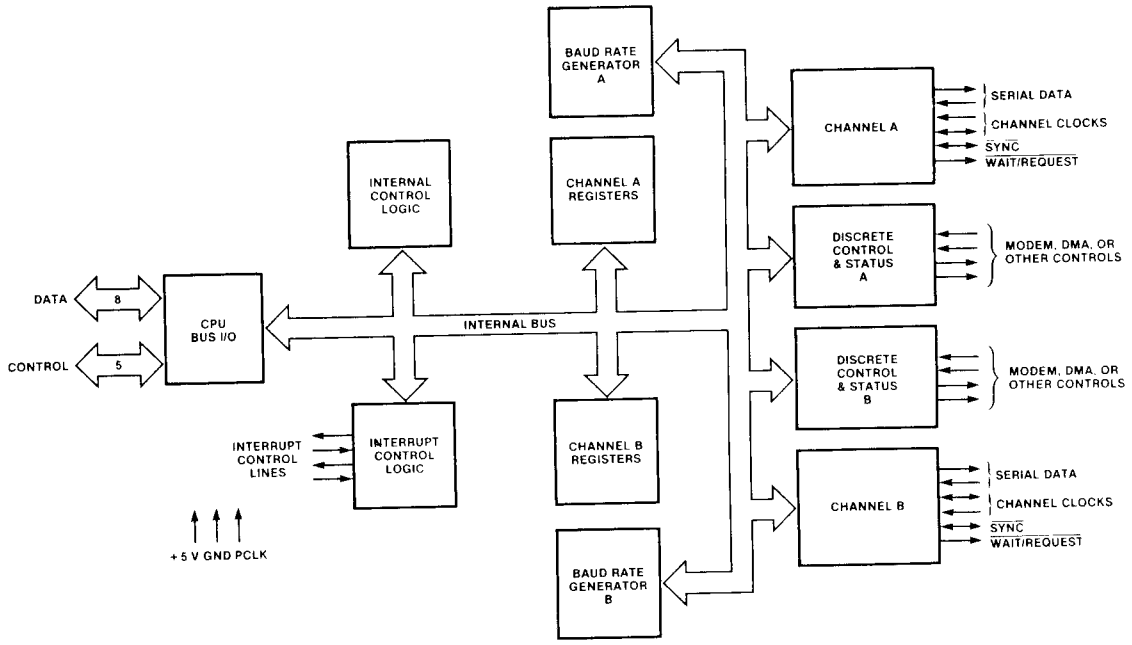
In all operations (Search, Transfer, and Transfer-and-Search), the DTC can operate in either Flow-through or Flyby transfer mode. In the Flow-through mode, data is stored temporarily within the DTC on its way from source to destination. In this mode, transfers can be made between a word-oriented memory and a byte-oriented peripheral through the bidirectional byte/word funneling option. In Flyby mode, data is transferred in a single step (from source to destination), thus providing twice the throughput.

In addition to providing a hardware $\overline{\text{WAIT}}$ input to accommodate different memory or peripheral speeds, the Z8016 DTC allows the user to program the automatic insertion of either zero, one, two, or four Wait states for either source or destination addresses. Alternatively, the $\overline{\text{WAIT}}$ input pin function can be disabled and these software-programmed Wait states used exclusively.

The Z8016 DTC minimizes CPU involvement by allowing each channel to load its control registers from memory automatically when a DMA operation is complete. By loading the address of the next block of control parameters as part of this operation, command chaining is accomplished. The only action required of the CPU is to load the address of the control parameter table into the channel's Chain Address register and then issue a Start Chain command.

The Z8016 DTC is directly Z-BUS compatible, and operates within the Z8000 daisy-chain vectored-priority interrupt scheme. The Demand Interleave operation allows the DTC to surrender the bus to the external system, or to alternate between internal channels. This capability allows for parallel operations between dual channels or between a DTC channel and the CPU.

Z8030/Z8530 Z-BUS SCC/SCC Serial Communications Controller



FEATURES

- 128-byte FIFO buffer provides asynchronous bidirectional CPU/CPU or CPU/peripheral interface, expandable to any width in byte increments by use of multiple FIOs.
- Interlocked 2-Wire or 3-Wire Handshake logic port mode; Z-BUS® or non-Z-BUS interface.
- Pattern recognition logic stops DMA transfers and/or interrupts CPU; present byte count can initiate variable-length DMA transfers.
- Seven sources of vectored/non-vectored interrupt which include pattern-match, byte count, empty or full buffer status; a dedicated "mailbox" register with interrupt capability provides CPU/CPU communication.
- REQUEST/WAIT lines control high-speed data transfers.
- All functions are software controlled via directly addressable read/write registers.

GENERAL DESCRIPTION

The Z8038/Z8538 FIO provides an asynchronous 128-byte FIFO buffer between two CPUs or between a CPU and a peripheral device. This buffer interface expands to a 16-bit or wider data path and expands in depth to add as many Z8060 FIFOs (and an additional FIO) as are needed.

The FIO manages data transfers by assuming Z-BUS, non-Z-BUS microprocessor (a generalized microprocessor interface), Interlocked 2-Wire Handshake, and 3-Wire Handshake operating modes. These modes interface dissimilar CPUs, or CPUs and peripherals running under differing speeds or protocols, allowing asynchronous data transactions and improving I/O overhead by as much as two orders of magnitude.

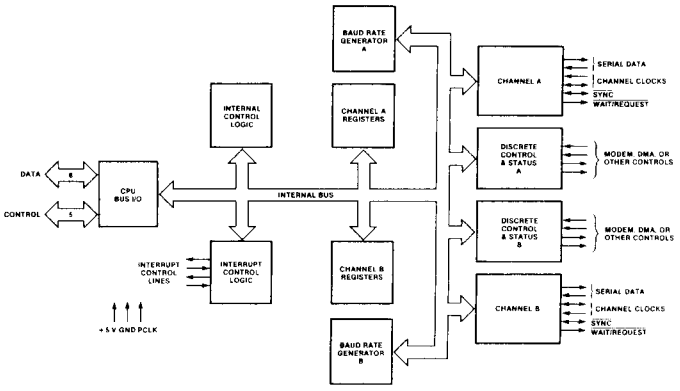
The FIO supports the Z-BUS interrupt protocols, generating seven sources of interrupts upon any of the following events: a write to a message register, change in data direction, pattern match, status match, over/underflow error, buffer full and buffer empty status. Each interrupt source can be enabled or disabled, and can also place an interrupt vector on the port address/data lines.

The data transfer logic of the FIO has been specially designed to work with DMA (Direct Memory Access) devices for high-speed transfers. It provides for data transfers to or from memory each machine cycle, while the DMA device generates memory address and control signals. The FIO also supports the variably sized block length, improving system throughput when multiple variable length messages are transferred amongst several sources.

Z-BUS SCC/SCC Serial Communications Controller Z80C30/Z85C30

FEATURES

- Low power CMOS.
- Pin compatible to NMOS version.
- Two independent, 0 to 2.5M bit/second, full-duplex channels, each with a separate crystal oscillator, baud rate generator, and Digital Phase-Locked Loop for clock recovery.
- Multi-protocol operation under program control; programmable for NRZ, NRZI, or FM data encoding.
- Asynchronous mode with five to eight bits and one, one and one-half, or two stop bits per character; programmable clock factor; break detection and generation; parity, overrun, and framing error detection.
- Synchronous mode with internal or external character synchronization on one or two synchronous characters and CRC generation and checking with CRC-16 or CRC-CCITT preset to either 1s or 0s.
- SDLC/HDLC mode with comprehensive frame-level control, automatic zero insertion and deletion, I-field residue handling, abort generation and detection, CRC generation and checking, SDLC Loop mode operation.



- Local Loopback and Auto Echo modes.
- Supports T1 digital trunk.
- Enhanced DMA support:
  - -10 x 19-bit status FIFO
  - -14-bit byte counter

GENERAL DESCRIPTION

The Z80C30/Z85C30 CMOS SCC Serial Communications Controller is a CMOS version of the industry standard NMOS SCC. It is a dual channel, multi-protocol data communications peripheral that easily interfaces to CPU's with either multiplexed or non-multiplexed address/data buses. The advance CMOS process offers lower power consumption, higher performance, and superior noise immunity. The programming flexibililty of the internal registers allows the SCC to be configured to satisfy a wide variety of serial communications applications. The many on-chip features such as baud rate generators, digital phase locked loops, and crystal oscillators dramatically reduce the need for external logic. Additional features including a 10 x 19-bit status FIFO and 14-bit byte counter were added to support high speed SDLC transfers using DMA controllers.

The SCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.).

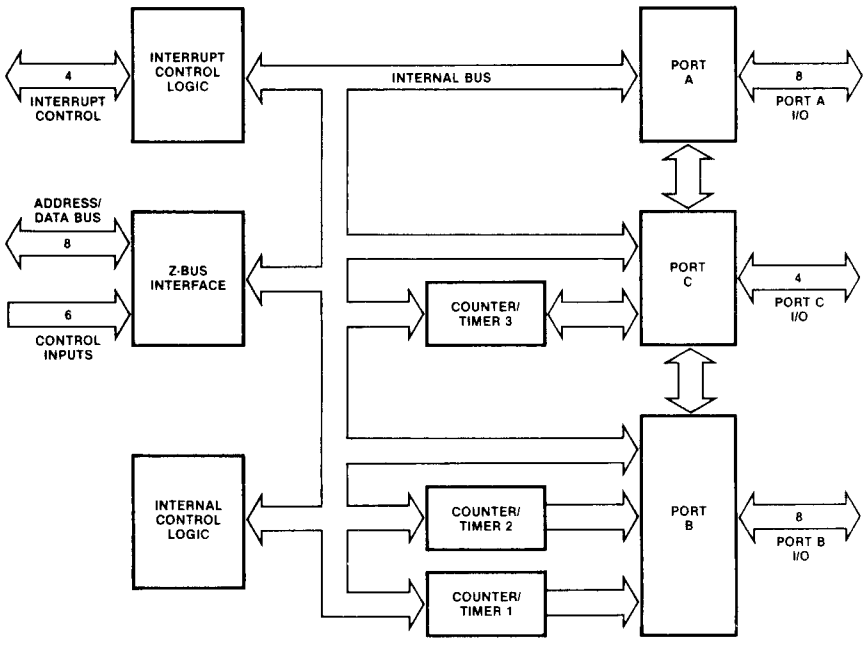
The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general purpose I/O.

The daisy-chain interrupt hierarchy is also supported-- and is standard for Zilog peripheral components.

The interrupt caused by the Abort or EOP has a special feature allowing the SCC to interrupt when the Abort or EOP sequence is detected or terminated. This feature facilitates the proper termination or the current message, correct initialization of the next message, and the accurate timing of the Abort condition in external logic in SDLC mode. In SDLC Loop mode, this feature allows secondary stations to recognize the wishes of the primary station to regain control of the loop during a poll sequence.

CPU/DMA Block Transfer.
The SCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers.

Z8036 Z8000® Z-CIO Counter/Timer and Parallel I/O Unit



Features

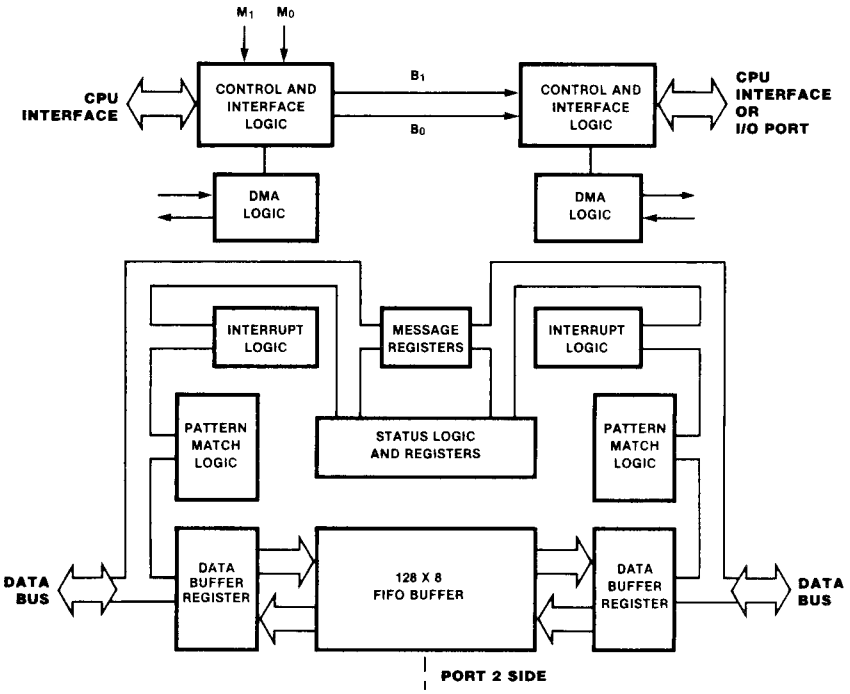
- Two independent 8-bit, double-buffered, bidirectional I/O ports plus a 4-bit special purpose I/O port. I/O ports feature programmable polarity, programmable direction (Bit mode), "pulse catchers," and programmable open-drain outputs.
- Four handshake modes, including 3-Wire (like the IEEE-488).
- REQUEST/$\overline{\text{WAIT}}$ signal for high-speed data transfer.
- Flexible pattern-recognition logic, programmable as a 16-vector interrupt controller.
- Three independent 16-bit counter/timers with up to four external access lines per counter/timer (count input, output, gate, and trigger), and three output duty cycles (pulsed, one-shot, and square-wave), programmable as retriggerable or non-retriggerable.
- Easy to use since all registers are read/write and directly addressable.

General Description

The Z8036 Z-CIO Counter/Timer and Parallel I/O element is a general purpose peripheral circuit, satisfying most counter/timer and parallel I/O needs encountered in system designs. This versatile device contains three I/O ports and three counter/timers. Many programmable options tailor its configuration to specific applications.

The use of the device is simplified by making all internal registers (command, status, and data) readable and (except for status bits) writable. In addition, each register is given its own unique address so that it can be accessed directly—no special sequential operations are required. The Z-CIO is directly Z-Bus compatible.

FIO FIFO Input/ Output Interface Unit Z8038/Z8538



Features

- 128-byte FIFO buffer provides asynchronous bidirectional CPU/CPU or CPU/peripheral interface, expandable to any width in byte increments by use of multiple FIOs.
- Interlocked 2-Wire or 3-Wire Handshake logic port mode; Z-BUS or non-Z-BUS interface.
- Pattern recognition logic stops DMA transfers and/or interrupts CPU; preset byte count can initiate variable-length DMA transfers.
- Seven sources of vectored/nonvectored interrupt which include pattern-match, byte count, empty or full buffer status; a dedicated "mailbox" register with interrupt capability provides CPU/CPU communication.
- $\overline{\text{REQUEST}}/\overline{\text{WAIT}}$ lines control high-speed data transfers.
- All functions are software controlled via directly addressable read/write registers.

General Description

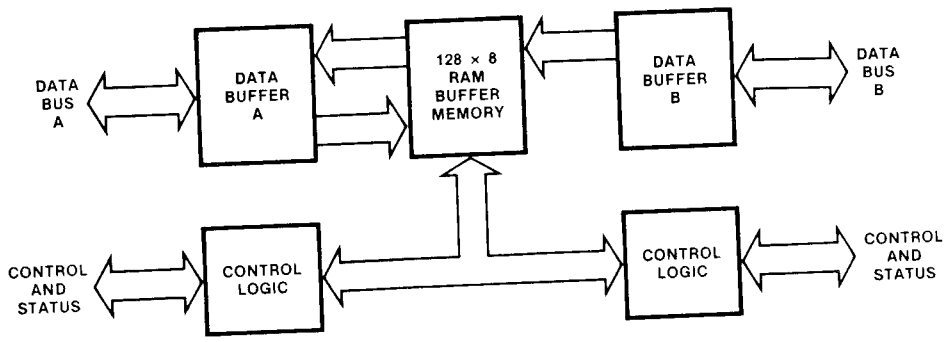
The Z8038/Z8538 FIO provides an asynchronous 128-byte FIFO buffer between two CPUs or between a CPU and a peripheral device. This buffer interface expands to a 16-bit or wider data path and expands in depth to add as many Z8060 FIFOs (and an additional FIO) as are needed.

The FIO manages data transfers by assuming Z-BUS, non-Z-BUS microprocessor (a generalized microprocessor interface), Interlocked 2-Wire Handshake, and 3-Wire Handshake operating modes. These modes interface dissimilar CPUs or CPUs and peripherals running under differing speeds or protocols, allowing asynchronous data transactions and improving I/O overhead by as much as two orders of magnitude.

The FIO supports the Z-BUS interrupt protocols, generating seven sources of interrupts upon any of the following events: a write to a message register, change in data direction, pattern match, status match, over/underflow error, buffer full and buffer empty status. Each interrupt source can be enabled or disabled, and can also place an interrupt vector on the port address/data lines.

The data transfer logic of the FIO has been specially designed to work with DMA (Direct Memory Access) devices for high-speed transfers. It provides for data transfers to or from memory each machine cycle, while the DMA device generates memory address and control signals. The FIO also supports the variably sized block length, improving system throughput when multiple variable length messages are transferred amongst several sources.

Z8060/Z8560 FIFO Buffer Unit



FEATURES

- Bidirectional, asynchronous data transfer capability.
- Large 128-bit-by-8-bit buffer memory.
- Two-wire, interlocked handshake protocol.
- Wire-ORing of empty and full outputs for sensing of multiple-unit buffers.
- 3-state data outputs.
- Connects any number of FIFOs in series to form buffer of any desired length.
- Connects any number of FIFOs in parallel to form buffer on any desired width.

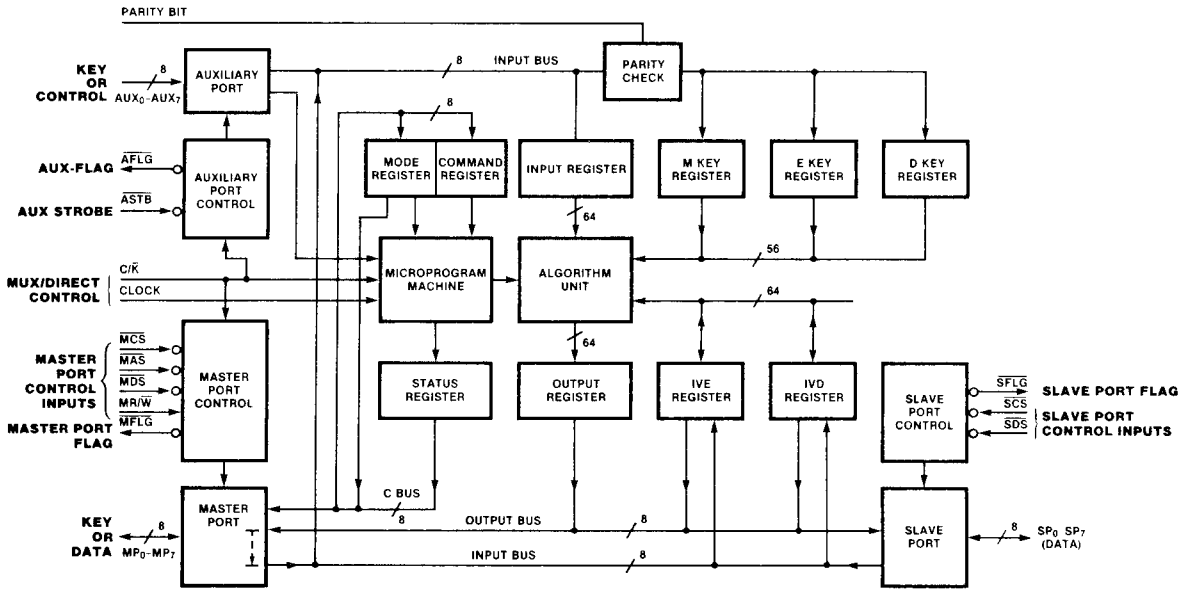
GENERAL DESCRIPTION

The Z8060/Z8560 First-In First-Out (FIFO) Buffer Units consist of a 128 by 8-bit memory, bidirectional data transfer and handshake logic. The structure of the FIFO unit is similar to that of other available buffer units. FIFO is a general purpose unit; its handshake logic is compatible with that of other members of Zilog's Z8® and Z8000® Families.

FIFOs can be cascaded end-to-end without limit to form a parallel 8-bit buffer of any desired length (in 128-byte increments). Any number of single or multiple unit FIFO serial buffers can be connected in parallel to form buffers of any desired width (in 8-bit increments).

The FIFO buffer units are available as 28-pin packages.

Data Ciphering Processor Z8068/Z9518 Z-DCP



FEATURES

- Encrypts and decrypts data using the National Bureau of Standards encryption algorithm.
- Supports three standard ciphering modes: Electronic Code Book, Chain Block and Cipher Feedback.
- Three separate registers for encryption, decryption, and master keys improve system security and throughput by eliminating frequent reloading of keys.
- Three separate programmable ports (master, slave, and key data) provide hardware separation of encrypted data, clear data, and keys.
- Data rates greater than 1M bytes per second can be handled.
- Key parity check.

GENERAL DESCRIPTION

The Z8068 Data Ciphering Processors (DCP) are n-channel, silcon-gate LSI devices, which contains the circuitry to encrypt and decrypt data using National Bureau of Standards encryption algorithms. It is designed to be used in a variety of environments, including dedicated controllers, communication concentrators, terminals, and peripheral task processors in general processor systems.

The DCP provides a high throuput rate using Cipher Feedback, Electronic code book, or Cipher Block Chain operation modes. The provisions of separate ports for key input, clear data, and enciphered data enhances security.

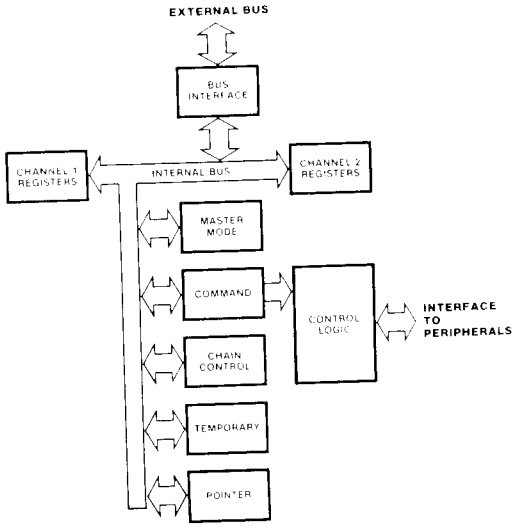
The host system communicates with the DCP using commands entered in the master port or through auxiliary control lines. Once set up, data can flow through the DCP at high speeds because input, output and ciphering activities can be performed concurrently. External DMA control can easily be used to enhance throughput in some system configurations.

The Z8068 DCP is designed to interface directly to Zilog's Z-BUS .

Z8516/Z9516 DMA Transfer Controller

FEATURES

- Two independent multi-function channels.
- Transfer Modes: single, demand dedicated with bus hold, demand dedicated with bus release, demand interleave.
- Memory/peripheral transfers up to 2.66 Megabyte/second at 4 MHz and 4 Megabyte/second at 6 MHz.
- Memory/memory flow-through transfer up to 1.33 Megabytes/second 4 MHz and 2 Megabyte/second at 6 MHz.
- 16 Megabyte physical addressing range in each address space.
- Data types: byte-to-byte, word-to-word, byte/word funneling.
- Automatic loading/reloading of control parameters by each channel.
- Optional automatic chaining of operations.
- Masked data pattern matching for search operations.
- Vectored interrupts on selected transfer conditions.
- Software or hardware wait state insertion.



- Address increment, decrement, or hold.
- Channel interleave operations.
- Interleave operations with system bus.
- Base registers for efficient repetitive operations.
- Reload word table for efficient channel initialization.
- Software DMA request.

GENERAL DESCRIPTION

The Z8516 Universal DMA Transfer Controller (DTC) is a high performance peripheral interface circuit for non-Z-BUS CPUs. In addition to providing data block transfer capability between memory and peripherals, each of the DTC's two channels can perform peripheral-to-peripheral and memory-to-memory transfers. A special Search Mode of operation compares data read from a memory or peripheral source with the contents of a pattern register.

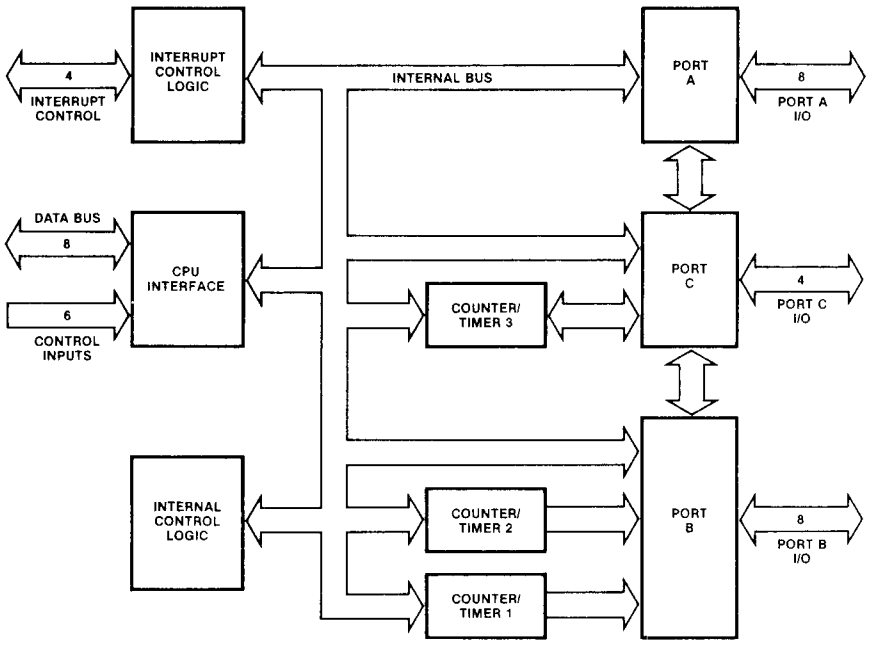
For all DMA operations (search, transfer, and transfer-and-search), the DTC can operate with either byte or word data sizes. In some system configurations it may be necessary to transfer between word-organized memory and a byte-oriented peripheral. The DTC provides a byte packing/unpacking capability through its byte-word funneling transfer or transfer-and-search option. Some DMA applications may continuously transfer data between the same two memory areas; these applications may not require the flexibility inherent in reloading registers from memory tables. To service these repetitive DMA operations, base registers, which reinitialize the current source and destination address and Operation Count registers, are provided on each channel. To change the data transfer direction under CPU control, provision is made for reassigning the source address as a destination and the destination as a source, eliminating the need for actual reloading of these address registers.

DMA devices frequently must interface to slow peripherals or slow memory. In addition to providing a hardware WAIT input, the Z8516 DTC allows the user to program the automatic insertion of either 0,1,2, or 4 wait states for either source or destination addresses. The user may even disable the wait pin function and exclusively use these software programmed wait states.

High throughput and powerful transfer options are less useful if a DMA requires frequent reloading by the host CPU. The Z8516 minimizes CPU interactions by allowing each channel to load its control registers. The only CPU action required is to load the control parameter table's address into the channel's Chain Address register and then issue a Start Chain command to start the register loading operation. This reloading operation is called command chaining and the table is called the Chain Control Table.

The Z8516 DTC is packaged in a 48-pin DIP and uses a single +5V power supply.

Counter/Timer and Parallel I/O Unit Z8536 CIO



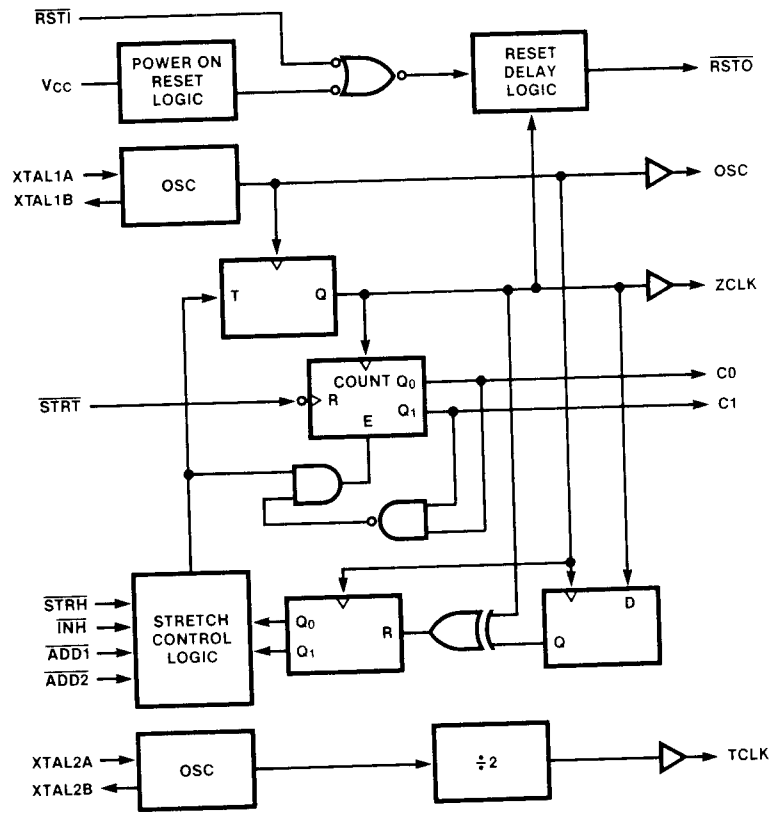
Features

- Two independent 8-bit, double-buffered, bidirectional I/O ports plus a 4-bit special-purpose I/O port. I/O ports feature programmable polarity, programmable direction (Bit mode), "pulse catchers," and programmable open-drain outputs.
- Four handshake modes, including 3-Wire (like the IEEE-488).
- REQUEST/$\overline{\text{WAIT}}$ signal for high-speed data transfer.
- Flexible pattern-recognition logic, programmable as a 16-vector interrupt controller.
- Three independent 16-bit counter/timers with up to four external access lines per counter/timer (count input, output, gate, and trigger), and three output duty cycles (pulsed, one-shot, and square-wave), programmable as retriggerable or nonretriggerable.
- Easy to use since all registers are read/write.

General Description

The Z8536 CIO Counter/Timer and Parallel I/O element is a general purpose peripheral circuit, satisfying most counter/timer and parallel I/O needs encountered in system designs. This versatile device contains three I/O ports and three counter/timers. Many programmable options tailor its configuration to specific applications. The use of the device is simplified by making all internal registers (command, status, and data) readable and (except for status bits) writable. In addition, each register is given its own unique internal address, so that any register can be accessed in two operations. All data registers can be directly accessed in a single operation. The CIO is easily interfaced to all popular microprocessors.

Z8581 Clock Generator and Controller



FEATURES

- Two independent 20 MHz oscillators generate two 10 MHz clock outputs and one 20 MHz clock output.
- Oscillator input frequency sources can be either crystals or external oscillators.
- Outputs directly drive the Z80, Z8000, 8086, 8088, and 68000 microprocessor clock inputs.
- Can be used as a general purpose clock generator.
- 18-pin slimline package used; single +5V dc power required.
- Provides ability to stretch High and/or Low phase of clock signal under external control.
  - On-chip 2-bit counter can be used to selectively stretch clock cycles.
- On-chip reset logic
  - Reset output is synchronized with System Clock output.
  - Power-up reset period is maintained for a minimum of 30 ms.
  - External input initiates system reset.

GENERAL DESCRIPTION

The Z8581 Clock Generator and Controller is a versatile addition to Zilog's family of Universal microprocessor components. The selective clock-stretching capabilities and variety of timing outputs produced by this device allow it to easily meet the timing design requirements of systems with microprocessors and LSI peripherals. The clock output drivers of the Z8581 also meet the non-TTL voltage requirements for driving NMOS clock inputs with no additional external components. The Z8581 provides an elegant, single-chip solution to the design of system clocks for microprocessor-based products.

The Z8581 oscillators are referenced as the system clock oscillator and the general purpose clock oscillator. Both oscillators are driven by external crystals or other frequency sources.

Zilog's Quality and ReliabilityProgram

Introduction
The Zilog corporation has an excellent reputation for quality and reliability in its products. We recognize that the expecta - tion of our customers is increasing.

Zilog's Quality and Reliability Program is based on careful study of the principles laid down by such pioneers as W.E. Deming and J.M. Juran and, perhaps even more important, observation of the practical implementation of those principles in Japanese, European and American manufacturing facilities.

The Zilog program begins with employee involvement. Whether the judgement of our performance is based on perfection in incoming inspection, trouble-free service in the field or timely and accurate customer service, we recongnize that our employees ultimately control these factors. Hence, our Quality Program is broadly shared throughout the organization.

1. Harmony Between Design and Process
High product quality and reliability in VLSI products is possible only if there is structural harmony between product design and the manufacturing process. Great care is taken to assure that the statistical process control limits observed within the manufacturing plants properly guardband the design technology used to configure the circuit and layout in Zilog's automated design methodology.

By use of a technique which we call Process Templating, the technology file in the automated design system periodically is updated to assure that product design parameters fall within the statistical control limits with which the process is actually operated.

In simple terms, the Process Template is the profile displayed by the process evaluation parameters which are automatically recorded from the test patterns on wafers as they proceed through the production line. These parameters are translated into the design technology file attributes such that the product design bears a key and lock relationship with the process.

2. Training
Product Design and Processing are people-dependent. Zilog training emphasizes the fundamentals involved in design for quality and reliability.

Customer Service, an important aspect of Zilog's quality performance as a vendor, also depends upon our people clearly understanding their jobs, and our obligations to our customers. This too is part of the curriculum administered by Zilog.

3. Order Acknowledgement Policy
One definition of vendor quality performance is that the vendor "does what he promises or acknowledges." Reliability and quality warranties can be met only if Zilog and the customer agree on product and delivery specifications. Zilog makes an extra effort by providing a series of documents as part of its purchase order acknowledgements. These clearly state what Zilog understands the specifications to be.

4. Test Guardbanding
No physical attribute is absolute. Customers' test methods may differ from Zilog's due to variations in test equipment, temperature or specification interpretation. To assure that every Zilog product performs to full customer expectations, Zilog uses a "waterfall" methodology in its testing. The earliest electrical tests made on the circuit, at the wafer probe operations, are guardbanded to the final test specifications. Final test specifications are guardbanded to the quality control outgoing sample. The quality control outgoing sample is guardbanded to the customer procurement or data sheet specifications. This technique of "waterfall" guardbanding assures that circuits which may be marginal to the customer's expectations are eliminated in the manufacturing process long before they get to the shipping container.

5. Probe at Temperature
Semiconductor devices tend to exhibit their most limited performance at the highest operating temperature. Therefore, it is Zilog's policy that all chips are tested at high temperature the very first time they are electrically screened, at the wafer probe station. The circuits are tested again at their upper operating temperature limit in the 100% final test operation.

6. Process Characterization
Before release to production, every process is thoroughly characterized by an exhaustive series of pilot production runs and tests which identify the statistical, electrical, and mechanical limits of which that particular process regime is capable. This documentation, which fills a large looseleaf binder for each process, is maintained as the historical record or "footprint" for that particular regime.

Process recharacterization is done any time there is a major process or manufacturing site change, and that documentation is added to the characterization history. The daily test site evaluation work recorded in the process template noted earlier in this presentation, demonstrates that the process remains in specification between times of formal characterization.

7. Product Characterization
Every Zilog product design is evaluated over extremes of operating temperature, supply voltage and clock frequency, prior to release to production. This information permits the proper guardbanding of the test program waterfall and identification of any marginal "corners" in design tolerances.

A product characterization report, which summarizes the more important tolerances identified in the process of this exhaustive product design evaluation, is available to Zilog's customers.

8. Process Qualification
Just as Zilog measures the robustness and reliability of its products by a qualification process separate from the performance characterization process, Zilog also qualifies every process prior to production by an exhaustive stress sequence performed on test chips and on representative products. Once a process regime is qualified, a process requalification is performed any time there is a major process change, or whenever the process template statistical quality limits are significantly exceeded or adjusted.

9. Product Qualification
In addition to characterization, every new Zilog product design is fully qualified by a comprehensive series of life, electrical, and environmental tests before release to production. Again, a qualification report is available to our customers which summarizes certain key life and environmental data taken in the course of these evaluations. Whenever possible, industry standard environmental and life tests are employed.

10. PPM Measurement, Direct and Indirect
It is frequently said that if you want to improve something, you need to put a measure on it. Therefore, Zilog measures its outgoing quality "parts per million" by the maintenance of careful records on the statistical sampling of production lots prepared for shipment. This information is then translated by our statisticians to a statement of our parts per million (or parts per billion) outgoing quality performance.

Of course, it is one thing for Zilog to think it is doing a good job in outgoing product quality and it is another for a customer to agree. Therefore, we ask certain key customers to provide us with their incoming inspection data which helps us calibrate our own outgoing performance in terms of the actual results in the field. The fact that Zilog has been awarded "ship to stock" status by many customers testifies to our success in this area.

11. Field Quality Engineers
It is also frequently said that "the customer is always right." If the customer has an application quality or reliability problem while using a Zilog product, whether it is Zilog's responsibility or not, we believe that we

have a responsibility to resolve it. Therefore, Zilog maintains a force of skilled Applications Engineers who are also trained as field quality engineers and are available on immediate call to consult at the customers' locations on any problems they may be experiencing with Zilog product performance.

12. Product Analysis
As noted earlier, we feel that a customer problem is a Zilog problem. Accordingly, Product Analysis facilities, staffed by experienced professionals, exist at each Zilog site to provide rapid evaluation of in-process and in-field rejects to determine the cause and provide corrective action through a feedback loop into the production, design, and applications process. Zilog is pleased to share product analysis reports on specific products with the customer upon request.

13. FIT Measurement Direct and Indirect
Just as Zilog records its outgoing quality in terms of parts per million, it also measures its outgoing product reliability in terms of "FITS" or failures per billion device hours, using the results of weekly operating life test measurements on the circuits, performed in accordance with the standard specifications.

14. Test Site Step-Stress
The process evaluation test sites on the wafer are packaged and subjected to step-stress testing. Any drift in parameters under severe conditions of stress outside the norm is taken as an indication of possible process contamination or variation.

15. Statistical Process Control
Zilog employs statistical Process Control at all critical process steps. Deviations from norms must be evaluated by a Q/R review board.

16. Document Control
Skilled quality control professionals maintain careful and up-to-date specifications on all aspects of Zilog's products and processes in an elaborate document control system administered and controlled from the Zilog headquarters site. Specification changes and updates are electronically transmitted to the factory floor in order to assure that processing operations are being performed to the most up-to-date specifications. We are pleased to have a customer audit of this system at any time.

Zilog's Quality and Reliability Summary

Zilog's Quality and Reliability program employs effective controls and gates. All quality control monitors are documented to ensure consistency of test methods, testing frequency, sample selection, sampling plan, reject disposition, and reporting format. Statistical Quality Control (SQC) charts are used to record the monitor results. This form of record keeping is used to ensure minimum process variation in such operations as ion-implant, diffusion, delineation, wire bonding, and plastic molding.

Zilog subjects each lot of finished goods to an independent electrical and mechanical quality control audit prior to shipment.

ZiLOG Sales Representatives and Distributors

U.S., CANADIAN & PUERTO RICAN REPRESENTATIVES

ALABAMA
Huntsville
Electronic Sales, Inc. . . . . (205)533-1735

ARIZONA
Scottsdale
Thom Luke Sales, Inc. . . . . (602)941-1901

CALIFORNIA
San Diego
Earle Associates, Inc. . . . . (619)278-5441
Santa Ana
Jones & McGeoy Sales, Inc. . . . . (714)547-6466
Van Nuys
Jones & McGeoy Sales, Inc. . . . . (818)994-6500

COLORADO
Englewood
Thorson Rocky Mountain . . . . . (303)799-3435

CONNECTICUT
Woodbury
Lindco Associates, Inc. . . . . (203)266-0728

FLORIDA
Cassleberry
Dyne-A-Mark Corp. . . . . (305)831-2822
Clearwater
Dyne-A-Mark Corp. . . . . (813)441-4702
Dade
Dyne-A-Mark Corp. . . . . (305)994-5031
Fort Lauderdale
Dyne-A-Mark Corp. . . . . (305)771-6501
Palm Beach
Dyne-A-Mark Corp. . . . . (305)276-0070

GEORGIA
Norcross
Electronic Sales, Inc. . . . . (404)448-6554

ILLINOIS
Northbrook
Dolin Sales Company . . . . . (312)498-6770

INDIANA
Indianapolis
SAI Marketing Corp. . . . . (317)545-1010

IOWA
Cedar Rapids
Advanced Technical Sales . . . . . (319)393-8280

KANSAS
Olathe
Advanced Technical Sales . . . . . (913)782-8702

MARYLAND
Severna Park
New Era Sales . . . . . (301)544-4100

MASSACHUSETTS
North Reading
Advanced Tech Sales . . . . . (508)664-0888

MICHIGAN
Grand Rapids
Rathsburg Associates Inc. . . . . (616)949-7400
Southfield
Rathsburg Associates Inc. . . . . (313)559-9700

MINNESOTA
Minneapolis
Professional Sales for Industry . . . . . (612)944-8545

MISSOURI
St. Louis
Advanced Technical Sales . . . . . (314)878-2921

NEW JERSEY
Haddonfield
Tritek Sales, Inc. . . . . (609)429-1551

NEW MEXICO
Albuquerque
Quatra Associates . . . . . (505)821-1455

NEW YORK
Commack
ERA, Inc. . . . . (516)543-0510
East Rochester
L-Mar Associates, Inc. . . . . (716)381-9100

NORTH CAROLINA
Cary
Electronic Sales, Inc. . . . . (919)467-8486

OHIO
Columbus
SAI Marketing Corp. . . . . (614)451-0778
Dayton
SAI Marketing Corp. . . . . (513)435-3181
Warrensville Heights
SAI Marketing Corp. . . . . (216)591-0530

OKLAHOMA
Tulsa
Nova Marketing, Inc. . . . . (918)660-5105

OREGON
Portland
Northwest Marketing Associates Inc. . . . . (503)620-0441

TEXAS
Austin
Nova Marketing, Inc. . . . . (512)343-2321
Dallas
Nova Marketing, Inc. . . . . (214)750-6082
Houston
Nova Marketing, Inc. . . . . (713)988-6082

UTAH
Salt Lake City
Thorson Rocky Mountain . . . . . (801)973-7969

WASHINGTON
Bellevue
Northwest Marketing Associates Inc. . . . . (205)455-5846

WISCONSIN
Milwaukee
Dolin Sales Company . . . . . (414)482-1111

CANADA
Calgary
Hi-Tech Sales, Ltd. . . . . (403)239-8518
St. Laurent
Electronic Sales Professionals . . . . . (514)737-9344
Mississauga
Electronic Sales Professionals . . . . . (416)626-8221
Ottawa
Electronic Sales Professionals . . . . . (613)236-1221
Surrey
Hi-Tech Sales, Ltd. . . . . (604)596-1886
Winnipeg
Hi-Tech Sales, Ltd. . . . . (204)694-0000

PUERTO RICO
San Juan
Electronic Technical Sales . . . . (809)720-1300

Sales Representatives and Distributors

U.S. AND CANADIAN DISTRIBUTORS

ALABAMA

Huntsville
Hall-Mark Electronics.....(205)837-8700
Schweber Electronics.....(205)895-0480

ARIZONA

Phoenix
Hall-Mark Electronics.....(602)437-1200
Tempe
Schweber Electronics.....(602)431-0030
Anthem Electronics.....(602)966-6600

CALIFORNIA

Calabasas
Schweber Electronics.....(818)880-9686
Chatsworth
Anthem Electronics.....(818)700-1000
Hall-Mark Electronics.....(818)773-4500
Irvine
Anthem Electronics.....(714)768-4444
Schweber Electronics.....(714)863-0200
Hall-Mark Electronics.....(714)727-6000
Reseda
JAN Devices, Inc.....(818)708-1100
Rocklin
Hall-Mark Electronics.....(916)624-9781
Rockwell
Anthem Electronics.....(916)624-9744
Sacramento
Schweber Electronics.....(916)364-0222
San Diego
Anthem Electronics.....(619)453-9005
Hall-Mark Electronics.....(619)268-1201
Schweber Electronics.....(619)495-0015
San Jose
Anthem Electronics.....(408)453-1200
Hall-Mark Electronics.....(408)432-4000
Schweber Electronics.....(408)432-7171
Saratoga
Western Microtechnology.....(408)725-1660

COLORADO

Englewood
Anthem Electronics.....(303)790-4500
Hall-Mark Electronics.....(303)790-1662
Schweber Electronics.....(303)799-0258

CONNECTICUT

Cheshire
Hall-Mark Electronics.....(203)271-2844
Merriden
Anthem Electronics.....(203)237-2282
Oxford
Schweber Electronics.....(203)264-4998

FLORIDA

Altamonte Springs
Schweber Electronics.....(407)331-7555
Casselberry
Hall-Mark Electronics.....(407)830-5855
Largo
Hall-Mark Electronics.....(813)541-7440
Schweber.....(813)541-5100
Pompano Beach
Schweber Electronics.....(305)997-7511
Hall-Mark Electronics.....(305)971-9280

GEORGIA

Norcross
Hall-Mark Electronics.....(404)447-8000
Schweber Electronics.....(404)449-9170

ILLINOIS

Elk Grove Village
Anthem Electronics.....(312)640-6066
Schweber Electronics.....(312)364-3750
Wood Dale
Hall-Mark Electronics.....(312)860-3800

INDIANA

Indianapolis
Hall-Mark Electronics.....(317)872-8875
Schweber Electronics.....(317)843-1050

IOWA

Cedar Rapids
Schweber Electronics.....(319)373-1417

KANSAS

Lenexa
Hall-Mark Electronics.....(913)888-4747
Overland Park
Schweber Electronics.....(913)492-2922

MARYLAND

Columbia
Anthem Electronics.....(301)995-6640
Hall-Mark Electronics.....(301)988-9800
Schweber Electronics.....(301)596-7800

MASSACHUSETTS

Bedford
Schweber Electronics.....(617)275-5100
Billerica
Hall-Mark Electronics.....(508)667-0902
Wilmington
Anthem Electronics.....(508)657-5170

MICHIGAN

Livonia
Hall-Mark Electronics.....(313)462-1205
Schweber Electronics.....(313)525-8100

MINNESOTA

Eden Praire
Anthem Electronics.....(612)944-5454
Hall-Mark Electronics.....(612)941-2600
Edina
Schweber Electronics.....(612)941-5280

MISSOURI

Earth City
Hall-Mark Electronics.....(314)291-5350
Schweber Electronics.....(314)739-0526

NEW HAMPSHIRE

Manchester
Schweber Electronics.....(603)625-2250

NEW JERSEY

Fairfield
Anthem Electronics.....(201)227-7960
Hall-Mark Electronics.....(201)575-4415
Schweber Electronics.....(201)227-7880
Mt. Laurel
Hall-Mark Electronics.....(609)235-1900

NEW YORK

Hauppauge
Anthem Electronics.....(516)273-1660
Fairport
Hall-Mark Electronics.....(716)425-3300
Rochester
Schweber Electronics.....(716)424-2222
Ronkonkoma
Hall-Mark Electronics.....(516)737-0600
Westbury
Schweber Electronics.....(516)334-7474

ZiLOG Sales Representatives and Distributors

NORTH CAROLINA

Raleigh
Hall-Mark Electronics.....(919)872-0712
Schweber Electronics.....(919)876-0000

OHIO

Beachwood
Schweber Electronics.....(216)464-2970
Dayton
Schweber Electronics.....(513)439-1800
Solon
Hall-Mark Electronics.....(216)349-4632
Worthington
Hall-Mark Electronics.....(614)888-3313

OKLAHOMA

Tulsa
Schweber Electronics.....(918)622-8000
Hall-Mark Electronics.....(918)254-6110

OREGON

Beaverton
Anthem Electronics.....(503)643-1114
Western Microtechnology.....(503)629-2082

PENNSYLVANIA

Horsham
Anthem Electronics.....(215)443-5150
Schweber Electronics.....(215)441-0600
Pittsburgh
Schweber Electronics.....(412)963-6804

TEXAS

Austin
Hall-Mark Electronics.....(512)258-8848
Schweber Electronics.....(512)339-0088
Dallas
Hall-Mark Electronics.....(214)553-4300
Schweber Electronics.....(214)661-5010
Houston
Hall-Mark Electronics.....(713)781-6100
Schweber Electronics.....(713)784-3600
Richardson
Anthem Electronics.....(214)238-7100

UTAH

Salt Lake City
Anthem Electronics.....(801)973-8555
West Valley City
Hall-Mark Electronics.....(801)972-1008

WASHINGTON

Bothel
Anthem Electronics.....(206)443--1700
Redmond
Western Microtechnology.....(206)881-6737

WISCONSIN

New Berlin
Hall-Mark Electronics.....(414)797-7844
Schweber Electronics.....(414)784-9020

CANADA

Burnaby
Semad.....(604)420-9889
Calgary
Semad.....(403)252-5664
Future Electronics.....(403)235-5325
Downsview
Future Electronics.....(416)638-4771
Edmonton
Future Electronics.....(403)438-2858
Markham
Semad.....(416)475-8500
Ottawa
Future Electronics.....(613)820-8313
Semad.....(613)727-8325
Pointe Claire
Future Electronics.....(514)694-7710
Semad.....(514)694-0860
St. Foy
Future Electronics.....(418)682-8092
Vancouver
Future Electronics.....(604)294-1166
Winnipeg
Future Electronics.....(204)786-7711

Sales Representatives and Distributors

EUROPE

AUSTRIA

VIENNA
EBV Elektronik.....(43)222838519
Nowatron Instruments.....(43)2226925310

BELGIUM

ANTWERP
D&D Electronics.....(32)38277934

DENMARK

BRONDBY
Ditz Schweitzer AS.....(45)2453044

ENGLAND

BERKSHIRE
Celdis.....(44)734585171
Gothic Crellon.....(44)734787848
Macro Marketing Limited.....(44)628604383
SURREY
Microlog Ltd.....(44)486229551

FINLAND

ESPOO
OY SW Instruments, AB.....(358)08041041

FRANCE

LE CHESNAY
A2M.....(33)139549113
Almex Zi D'Antony.....(33)146662112

GREECE

ATHENS
Microsystems.....(30)19025786

ISRAEL

TEL AVIV
RDT.....(972)35483737

ITALY

MILANO
Dott.Ing. Giuseppe De Mico SPA.....(39)29520551

NETHERLANDS

ZOETERMEER
Tekelec Airtronic BV.....(31)79310100

NORWAY

OSLO
Hefro Elektronikk A/S.....(47)2107300

SPAIN

MADRID
Unitronics SA.....(34)15425204

SWEDEN

SOLNA
AB Nordqvist & Berg.....(46)87646710

SWITZERLAND

REGENSDORF
W Moor AG.....(41)18433287

ZURICH
Kontron Electronics AG.....(41)14354445

WEST GERMANY

AICHTAL
Neumueller GMBH.....(49)712750878
BERLIN
Distron (EBV).....(49)303421041
Neumueller GMBH.....(49)30247212
BURGWEDEL
EBV Elektronik.....(49)513980870
DORTMUND
Neumueller GMBH.....(49)231271671
EDEMISSEN
Neumueller GMBH.....(49)51771533
FRANKFURT
EBV Elektronik.....(49)69785037
MUNICH
Alfatron GMBH.....(49)893290990
NeumuellerGMBH.....(Toll Free)(49)0130/4044
HAMBURG
Alfatron GMBH.....(49)4068295122
HATTERSHEIM
Neumueller GMBH.....(49)619071168
LEONBERG
Alfatron GMBH.....(49)715221067
NEUSS
EBV Elektronik.....(49)2101530072
Alfatron GMBH.....(49)210121093
NIEFERN
Neumueller GMBH.....(49)72331897
NURNBURG
Alfatron GMBH.....(49)9115190822
ROEDERMARK
Alfatron GMBH.....(49)06074900012
STUTTGART
EBV Elektronik.....(49)711619100
TAUFKIRCHEN
Neumueller GMBH.....(49)89612080
UNTERHACHING
EBV Elektronik.....(49)89611051

ZiLOG Sales Representatives and Distributors

ASIA-PACIFIC

AUSTRALIA

NSW

R & D Electronics.....(61)-2-7123855
George Brown & Co Pty Ltd.....(61)-2-5195855

VICTORIA

R & D Electronics.....(61)-3-2888911
George Brown & Co Pty Ltd.....(61)-3-8788111

HONG KONG

KOWLOON

Electrocon Products Ltd.....(852)-3-687214
Lestina International Ltd.....(852)-3-7231736

INDIA

BANGALORE

American Components Inc.....(812)-28747

BOMBAY

American Components Inc.....(22)-2040452

NEW DELHI

American Components Inc.....(11)-644-9195

SECUNDERABAD

American Components Inc.....(842)-822385

USA

American Components Inc.....(408)-727-2440

KOREA

SEOUL

ENC Korea.....(82)-2-5875723

NEW ZEALAND

AUCKLAND

Microcomputer Elect Co Ltd.....(64)-9-504774

TAIWAN (ROC)

TAIPEI

Princeton Tech Corp.....(886)-2-7171439
Ramtek Enterprise Co.....(886)-2-776 3512
Sertek International Inc.....(886)-2-5010055

SINGAPORE

SINGAPORE

Eltee Electronics PTE Ltd.....(65)-2850633

JAPAN

TOKYO

Internix Inc. .....(81)-3-369-1105
Teksel Co Ltd.....(81)-3-461-5121
Kanematsu Elect Comp Corp.....(81)-3-779-7811
Systems Marketing Inc.....(81)-3-254-2751

LATIN AMERICA

ARGENTINA

Yel.....(1)-46-2211

BRAZIL

SÃO PAULO

Digibyte.....(011)-581-1945

MEXICO

Semiconductores Profesionales.....(5)-536-1312

(408)453-1200 (408)432-4000

Irvine
Hall-Mark Electronics.....(714)727-6000

Largo
Hall- Mark Electronics.....(813)541-7440
Schweber.....(813)541-5100

(508)935-9777 (508)657-5170

Z8/Super8 Microcomputer Family	Part No	Unit Cost
Z8 Design Handbook	03-8275-03	5.00

Z8 NMOS MCU MICROCOMPUTERS
Z8600 Z8 MCU 2K 28-pin Product Spec
Z8601/03/11/13 Z8 MCU 2K/4K Product Spec
Z8671 MCU with Basic/Debug Interpreter
Z8681/82 Z8 MCU ROMless Product Spec
Z8691 Z8 MCU ROMless Product Spec
Super8 MCU ROMless Product Spec

Z8 CMOS MICROCOMPUTERS
Z86C08 MCU 2K 18-pin Product Spec
Z86C00/C10/C20 MCU 4K/8K 28-pin OTP Pd Spec
Z86C11/ MCU 4K
Z86C21/Z86E21/C12 8K/OTP Product Spec
Z86C91 MCU ROMless

Z8 APP NOTES AND TECHNICAL ARTICLES
Memory Space and Register Org App Note
A Programmer's Guide to the Z8 MCU
Z8 Subroutine Library
A Comparison of MCU Units
Z86xx Interrupt Request Registers
Z8 Family Framing

Z8 MCU Technical Manual

SUPER8 MCU MICROCOMPUTER
Z8800/01 MCU ROMless
Z8820 MCU 8K
Z8822 MCU 8K Protopak

SUPER8 APP NOTES AND TECHNICAL ARTICLES
Getting Started with the Zilog Super8
Polled Async Serial Operations with the Super8
Using the Super8 Interrupt Driven Communications
Using the Super8 Serial Port with DMA
Generating Sine Waves with Super8
Generating DTMF Tones with Super8
A Simple Serial Parallel Converter Using the Super8

Other Z8 Literature	Part No	Unit Cost
Z8 Basic/Debug Software Manual	03-3149-03	3.00
Univ Obj File Utilities User's Manual	00-8236-04	3.00
ASM8 Cross Assembler User's Guide	00-8267-04	3.00

Z80/Z280 Microprocessor Family	Part No	Unit Cost
Z80 Family Data Book	00-2480-01	5.00

Z80 NMOS/CMOS MICROCOMPUTERS
Z84C00 NMOS/CMOS Z80 CPU Prelimin Product Spec
Z84C01 Z80 CPU w/CTC
Z84C10 NMOS/CMOS Z80 DMA Product Spec
Z84C20 NMOS/CMOS Z80 PIO Product Spec
Z84C30 NMOSCMOS Z80 CTC Product Spec
Z84C40 NMOS/CMOS Z80 SIO Product Spec
Z84C50 RAM 80 Product Spec
Z8470 DART
Z84C80 Product Spec
Z84C90 CMOS Z80 KIO Product Spec
Z80180 Z180 MPU
Z280 MPU Preliminary Product Spec

Z80 APP NOTES AND TECHNICAL ARTICLES
Z80 Interrupt Structure
Using the Z80 SIO in Async Communications
Using the Z80 SIO with SDLC
Binary Synchronous Comm Using the Z80 SIO
Timing in Interrupt-Based System with Z80 CTC
Interfacing Z80 CPU's to the Z8500 Periph Family
A Z80 Based System Using the DMA with SIO
Z80 Q&A's
Package Information
Literature List
PSI List
Ordering Information

Z80 Technical Manuals	Part No	Unit Cost
Z80 CPU Technical Manual	03-0029-03	3.00
Z80 CPU Programmer's Ref Guide	03-0012-04	3.00
Z80 DMA Technical Manual	00-2013-02	3.00
Z80 PIO Technical Manual	03-0008-02	3.00
Z80 CTC Technical Manual	03-0036-02	3.00
Z80 SIO Technical Manual	03-3033-01	3.00
Z180 Technical Manual	03-8276-01	3.00
Z280 Technical Manual	03-8224-02	30.0

Literature Guide (Continued)

Z8000/80,000 Microprocessor Family	Part No	Unit Cost
Z8000 Family Data Book	**00-2488-01**	**5.00**
Z8000/80,000 NMOS/CMOS MICROS		
Z160 CPU Product Spec		
Z5380 CMOS SCSI Product Spec		
Z7220A HPGD Product Spec		
Z765A FDC Product Spec		
Z8001/Z8002 CPU Product Spec		
Z8010 MMU Product Spec		
Z8016 Z-DTC Product Spec		
Z16C20 CMOS Z-BUS GLU		
Z80C30/Z85C30 CMOS SCC Product Spec		
Z8030/8530 SCC Product Spec		
Z8036/Z8535 CIO Technical Manual		
Z8536 CIO Product Spec		
Z8038/8538 FIO FIFO Product Spec		
Z8060/8560 FIFO Product Spec		
Z8068 Z-DCP Product Spec		
Z8516 DMA (DTC) Product Spec		
Z8581 Clock Generator Product Spec		
APP NOTES AND TECHNICAL ARTICLES		
Interfacing Z80 CPUs to Z8500 Peripheral Family		
Interfacing the Z8500 Peripheral to 68000		
Design Considerations Using Quartz Crystals		
Using Z8581 Clock Stretches in Z80 CPU Apps		
Interfacing Z-BUS Periph. to the V20/V30/8086/8088		
Interfacing the Z-BUS Peripherals Articles Reprint		
Using SCC with Z8000 in SDLC Protocol		
SCC in Binary Synchronous Communications		
Z8000 Development Support		
Zilog Quality and Reliability		
Literature Guide		
Ordering Information		

Z8000/80,000 Technical Manuals	Part No	Unit Cost
Z8000 CPU Technical Manual	**00-2010-06**	**3.00**
Z8010 MMU Technical Manual	**00-2015-A0**	**3.00**
Z8030/Z8530 SCC Technical Manual	**00-2057-06**	**3.00**
Z8036/28536 CIO Technical Manual	**00-2091-02**	**3.00**
Z8038 Z-FIO Technical Manual	**00-2051-01**	**3.00**
Z80,000 Technical Manual	**03-8225-01**	**3,00**
Z8000 Programmer's Pocket Guide	**03-0122-03**	**3.00**
Memory Management w/Z80,000 Apps Note	**00-2324-01**	**N/C**

Components Military Literature	Part No	Unit Cost
Zilog Military Products Binder	**00-5498-01**	**8.00**
Z8681 ROMless Military Spec	00-2392-02	
Z800 1/2 CPU Military Spec	00-2342-03	
Z851 CGC Military Spec	00-2346-01	
Z8030 Z-SCC Military Spec	00-2388-01	
Z8530 SCC Military Spec	00-2397-01	
Z8036 Z-CIO Military Spec	00-2389-01	
Z8038/8538 FIO FIFO Military Spec	00-2463-02	
Z8536 CIO Military Spe	00-2396-01	
Z8400 Z80 CPU Military Spec	00-2351-02	
Z84C00 Military Spec	00-2441-03	
Z8420 PIO Military Spec	00-2384-01	
Z8430 CTC Military Spec	00-2385-01	
Z8440/1/2/4 Military Spec	00-2386-01	
Z80C30/85C30 Military Product Spec	00-2478-01	
Z84C20 PIO CMOS Military Spec	00-2384-02	
Z84C30 CTC CMOS Military Spec	00-2481-01	
Z84C40/1/2/4 SIO CMOS Military Spec	00-2482-01	

Note: Military Specs may be ordered individually at no charge.

General Literature	Part No	Unit Cost
Component Short Form Catalog	**00-5472-05**	**N/C**
Reliability Handbook	**00-2475-02**	**N/C**
Superintegration Brochure	**00-2493-01**	**N/C**
Corporate Profile	**00-3124-00**	**N/C**
Superintegration Products Guide	**00-5499-01**	**N/C**

New Product Preliminary Specs	Part No	Unit Cost
Z86E21 OTP	**00-2487-01**	**N/C**
Z16C30 USC	**00-2492-01**	**N/C**

ZILOG DOMESTIC SALES OFFICES AND TECHNICAL CENTERS

CALIFORNIA
Agoura 818-707-2160
Campbell 408-370-8120
Tustin 714-838-7800

COLORADO
Boulder 303-494-2905

FLORIDA
Largo 813-585-2533

GEORGIA
Norcross 404-923-8500

ILLINOIS
Schaumburg 312-517-8080

NEW HAMPSHIRE
Nashua 603-888-8590

MINNESOTA
Edina 612-831-7611

NEW JERSEY
Clark 201-382-5700

OHIO
Seven Hills 216-447-1480

PENNSYLVANIA
Ambler 215-653-0230

TEXAS
Dallas 214-987-9987

INTERNATIONAL SALES OFFICES

CANADA
Toronto 416-673-0634

GERMANY
Munich 49-89-672-045

JAPAN
Tokyo 81-3-587-0528

HONG KONG
Kowloon 852-3-723-8979

KOREA
Seoul 82-2-552-5401

SINGAPORE
Singapore 65-235-7155

TAIWAN
Taipei 886-2-741-3125

UNITED KINGDOM
Maidenhead 44-628-392-00

Zilog, Inc. 210 Hacienda Ave., Campbell, CA 95008-6609
Telephone (408) 370-8000 TWX 910-338-7621

00-5472-05