Interfacing Static R/W Memories to the 8080A

Addressing Techniques

The INS8080A has a 16-bit address bus that is capable of addressing up to 65k bytes of memory and up to 256 input and 256 output devices. In small systems with minimum memory and input/output requirements, buffering of the A_{15}-A_0 Address Bus may not be required. However, as memory and input/output device requirements increase, buffering is required for the bus. This address buffering function can be implemented by using two National Semiconductor DM81LS95 TRI-STATE Octal Buffers as shown in figure 1. Note that the system Bus Enable (BUSEN) signal is connected to the buffers so that they are forced into their high-impedance state during a DMA data transfer (BUSEN = logic 1) or any other time that bus access is desired, thereby allowing other devices to gain access of the address bus. As mentioned above, up to 65k bytes of memory and up to 256 input and 256 output devices can be directly addressed via the A_{15}-A_0 Address Bus of the INS8080A. The INS8080A microcomputer system can be configured so that memory and input/output devices are either treated separately (isolated input/output) or as a single memory array (memory mapped input/output) as described below. The mapping for the isolated input/output and memory mapped input/output addressing techniques is shown in figure 2. With both of these addressing techniques, the most common method of addressing memory or input/output devices is to decode some of the address bus bits as "chip selects" (using a device such as the National Semiconductor 74LS138) to enable the addressed memory or the input/output device. The linear select method is another way of addressing the input/output devices using either of the addressing techniques. In linear select, a singular address bus bit is assigned as the exclusive enable for a specified input/output device. Using this method limits the number of input/output devices that can be addressed but eliminates the need for extra decoders. In small system design this is an important consideration.

When the INS8080A system is configured for isolated input/output addressing, the memory address space is separated from the Input/output device's address space by using system control signals for the input/output architecture as shown in figure 3. Also, with isolated input/output addressing, the input/output devices communicate only with the Accumulator using the IN and OUT Instructions. Thus, since the memory address space is not affected by input/output device addressing, the full address space of 65k bytes is available for memory.

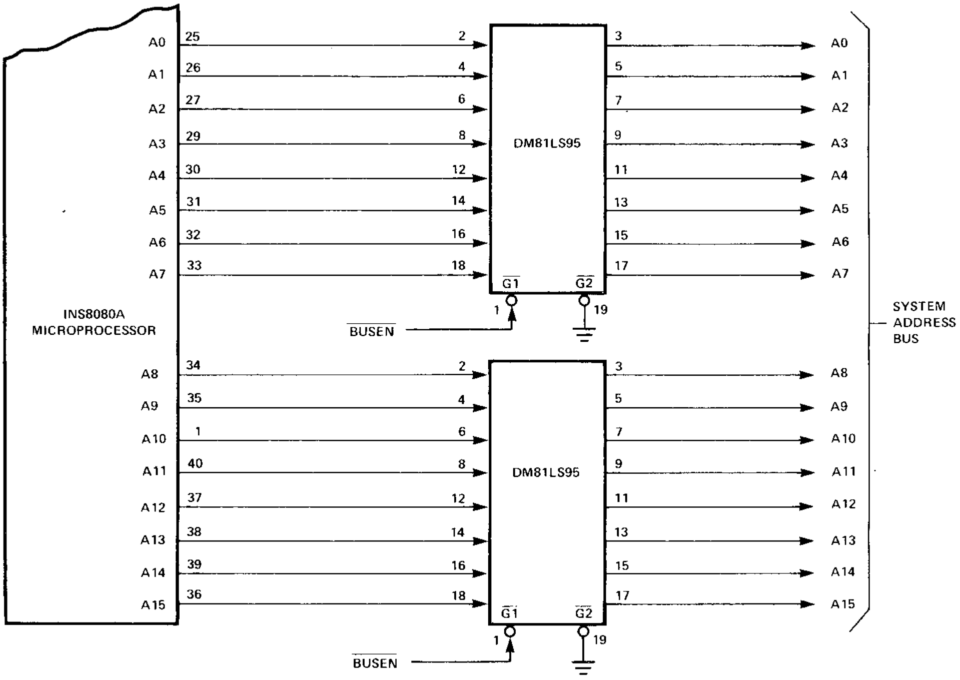

Figure 1. Address Buffer Design Using DM81LS95 Devices

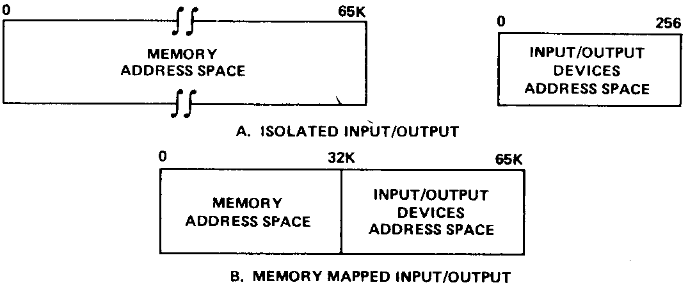
0
65K
MEMORY ADDRESS SPACE
0
256
INPUT/OUTPUT DEVICES ADDRESS SPACE
A. ISOLATED INPUT/OUTPUT
0
32K
65K
MEMORY ADDRESS SPACE
INPUT/OUTPUT DEVICES ADDRESS SPACE
B. MEMORY MAPPED INPUT/OUTPUT

Figure 2. Mapping for Isolated Input/Output and Memory Mapped Input/Output Techniques

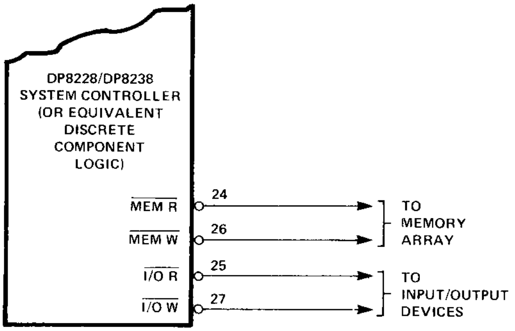
DP8228/DP8238 SYSTEM CONTROLLER (OR EQUIVALENT DISCRETE COMPONENT LOGIC)
$\overline{\text{MEM R}}$
$\overline{\text{MEM W}}$
$\overline{\text{I/O R}}$
$\overline{\text{I/O W}}$
24
26
25
27
TO MEMORY ARRAY
TO INPUT/OUTPUT DEVICES

Figure 3. System Control Signals for Isolated Input/Output Addressing

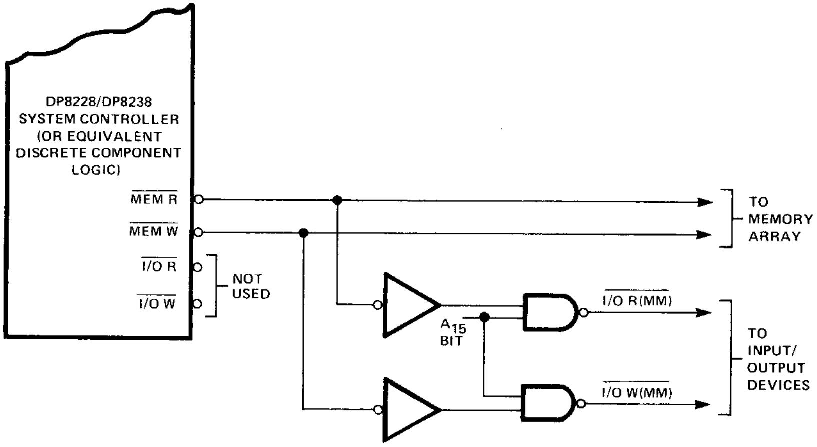
DP8228/DP8238 SYSTEM CONTROLLER (OR EQUIVALENT DISCRETE COMPONENT LOGIC)
$\overline{\text{MEM R}}$
$\overline{\text{MEM W}}$
$\overline{\text{I/O R}}$
$\overline{\text{I/O W}}$
NOT USED
A_{15} BIT
$\overline{\text{I/O R(MM)}}$
$\overline{\text{I/O W(MM)}}$
TO MEMORY ARRAY
TO INPUT/ OUTPUT DEVICES

Figure 4. System Control Signals for Memory Mapped Input/Output Addressing

When the INS8080A system is configured for memory mapped input/output addressing, an area of the memory array is assigned to the input/output devices by using system control signals for the input/output architecture as shown in figure 4. In this configuration, new input/output control signals [I/O R (MM) and I/O W (MM)] are generated by gating the MEM R and MEM W signals with most significant address bit A_{15}. (Since these new input/output signals connect in exactly the same manner as the corresponding signals of the isolated input/output configuration, the system bus characteristics are unaltered.) Address bit A_{15} is used because it allows up to 32k bytes of memory addressing, and because it is easier to control with software. However, any other address bit may be used for this gating function. When bit A_{15} is low, the memory address space is active and when bit A_{15} is high, the input/output device's address space is active.

With memory mapped input/output addressing, all of the instructions that can be used to manipulate memory locations (for example, MOV M, r; LDA; STA; LHLD; et cetera) can also be used for the input/output devices. These devices are still considered addressed "PORTS" but instead of the Accumulator being the only data transfer medium for the peripherals, any of the internal registers of the INS8080A can also be used for this purpose. Thus, memory mapped input/output addressing is suited for small systems that require high throughput and have less than 32k bytes of memory.

Memory Interfacing

The CPU group of the N8080 microcomputer family interfaces with standard semiconductor memory components (and input/output devices) via a 3-bus architecture that includes an 8-bit bidirectional External Data Bus, a 6-bit Control Bus, and a 16-bit Address Bus. A typical interface to a memory array having 8k bytes of ROM storage and 512 bytes of RAM storage is shown in figure 5. This typical memory interface is suitable for almost any size of memory array. However, in larger systems, buffers may be required for driving the three buses and decoders may be required for generating the chip select signals for the memory array (and input/output devices).

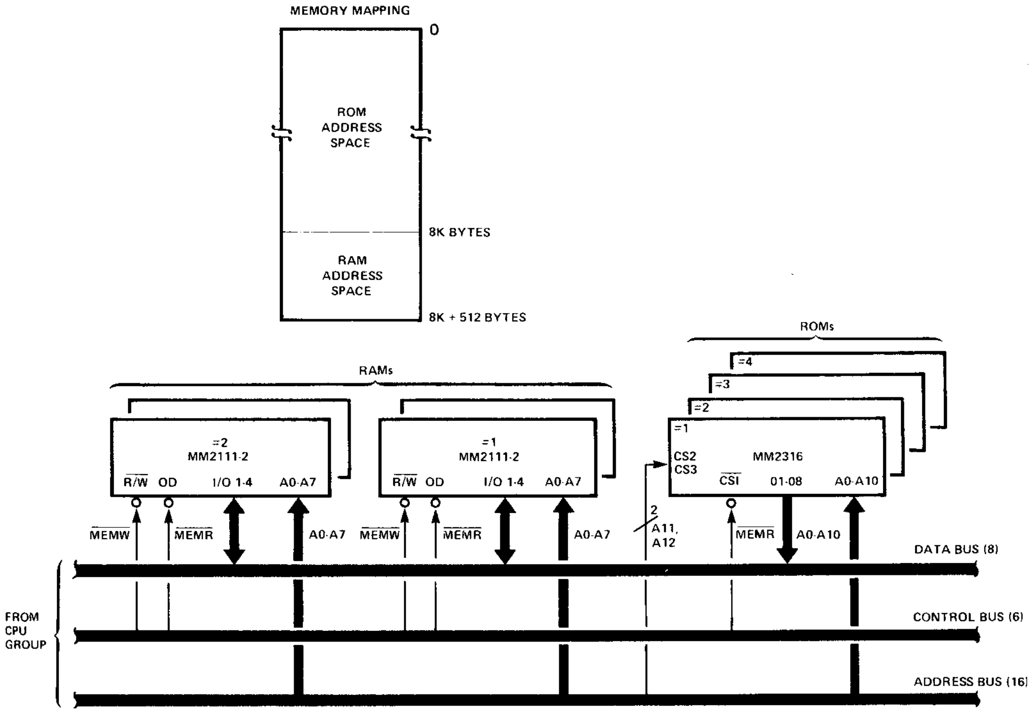

Figure 5. Typical Memory Interface

As shown in figure 5, the interfacing to the National Semiconductor MM2316 static ROMs is quite straightforward. The D_0-D_7 output lines of the ROMs are connected to the bidirectional External Data Bus; the A_0-A_{10} address inputs are connected to corresponding bits of the Address Bus; the CS2 and CS3 chip select inputs are connected to the A_{11} and A_{12} bits (most significant) of the Address Bus; and the CS1 chip select input of the ROMs is connected to the MEM R signal of the Control Bus. During a FETCH or MEMORY READ machine cycle, the CPU group may output an address in the ROM address space of the memory array. When this occurs, the data stored at the addressed ROM location are then gated onto the External Data Bus with a low-level MEM R signal. In this way, data are read from the ROMs in the INS8080A.

The interfacing to the four National Semiconductor MM2111-2 static RAMs is also straightforward. The I/O_1-I/O_4 common input/output lines of the RAMs are connected to corresponding bits of the bidirectional Data Bus; the A_0-A_7 address bits are connected to corresponding bits of the Address Bus; and the R/W and OD inputs of the RAMs are connected to the MEM W and MEM R (or DBIN) signals, respectively, of the Control Bus. During a FETCH, MEMORY READ, or STACK READ machine cycle, the CPU group reads data from the RAMs in exactly the same manner as described above for the ROMs. During a MEMORY WRITE or STACK WRITE machine cycle, the CPU group outputs an address in the RAM address space of the memory array. When this occurs, the data to be written into memory are then strobed into the addressed RAM location with a low-level MEM W signal. In these ways, data are read from and written into RAMs in the INS8080A microcomputer system.

The memory array of figure 5 includes ROMs (MM2316) and RAMs (MM2111-2) that have an access time of 850 nanoseconds (maximum). When the INS8080A microprocessor is operated from a clock generator with a t_{CY} of 500 nanoseconds, the required memory access time is from 450 to 550 nanoseconds. Therefore, to use the slower memory components in the system, the INS8080A microprocessor must contain a synchronization provision to allow the memory components to request the wait state (t_W). (The actual number of t_W states to be inserted is determined by external logic that is user designed.) This provision can be implemented for any slow memory (RAM or ROM) by a simple logic control of the READY input of the INS8080A as follows. When the addressed slower memory receives a MEM R or MEM W signal, it places a low-level on the READY line of the microprocessor, causing the INS8080A to enter the WAIT sequence. After the slower memory has had time to respond, it places a high-level on the READY line, thereby allowing completion of the instruction cycle.