

MC1 4499

A perspective view of a 14-pin DIP package. The package is black with a white top surface. The pins are numbered 1 to 18, with 1 at the bottom left and 18 at the top left.

A diagram of a 20-pin DIP package. The package is shown from a perspective view. The pins are numbered 1 to 20. Pin 1 is at the bottom center, and pin 20 is at the top center. The pins are arranged in two rows of 10 pins each.

MC14499P	Plastic DIP
MC14499DW	SOG Package

- | | | | |
|-----------------|---|----|-----------------|
| d | 1 | 18 | V _{DD} |
| c | 2 | 17 | e |
| b | 3 | 16 | f |
| a | 4 | 15 | g |
| DATA | 5 | 14 | h |
| OSC | 6 | 13 | CLK |
| IV | 7 | 12 | ENB |
| III | 8 | 11 | i |
| V _{SS} | 9 | 10 | II |

d	1	20	V _{DD}
c	2	19	e
b	3	18	f
a	4	17	g
DATA	5	16	h
OSC	6	15	CLK
IV	7	14	$\overline{\text{ENB}}$
III	8	13	i
V _{SS}	9	12	II
NC	10	11	NC

[illegible] **MOTOROLA**

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to $+7$	V
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	V
Storage Temperature Range	T_{stg}	-65 to $+150$	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics table or Circuit Operation section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS ($V_{DD} = 4.5$ to 6.5 V)

Characteristic	Symbol	0°C		25°C		70°C		Unit
		Min	Max	Min	Max	Min	Max	
Serial Port Input Voltage '0' Level '1' Level	V_{IL} V_{IH}	— $0.7 \times V_{DD}$	$0.3 \times V_{DD}$ —	— $0.7 \times V_{DD}$	$0.3 \times V_{DD}$ —	— $0.7 \times V_{DD}$	$0.3 \times V_{DD}$ —	V
Serial Port Input Current ($V_{in} = 0$ to V_{DD})	I_{in}	—	± 0.1	—	± 0.1	—	± 1.0	μA
Oscillator Input Voltage '0' Level '1' Level	V_{IL} V_{IH}	— $0.75 \times V_{DD}$	$0.25 \times V_{DD}$ —	— $0.75 \times V_{DD}$	$0.25 \times V_{DD}$ —	— $0.8 \times V_{DD}$	$0.2 \times V_{DD}$ —	V
Oscillator Input Current $V_{OSC} = 0$ $V_{OSC} = V_{DD}$	I_{IL} I_{IH}	— —	100 -100	30 -30	80 -80	10 -10	— —	μA
Segment Driver Voltage Below V_{DD} $I_{out} = 50$ mA $I_{out} = 10$ mA	ΔV_{OH}	— —	1.1 0.8	— —	1.0 0.75	— —	1.1 0.8	V
Segment Driver Off Leakage $V_{out} = 0$	I_{OZ}	—	100	—	50	—	100	μA
Digit Drivers Source (On) Sink (Off)	I_{OH} I_{OL}	6 -0.2	— —	5.5 -0.2	— —	4 -0.1	— —	mA
Supply Current $V_{in} = 0$, $I_{out} = 0$, $C_{OSC} = 0.015$ μF	I_{DD}	—	1	—	1	—	1	mA
Maximum Power Dissipation	P_D	—	500	—	500	—	500	mW

SWITCHING CHARACTERISTICS ($V_{DD} = 5$ V $\pm 10\%$, $T_A = 0$ to $70^\circ C$)

Characteristic	Figure No.	Symbol	Min	Max	Unit
Clock High Time	2	t_{CH}	2	—	μs
Clock Low Time	2	t_{CL}	2	—	μs
Clock Rise Time	2	t_{CR}	—	2	μs
Clock Fall Time	2	t_{CF}	—	2	μs
Enable Lead Time	2	t_E LEAD	200	—	ns
Enable Lag Time	2	t_E LAG	200	—	ns
Data Set-Up Time	2	t_D SUP	200	—	ns
Data Hold Time	2	t_D HOLD	1	—	μs
Scanner Frequency*	4	$1/t_{SCAN}$	50	300	Hz
OSC/Digit Lead Time	4	t_{OD}	—	10	μs
OSC/Segment Lead Time	4	t_{OS}	—	10	μs
Digit Overlap	4	t_{OV}	—	5	μs

* Scanner Capacitance = 0.022 μF .

CIRCUIT OPERATION

The circuit accepts a 20-bit input, 16 bits for the four-digit display plus 4 bits for the decimal point — these latter four bits are optional.

The input sequence is the decimal point code followed by the four digits, as shown in Figure 1.

In order to enter data the enable input, ENB, must be active low. The sample and shift are accomplished on the falling clock edge, see Figure 2. Data are loaded from the shift register to the latches when ENB goes high. While the shift register is being loaded, the previous data are stored in the latches.

If the decimal point is used, the system requires 20 clock pulses to load data; otherwise only 16 are required.

CASCADING

The circuit may be cascaded in the following manner.

If a 1111 word is loaded into the decimal point latch, the output of the shift register is switched to the decimal point driver, see Figure 3. Therefore, to cascade n four-digit display drivers, a set-up is used which loads the 1111 cascading word:

1. ENB = active low.
2. Load 20 bits, the first four bits being 1, with 20 clock pulses.
3. ENB = high, to load the latch.
4. Repeat steps 1 to 3 ($n - 1$) times.

5. ($n \times 20$) bits can be loaded into n circuits, with 1111 as decimal point word to continue the cascading.

SCANNER

The scanner frequency is determined by an on-chip oscillator, which requires an external frequency-determining capacitor. The capacitor voltage varies between two trigger levels at the oscillator frequency.

An external oscillator signal can be used, within the recommended operating range of 200 to 800 Hz. For test purposes this frequency may be increased up to 10 kHz.

A divide by four counter provides four non-overlapping scanner waveforms corresponding to the four digits — see Figure 4.

SEGMENT DECODER

The code used in these matrix decoders is shown in Figure 5.

OUTPUT DRIVERS

There are two different drivers:

- The segment and decimal point drivers; these are NPN emitter followers with no current limiting devices.
- The digit output buffers; these are short-circuit protected CMOS devices.

A typical application circuit is shown in Figure 6.

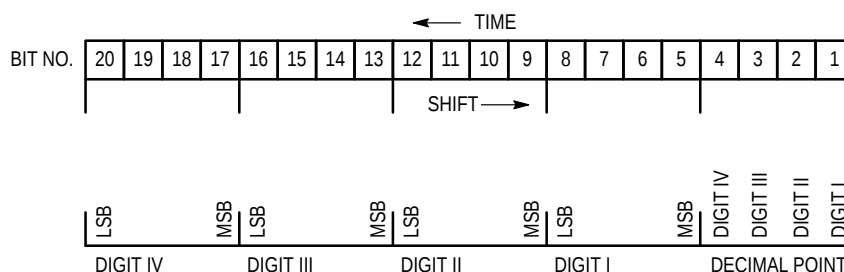


Figure 1. Input Sequence

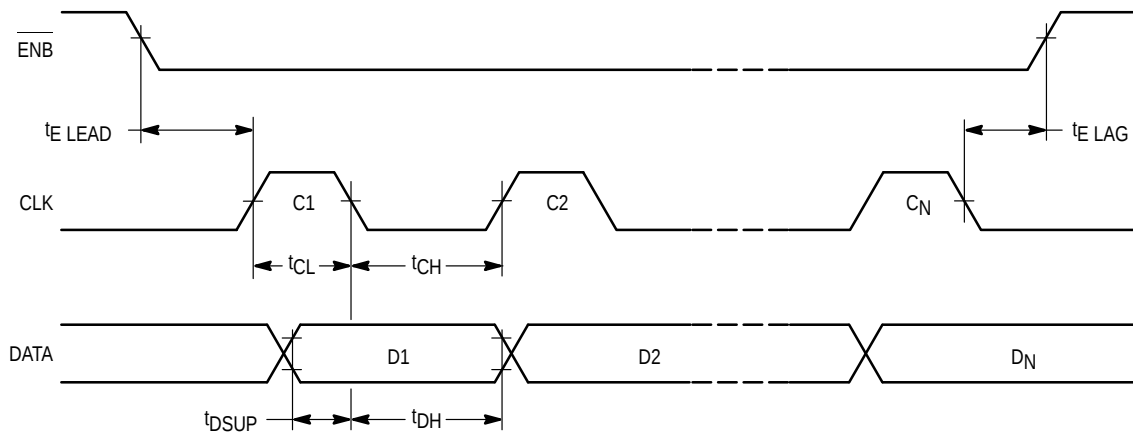


Figure 2a. Serial Input, Positive Clock

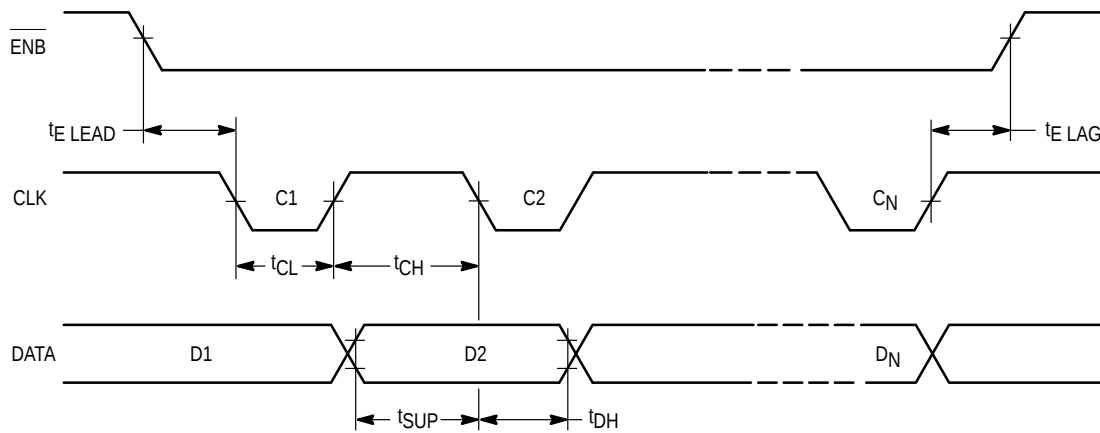


Figure 2b. Serial Input, Negative Clock

Figure 2. Serial Input

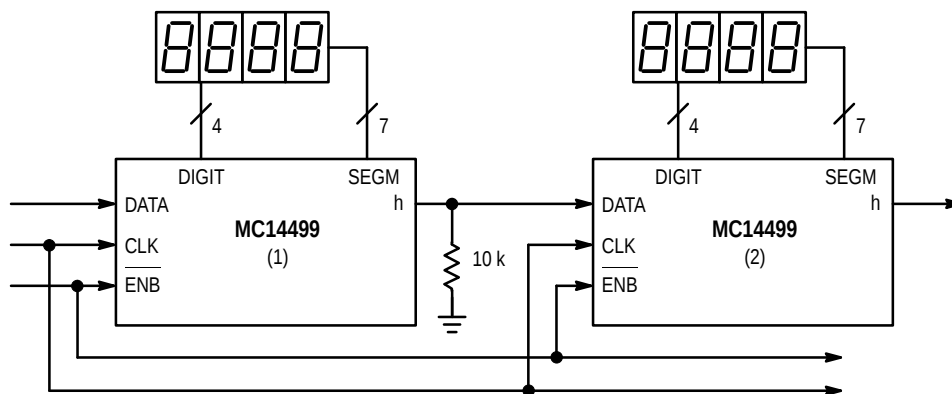


Figure 3. Cascading MC14499s

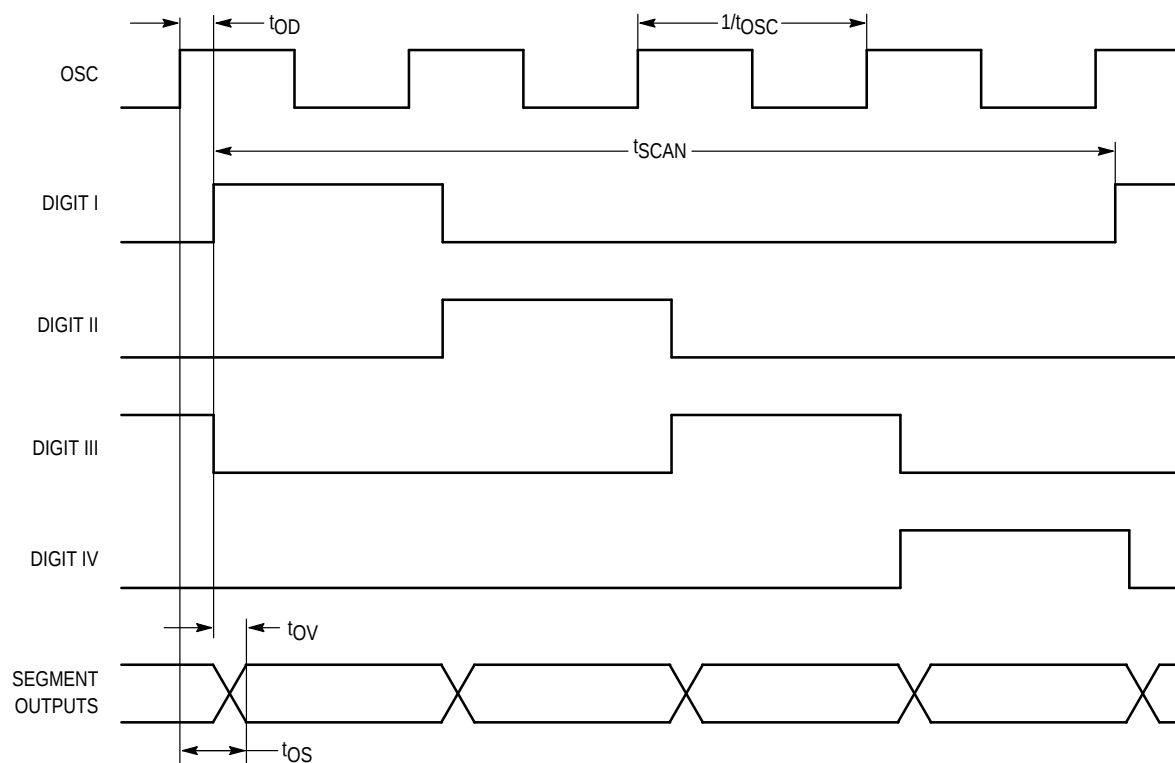


Figure 4. Scanner Waveforms

0000	0	1000	8
0001	1	1001	9
0010	2	1010	A
0011	3	1011	I
0100	4	1100	11
0101	5	1101	U
0110	6	1110	DASH -
0111	7	1111	BLANK

Figure 5. Segment Code

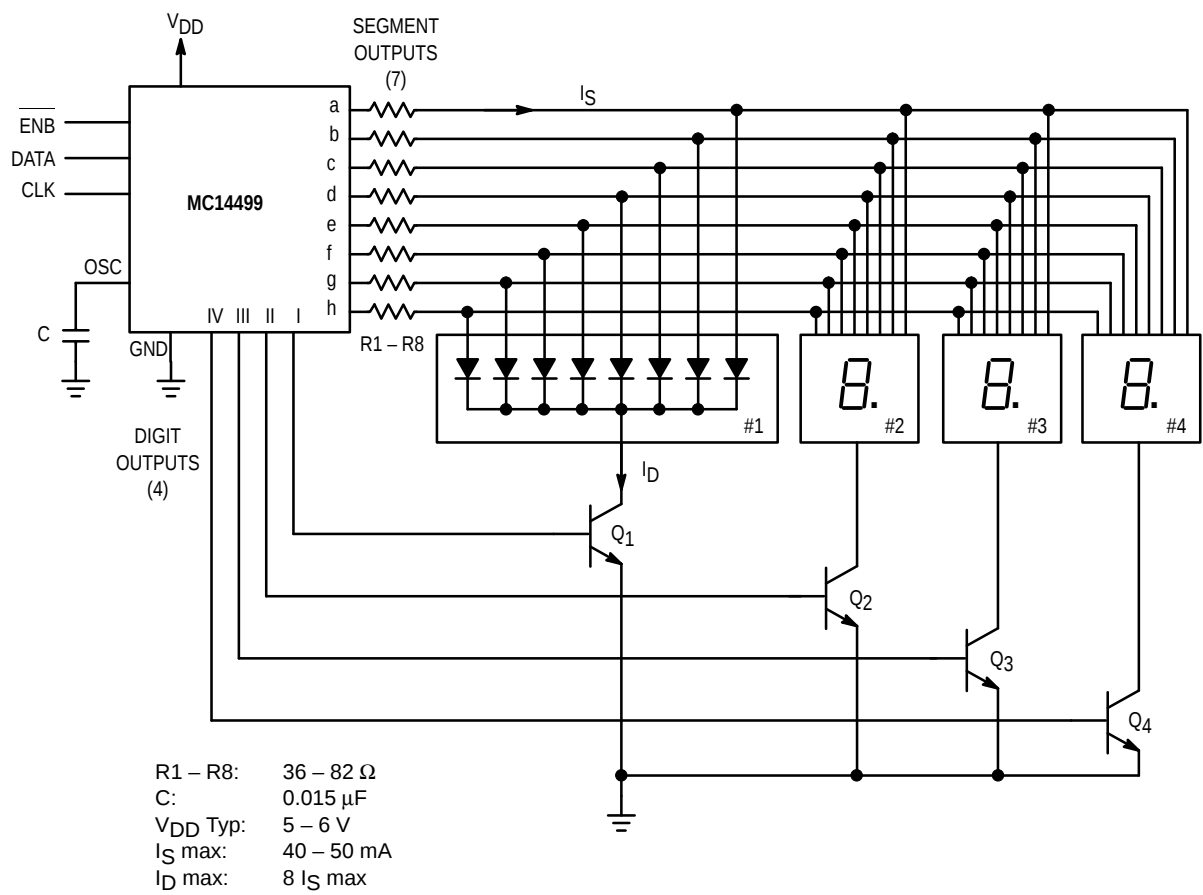
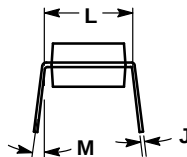
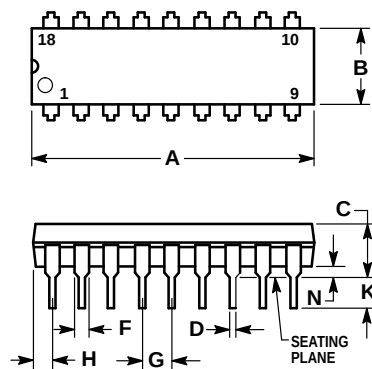


Figure 6. Application Example

PACKAGE DIMENSIONS

P SUFFIX PLASTIC DIP CASE 707-02

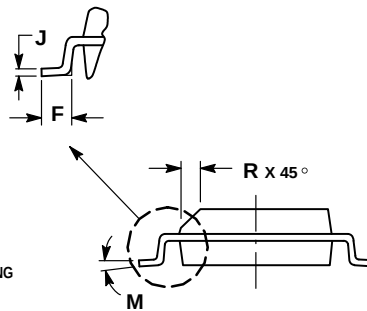
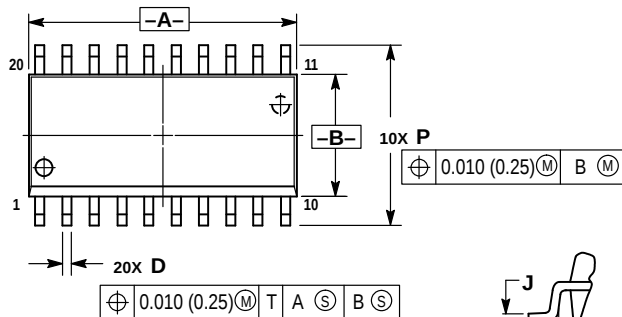


NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

DW SUFFIX SOG PACKAGE CASE 751D-04



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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