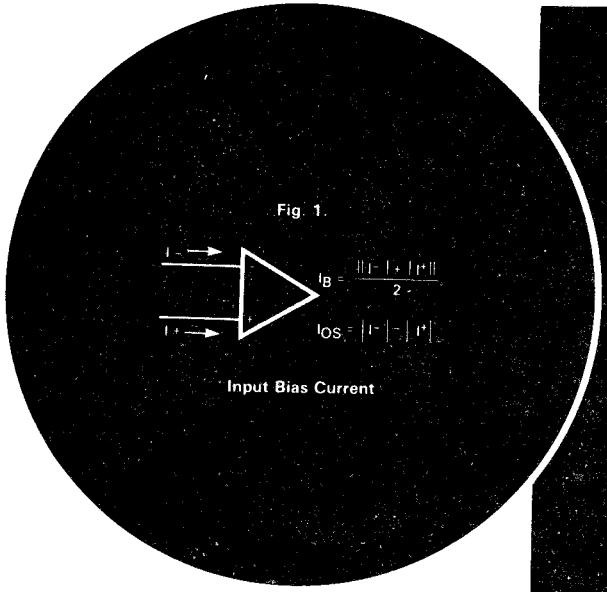

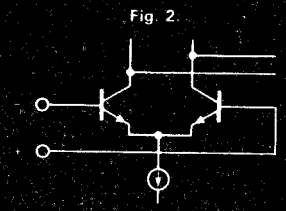

op amps

INPUT BIAS & INPUT OFFSET CURRENT

The selection of an operational amplifier for a given application requires a good understanding of op amp specification and parameters. This article is the first of a series which will discuss op amp parameters and their significance.

by Moise Hamaoui

Operational Amplifier Input Bias

Input bias current probably affects all applications of operation amplifiers. All applications are not included here, of course, but the problems caused by input bias current are usually the same, and the same derivations (hopefully) should apply.

In order for op amps to operate properly, it is necessary to supply a certain dc current (typically from pA to μA) at each input. Input bias current is the *average* of the two input currents *(Figure 1)*. Input offset current (I_{OS}) is the *difference between* the two input currents *(Figure 1)*.

What Causes Input Bias Current?

The input stage of an op amp is ordinarily some type of differential amplifier with a dc current source which sinks current from the emitters *(Figure 2)*. The inputs to the op amp which feed the bases of the differential amplifier transistors must supply the base current. This base current is the input bias current. It is primarily a function of the large signal current gain of the input stage (B). Input offset current is usually caused by mismatch of the differential amplifier, which results in different input bias currents for the two inputs.

How Does Input Bias Current Affect Applications?

The output offset voltage due to bias current for both inverting and non-inverting amplifiers is the same *(Figure 3)*. *Equation 1* shows derivation (also see *Figure 4*).

$$V_{offset} = I_{B1}R2 \quad I_{B2}R3\left(1 + \frac{R2}{R1}\right) \qquad (1)$$

For inverting and non-inverting operation, R3 is selected to minimize output offset without affecting gain.

R3 equals R2 in parallel with R1.

$$R3 = \frac{R1\,R2}{R1 + R2} \qquad (2)$$

Substituting *Equation 2* for *Equation 1*

$$V_{offset} = (I_{B1} - I_{B2})(R2) \qquad (3)$$

$$V_{offset} = I_{OS}\,R2 \qquad (4)$$

For R3 = 0

$$V_{offset} = I_B R2 \qquad (5)$$

NOTES:

(a) For the inverting configuration it is usually simple to make R3 equal to R1 in parallel with R2, which reduces the output offset voltage to only $I_{OS}R2$. If, however, the application doesn't require very low output offset voltage, or if the input bias current I_B is very low, make R3 = 0 and the output offset is simply I_BR2. Therefore, it is wise to

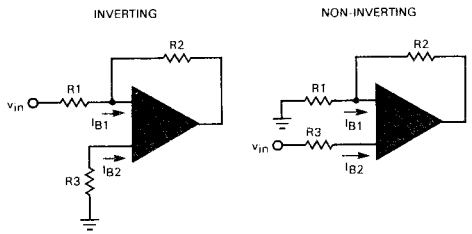

Fig. 3. Output Offset Voltage

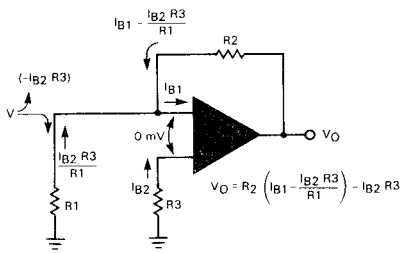

Fig. 4. Output Offset Voltage

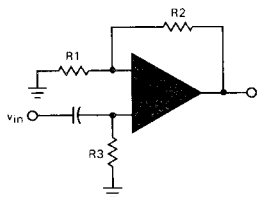

Fig. 5. AC Amplifier

first calculate the output offset voltage produced by the op amp assuming R3 = 0 (I_BR2). If this offset is low enough for the application, the use of one resistor is saved. If the offset is too high, add R3 to the circuit and then calculate offset (I_{OS} R2) to see if it meets your specification.

(b) In the non-inverting configuration, R3 is part of the signal source impedance and, in some cases, that source impedance is not well known and this complicates the minimizing of the output offset. If the source impedance is known to be very low, then a known series resistor can be added to make R3 = R1/R2. The limiting factor for increasing the value of this resistor is the op amp input impedance. If a high value of resistor is used, say 1 MΩ, and the amplifier input impedance is around 9 MΩ in the frequency range of interest, the result is a 10% drop in signal gain.

(c) Never forget the need for a dc current path to the op amp inputs. If the op amp is used in an ac amplifier as shown in *Figure 5*, notice that R3 is required to provide a dc current path to the non-inverting input. Without R3, the circuit just doesn't work! R3 is also necessary if the source can't supply the bias current.

(d) A fixed offset is not usually much of a problem and extra input circuitry may be added to cancel it. It is usually the *drift* of the offset with temperature, time, etc., which causes problems. Therefore, once an op amp with acceptable output offset voltage is found, it is necessary to investigate the offset change as a function of temperature voltage, supply, time, etc., and assure that it won't cause problems in a particular application. Most data sheets give input bias current and offset current as functions of temperature, supply voltage, and time, and also provide temperature dependance curves.

Where Does Input Bias Current Affect Applications?

Input bias current comes into effect in circuits where op amps act as buffers or amplifiers with a charged capacitor as a source. Because of input bias current, the charge across the capacitor starts draining even if the op amp input impedance is very high. Two examples are shown in *Figures 6* and *7*.

The sample and hold circuit shown in *Figure 6* consists of a voltage v_{in} which charges a holding capacitor C. When the electronic switch opens, the capacitor is expected to hold the voltage v_{in}, and the op amp simply acts as a buffer. The output of the op amp, therefore, should hold the value of v_{in} at the level it was when the switch opened for as long as the switch remains open. Because of bias current and other leakage, however, the held voltage gradually changes. This voltage changes at the following rate.

$$\frac{\Delta V}{\Delta t} = \frac{I}{C} \qquad (6)$$

where I is input bias current plus other leakages

Equation 6 determines how long a held voltage remains within specified accuracy of its original value. In this sample and hold application, the effect of input bias current shows in the holding time. For example, if the capacitor C = 1 μF, and the maximum permissible change of voltage ΔV is 10 mV, using a μA741 (I_B = 0.5 μA) and neglecting other leakages, the holding time is expressed as follows.

$$\Delta t = \frac{C\Delta V}{I} = \frac{1\times10^{-6}\times10\times10^{-3}}{0.5\times10^{-6}} = 20\ \text{ms} \qquad (7)$$

With a μA740, (I_B = 300 pA) a better holding time results.

$$\Delta t = \frac{C\Delta V}{I} = \frac{10^{-6}\times10\times10^{-3}}{300\times10^{-12}} = 33.3\ \text{s} \qquad (8)$$

Low input bias current is not the only criterion for sample and hold buffers, offset voltage drift is another important parameter.

Equation 6 also applies in circuits where the voltage held is across a capacitor in a feedback loop, *(Figure 7)*.

Another application where input bias current plays a role is in current-to-voltage conversion, *(Figure 8)*.

The causes and effects of input bias current have been briefly discussed. A few examples of applications where input bias current is important have been illustrated. Input offset voltage, also a factor, will be discussed in a future article.

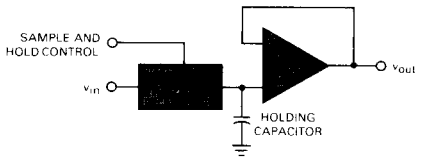

Fig. 6. Sample and Hold

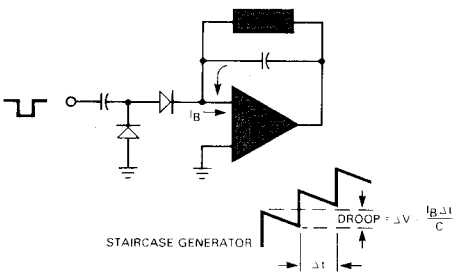

Fig. 7. Staircase Generator

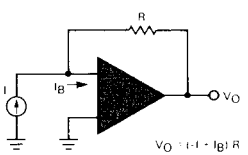

Fig. 8. Current-to-Voltage Conversion

op amps

INPUT OFFSET VOLTAGE

This is the second in a series of articles discussing op amp parameters and their significance. Last month the cause and effects of input bias and input offset current was the subject. Input offset voltage is a natural continuation of the series.

by Moise Hamaoui

What is Input Offset Voltage?

Input offset voltage is the magnitude of the voltage that, when applied between the inputs of the op amp, gives zero output voltage. This means that, even without applying a signal across the inputs of the op amp, a dc voltage difference exists between the inputs which is amplified and causes the output to be at a non-zero value. When a voltage is applied across the inputs of the op amp such that it gives zero output voltage, the initial input offset is cancelled. Therefore, the applied voltage is of the same magnitude as the initial input offset but of opposite polarity.

What Causes Input Offset Voltage?

Well, essentially every mismatch between the signal flow of the inverting input and the non-inverting input contributes to input offset voltage, V_{OS}. The major contributor, however, is the V_{BE} mismatch of the differential input stage. V_{OS} is generally in the 1 to 10 mV range for non-FET input op amps.

How Does Offset Voltage Affect Applications?

For inverting and non-inverting amplifier applications *(Figures 1 and 2)*, the output voltage has a dc output level due to V_{OS}. Output voltage offset is given by

$$V_O = V_{OS}\left(1 + \frac{R2}{R1}\right) \qquad (1)$$

and derived from the following (See Figure 3).

Input bias current = 0

$$I_1 = \frac{V_{OS}}{R1} \qquad I_2 = I_1 \; (I_{Bias} = 0)$$

$$V_O = I_2\,R2 + I_1\,R1$$

$$V_O = I_1\,(R2 + R1)$$

$$V_O = \frac{V_{OS}}{R1}\,(R2 + R1)$$

Remember that the output offset voltage given in *Equation 1* is caused only by the input offset voltage, V_{OS}. The last article explained the output offset voltage caused by the input bias and offset current. The total output offset voltage is thus given by the sum of the two offsets.

Total dc output offset, (2)

$$V_O = \left(1 + \frac{R2}{R1}\right) V_{OS} + I_{B1}\,R2 - I_{B2}\,R3\left(1 + \frac{R2}{R1}\right)$$

For $R3 = \dfrac{R1\,R2}{R1 + R2}$

$$V_O = V_{OS}\left(1 + \frac{R2}{R1}\right) + I_{OS}\,R2$$

where I_{OS} is the input offset current.

For R3 = 0

$$V_O = V_{OS}\left(1 + \frac{R2}{R1}\right) + I_{Bias}\,R2$$

Here are some examples that will give an idea of the range of values discussed.

For a gain of 10 in an inverting configuration,
R2 = 100 kΩ R1 = 10 kΩ R3 = 9 kΩ

Using μA741C,
$V_{OS(max)}$ = 6 mV
$I_{OS(max)}$ = 200 nA
Output Offset = 86 mV max

Using μA777,
$V_{OS(max)}$ = 2 mV
$I_{OS(max)}$ = 3 nA
Output Offset = 22 mV max

Using μA740C,
$V_{OS(max)}$ = 110 mV
$I_{OS(max)}$ = 0.3 nA
Output Offset = 1.2 V max

Keep in mind, however, that the input offset voltage and current vary with temperature and this is usually the most objectionable factor of those offsets. Most op amp data sheets give input offset voltage values and temperature dependance curves.

Offset Voltage Nulling

In some op amps, offset voltage may be nulled with only an external potentiometer to two device leads *(Figure 4)*. Usually what is happening internally is that one side of the input stage differential amplifier gets more or less current than the other side and thus causes a V_{BE} difference to null the initial V_{BE} mismatch.

Where Else Does Input Offset Voltage Affect Applications?

If V_{OS} is considered as a small dc voltage source connected to an ideal op amp *(Figure 5)*, its effect can be analyzed in almost every application. From *Figure 5*, it is apparent that in comparator applications, the output does not vary state until the inverting input is at least a V_{OS} different than the non-inverting input. That is, if a zero crossing detector is being designed and the non-inverting input is connected to ground, the output would change states at a V_{OS} voltage different than ground.

Hopefully, this discussion will help the designer choose the best op amp for a given application. Future articles will discuss such important parameters as open loop voltage gain, slew rate, input resistance, etc.

INVERTING

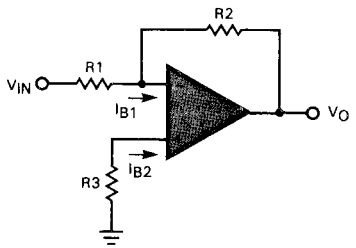

Figure 1

NON-INVERTING

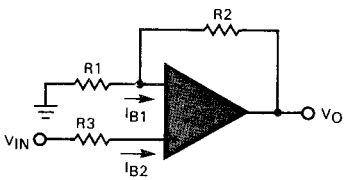

Figure 2

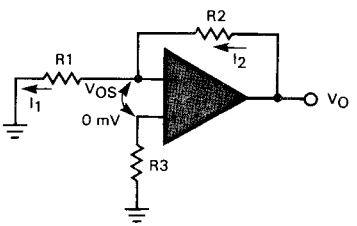

Figure 3

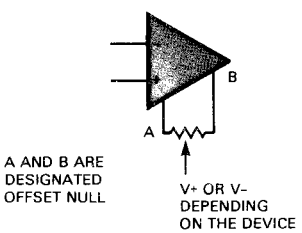

Figure 4

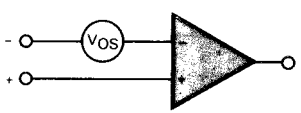

Figure 5

op amps

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

Our discussion series of op amp parameters and their significance in particular applications continues with a look at open loop voltage gain as a function of frequency.

by Moise Hamaoui

What is Open Loop Voltage Gain?

Open loop voltage gain, A_{VOL}, is defined as the ratio of the change in output voltage to the change in input voltage causing it *(Figure 1)*.

How Does Open Loop Voltage Gain Affect Applications?

In a typical application *(Figure 2)*,

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R2}{R1}$$

This is true *only* if the op amp has infinite or very high open loop gain. However, in practical op amps, the A_{VOL} decreases with frequency until it becomes even less than one. The question is, then, to what frequency does *Equation 1* hold true for a particular op amp? Simple derivations show that if

$$V_{OUT} = -\frac{R2}{R1} V_{IN}$$

is assumed, an error arises due to neglecting A_{VOL} given by the following equation.

$$\text{Closed loop gain error} = \frac{100}{1 + \frac{A_{VOL}\, R1}{R1 + R2}} \% \qquad (1)$$

For instance, if the op amp is a μA741 with R2/R1 = 100, $A_{VOL} = 10^4$ at 100 Hz, as determined from the curve of *Figure 3*. From *Equation 1*, there is an error in assuming $V_{OUT}/V_{IN} = 100$ at 100 Hz given by

$$\frac{100}{1 + \frac{10^4 \times 1}{101}} = 1\% \qquad (2)$$

The A_{VOL} of the μA741 is equal to 100 at 10 kHz and the 1% error in *Equation 2* becomes substantial.

$$\frac{100}{1 + \frac{100}{101}} = 50\%$$

Note that when the open loop voltage gain is equal to the feedback ratio, (R2 + R1)/R1, the amplifier gain drops by 6 dB.

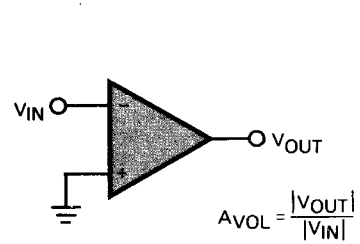

Figure 1

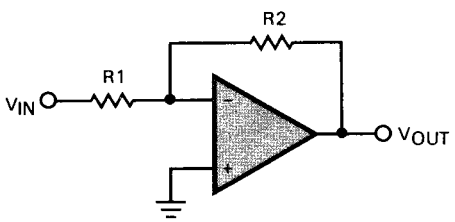

Figure 2

It's Easy to Choose the Right Op Amp.

Use the following simple rule. For a dc closed loop gain y and a decrease in gain of no more than x percent at a given maximum signal frequency f_{max}, an op amp is needed with an A_{VOL} at f_{max} given by

$$A_{VOL} \geq \frac{100\,(1 + y)}{x} - y + 1$$

For example, to achieve a dc closed loop gain of 100 with a decrease in gain of only 10% at 10 kHz, an operational amplifier is required with an A_{VOL} at 10 kHz of at least

$$\frac{100\,(1 + 100)}{10} - 100 + 1 = 911$$

One possibility is the μA725 which has an A_{VOL} of 1000 at 10 kHz with the proper compensation.

The graph in *Figure 4* is also helpful when choosing the right op amp. The horizontal axis is the feedback ratio (R2 + R1)/R1 in dB. The vertical axis is the minimum A_{VOL} required to be within 1, 3, 6 or 10 dB of the dc closed loop gain, V_{OUT}/V_{IN}.

For example, if R2 = 9 kΩ and R1 = 1 kΩ, the feedback ratio is 20 dB. At the frequency where the A_{VOL} of the op amp will be 28 dB, the closed loop gain will be 3 dB down from its dc value R2/R1. Therefore, to insure that amplifier gain does not fall off by more than 3 dB at f_{max}, choose an op amp with A_{VOL} > 28 dB at f_{max}.

Open loop voltage gain is not the only parameter that affects high frequency operation. Slew rate must be considered. Next month's article will cover this important subject.

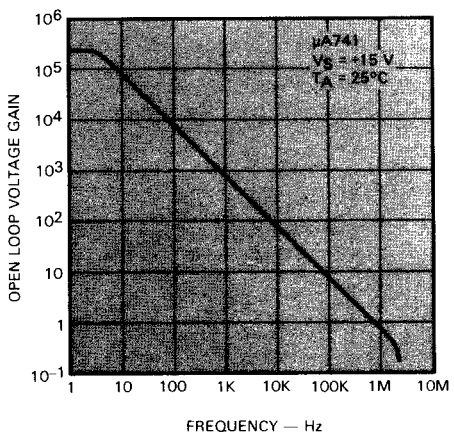

Figure 3

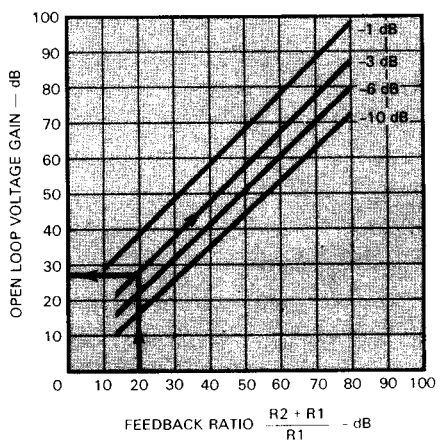

Figure 4

op amps

Fourth in the series of helpful suggestions on how to select the right op amp for your particular application

SLEW RATE-WHAT IS IT?

by Moise Hamaoui

Slew rate is the maximum rate of change of output voltage with respect to time, usually specified in volts per microsecond. For example, a 0.5 V/μs slew rate means that the output rises or falls no faster than 0.5 V every microsecond. Slew rate is also sometimes specified indirectly in data sheets as *output voltage swing as a function of frequency* or as *voltage follower large signal pulse response.*

What Causes Slew Rate?

Slew rate is caused by current limiting and saturation of an op amp internal stage. That limited current is the maximum current available to charge the compensation capacitance network. The voltage across the capacitor rises at a rate,

$$\frac{dV}{dt} = \frac{I}{C}$$

This capacitor charging rate is reflected at the output and causes slew rate limiting. Slew rate limiting therefore occurs with large input signals which saturate the internal stages. Remember that for small signals, *i.e.,* when the op amp is operated in its linear region, the step

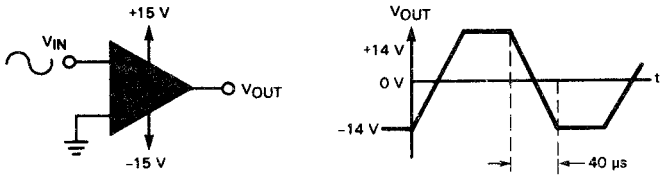

Figure 1

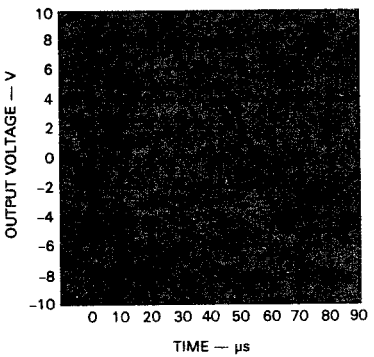

Figure 2

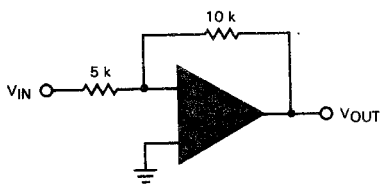

Figure 3

response of the op amp is an exponential of time constant

$$\tau = \frac{1}{2\pi f_{CL}}$$

where f_{CL} is the closed loop bandwidth of the circuit.

How Does Slew Rate Affect Applications?

In a simple application using a µA741 as a comparator *(Figure 1)*, the output will go to about −14 V and then to +14 V each time the input signal crosses zero volts. The µA741 has a typical slew rate of 0.7 V/µs, determined under electrical specifications or calculated from the slope of the output curve in *Figure 2*. Therefore, the µA741 output will go to +14 V from −14 V in

$$\frac{28\ V}{0.7\ V/\mu s} = 40\ \mu s$$

If the full 28 V output swing is desired, the input signal must have at least 40 µs between zero crossings. That is, the maximum input signal frequency should be 1/(2 x 40 µs) or 12.5 kHz assuming 50% duty cycle. Even at that frequency, the output is triangular instead of square wave. For higher frequencies or a more square wave output, an op amp with a faster slew rate is needed.

As another example of the effect of slew rate, consider the simple amplifier with a gain of two in *Figure 3*. Again, the µA741 is used. Its open loop voltage gain as a function of frequency curve *(Figure 4)* indicates that the amplifier circuit will operate with a gain of two up to about 80 kHz.

Now, what is the maximum input signal voltage that may be used up to 80 kHz? If the output is to be an undistorted sine wave, A sin ωt, then the rate of change of the output is

$$\frac{d}{dt} A \sin \omega t = A\omega \cos \omega t$$

and the maximum rate of change of the output is $A\omega$. The minimum slew rate of the operational amplifier, therefore, must be equal to $A\omega$. Thus, with $\omega = 2\pi\ (80 \times 10^3) = 503000$ and the slew rate of the µA741 typically 0.7 V/µs,

the maximum output swing A of the sine wave without distortion is

$$\frac{\text{slew rate}}{\omega} \text{ or } \frac{0.7\ V/\mu s}{503000} = 1.4\ V_{pk}$$

or $2.8\ V_{pk\text{-}pk}$

The maximum input signal should, therefore, be less than $2.8/2\ V_{pk\text{-}pk}$. The maximum output swing can also be easily read from the output voltage swing as a function of frequency curve on the data sheet *(Figure 5)*. From this curve, the maximum output swing without distortion can be determined for different frequencies.

To Sum Up

In applications where square wave outputs (comparators, oscillators, limiters, etc.) are expected, it is important to remember that the op amp output takes some time to change from one value to another. That time, which usually limits the maximum frequency of operation, is determined by the *change of output voltage divided by the slew rate.*

In applications where the output should be free of distortion, the slew rate determines the maximum frequency of operation for a desired output swing. The required slew rate can be determined by a simple formula. For a desired undistorted output voltage swing V_{pk} at a maximum frequency f_{max}, an op amp is needed with a slew rate given by

$$\text{slew rate} > 2\ \pi\ f_{max}\ V_{pk}$$

Figure 6 gives the slew rate required for different output swings at different frequencies. Another easy way to choose the right op amp is to check the data sheet curves of output voltage swing as a function of frequency *(Figure 5)*.

Remember, however, that these curves are typical and slew rate varies as a function of supply. Slew rates at different supply voltages are usually shown on the data sheet.

In some applications such as D/A or A/D, slew rate is not the only criterion for fast response. The settling time is another parameter to consider. High slew rate op amps sometimes have associated overshoot and ringing which may cause the output to reach a steady state after a longer period of time than maybe a slower slew rate op amp.

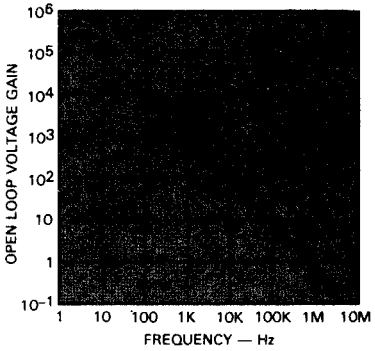

Figure 4

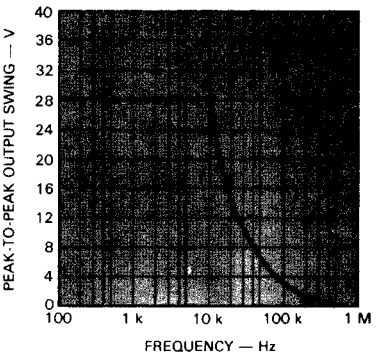

Figure 5

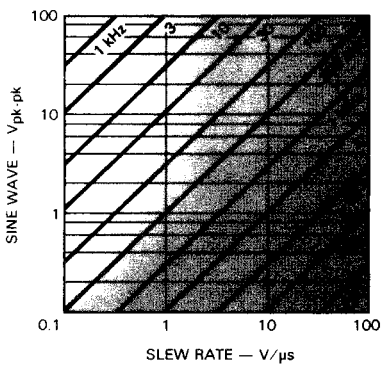

Figure 6

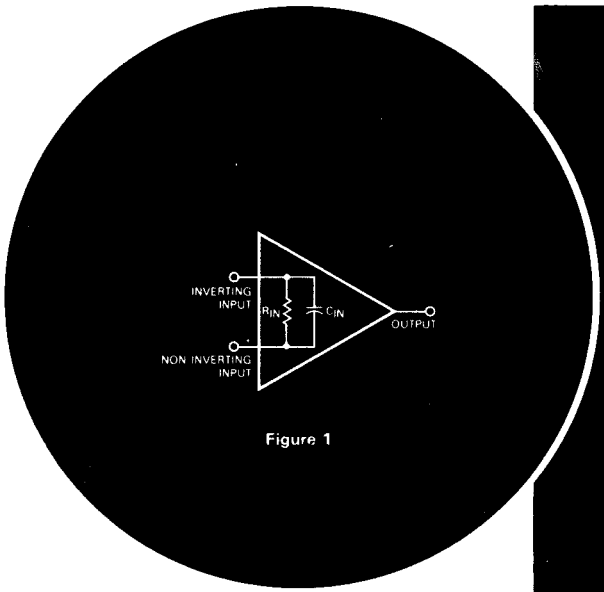

Figure 1

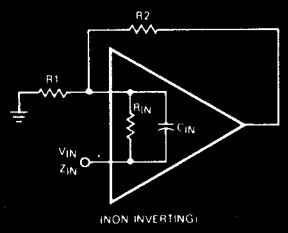

Figure 2

amps

Number five in our series — the importance of input impedance when designing with op amps.

INPUT IMPEDANCE

by Moise Hamaoui

Input Resistance and Input Capacitance—Major Factors of Op Amp Input Impedance

Input resistance, or differential input resistance usually specified in the data sheets, is the small signal resistance measured between the inverting and non-inverting inputs of the op amp. Input capacitance is the capacitance seen between the same two inputs. See *Figure 1*.

How Does Input Impedance Affect Applications?

The input impedance of an amplifier circuit with feedback is not only dependent on the op amp, but also on the circuit configuration. First order approximation for the input impedance of the non-inverting and inverting configurations is discussed.

Non-inverting Configuration (Figure 2)

Input impedance of an amplifier in the non-inverting configuration is expressed as follows.

$$Z_{IN} = Z + \frac{A_{VOL}\, Z}{1 + \frac{R2}{R1}} \qquad (1)$$

$$Z_{IN} = Z\left(1 + \frac{A_{VOL}}{1 + \frac{R2}{R1}}\right)$$

where A_{VOL} (ω) is the open loop gain of the op amp and Z is the op amp input impedance.

As indicated in *Equation 1*, the amplifier input impedance is equal to at least the op amp impedance and can go much higher at low frequencies due to high open loop gain. For example, if the μA741 is used with R2 = 9 kΩ and R1 = 1 kΩ, the open loop gain at dc is 10^5 and the input impedance of the op amp is 2 MΩ at low frequencies *(Figures 3 and 4)*. Therefore the low frequency input impedance of the amplifier, according to *Equation 1* is

$$Z_{IN} = 2\ M\Omega + \frac{10^5 \times 2\ M\Omega}{10} = 20002\ M\Omega$$

At 100 kHz, the op amp open loop gain is 10 *(Figure 3)* and R_{IN} = 1.8 MΩ *(Figure 4)*. Since the input capacitance is 2 pF, op amp input impedance is

$$Z = 1.8\ M\Omega // \frac{1}{2\pi\,(100\ kHz)\, 2 \times 10^{-12}} = 0.55\ M\Omega$$

From *Equation 1*,

$$Z_{IN} = 0.55 + \frac{10\,(0.55)}{1 + 9} = 1.10\ M\Omega$$

Obviously, it is important to consider the input impedance both at the minimum and maximum frequencies of

operation. It is safe to assume that in the non-inverting configuration, the input impedance is *at least* equal to the *input impedance* of the op amp.

For op amps to operate properly, it is necessary to supply a certain dc current at their inputs. That current is given in the data sheets as input bias current and ranges in value from picoamps to microamps depending on the op amp. In the non-inverting configuration of *Figure 2*, if V_{IN} has a series resistance of 1 MΩ and the input bias current of the op amp is 0.5 µA, there is a dc drop across the 1 MΩ series resistance of 0.5 µA x 1 MΩ = 0.5 V. This is independent of the signal (V_{IN}) amplitude. If V_{IN} is 1 V, there is 1 – 0.5 = 0.5 V at the non-inverting input. However, it is erroneous to assume that the op amp input impedance is 1 MΩ just because there is a straight voltage division. The drop is caused by input bias current and not by input impedance. If an ac signal is riding on the 1 V dc value of V_{IN}, the ac amplitude is not halved and only a 0.5 V offset is constantly there due to bias current. The signal amplitude is affected by the 1MΩ series resistance and the op amp input impedance.

Inverting Configuration (Figure 5)

Input impedance of an amplifier in the inverting configuration is

$$Z_{IN} = R1 + \frac{R2\ (Z + R)}{A_{VOL} Z} \qquad (2)$$

$$Z_{IN} \approx R1$$

In this configuration, the effect of the op amp input impedance is minimal. The input impedance is at least R1; at high frequencies, as A_{VOL} decreases, the input impedance increases and the value of $[R2\ (Z + R)]/A_{VOL}\ Z$ becomes comparable to that of R1.

For all practical applications, however, it is safe to assume that the input impedance is just R1. Again, remember that a constant dc bias current is required at the inverting input to operate the op amp. The dc bias current limits the increase in value of R1. The higher the value of R1, the greater the magnitude of the dc offset voltage occurring at the output.

Another interesting point concerning *Equation 2* is that the effect of increased input impedance at higher frequencies (A_{VOL} decreases in the denominator) is very similar to an inductance effect, usually referred to as Miller inductance. See Fairchild Application Note 321, "Operational Amplifiers as Inductors," for more detail.

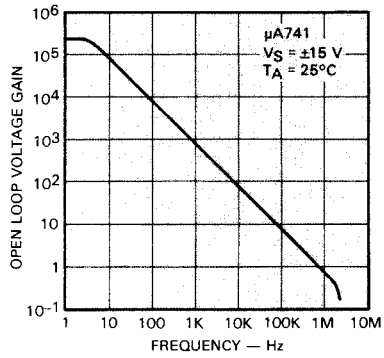

Figure 3

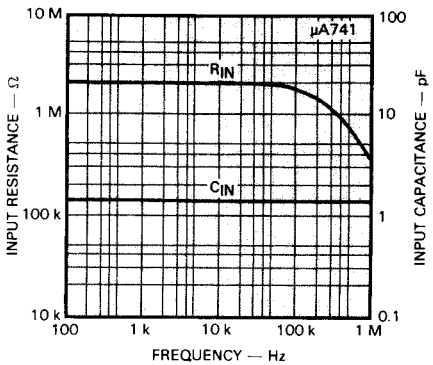

Figure 4

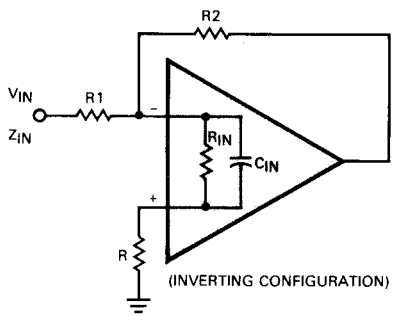

Figure 5

op amps

This article, the sixth in our Op Amp series, discusses circuit stability criteria and implementation along with a look at some basic applications.

CIRCUIT STABILITY

by Moise Hamaoui

How Can Circuit Stability Be Assured?

Circuit stability can easily be determined by following one simple rule and referring to the phase response and open loop voltage gain curves on the op amp data sheets.

Open loop voltage gain, $A_{VOL}(\omega)$, of the op amp is one consideration when determining circuit stability. It is defined as the ratio of the change in output voltage to the change in input voltage*. Open loop voltage gain versus frequency, readily available from the data sheets, may be written as:

$$A_{VOL}(\omega) = \frac{120 \times 10^3}{\left(1 + j\frac{f}{5}\right)\left(1 + j\frac{f}{3\ MHz}\right)}$$

(From *Figure 1*)

Next, it is necessary to consider the transfer functions for the inverting and non-inverting configurations shown in *Figures 2* and *3*. They can be expressed by the following equations.

Inverting:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{Z2}{Z2 + Z1}\right)\left(\frac{-A_{VOL}(\omega)}{1 + \frac{A_{VOL}(\omega)}{1 + \frac{Z2}{Z1}}}\right)$$

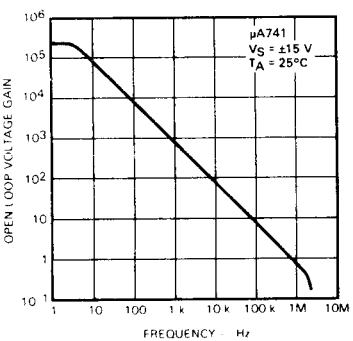

Fig. 1

*See PROGRESS, Vol. 2, No. 5, May 1974, pg. 8.

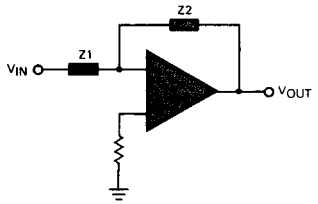

Fig. 2

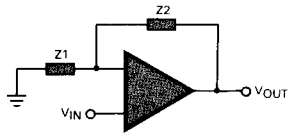

Fig. 3

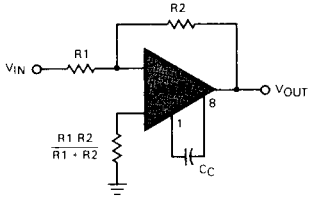

Fig. 4

Non-Inverting:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{A_{VOL}(\omega)}{1+\frac{A_{VOL}(\omega)}{\frac{Z2}{Z1}}}}{1+\frac{Z2}{Z1}}$$

From these transfer functions, as well as from feedback theory, the stability of the inverting and non-inverting configurations can be determined by following this simple rule. The circuits will be stable if the magnitude of the term

$$\frac{A_{VOL}(\omega)}{1+\frac{Z2}{Z1}}$$

is less than unity when its phase angle reaches 180°. Stated another way, the phase angle of the above term must be less than 180° when its magnitude reaches unity. The simplicity of this rule is illustrated in the following example.

Amplifier and Voltage Follower Stability

In amplifiers where Z2 and Z1 are resistive, the circuit stability depends mainly on $A_{VOL}(\omega)$ because there is no phase shift in 1 + Z2/Z1. For example, in the circuit of *Figure 4,*

for R2 = R1,

$$1+\frac{Z2}{Z1} = 2 \angle 0^\circ$$

Now, when $A_{VOL}(\omega) = 2$, the term

$$\frac{A_{VOL}(\omega)}{1+\frac{Z2}{Z1}} = 1$$

From the open loop voltage gain curve *(Figure 5),* it is apparent that $A_{VOL}(\omega) = 2$ at about 500 kHz with C_C = 30 pF or at about 5 MHz with C_C = 3 pF. In *Figure 6,* note that the phase shift of the $A_{VOL}(\omega)$ is close to 180° at 5 MHz; therefore the circuit is potentially unstable or oscillatory. The phase is close to 110° at 500 kHz. Therefore the compensation, C_C = 30 pF, should be used instead of C_C = 3 pF since with C_C = 3 pF

$$\frac{A_{VOL}(\omega)\ (5\ MHz)}{1+1} = 1 \angle 180^\circ \text{ (unstable)}$$

and with C_C = 30 pF

$$\frac{A_{VOL}(\omega)\ (500\ kHz)}{1+1} = 1 \angle 110^\circ \text{ (stable)}$$

Summary

To determine stability for a resistive feedback circuit, the frequency at which $A_{VOL}(\omega)$ is equal to 1 + R2/R1 is found on the open loop voltage gain curve. At that frequency, the ratio

$$\frac{A_{VOL}(\omega)}{1+\frac{Z2}{Z1}} = 1$$

The phase shift at that frequency is then read on the op amp phase response curve. If the phase shift is less than 180°, the configuration is stable; if it is more than 180°, the configuration is unstable. Often the results of these computations are given in the data sheet as frequency response for various closed loop gains using recommended compensation networks *(Figure 7).*

When Z2/Z1 is non-resistive as in integrators and differentiators, the same rule holds but the phase response of both $A_{VOL}(\omega)$ and 1 + Z2/Z1 must be considered. For more information on stability rules for integrators and differentiators, see Fairchild Application Note 289, "Applications of the μA741 Operational Amplifier".

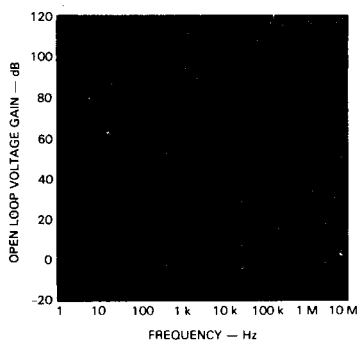

Fig. 5

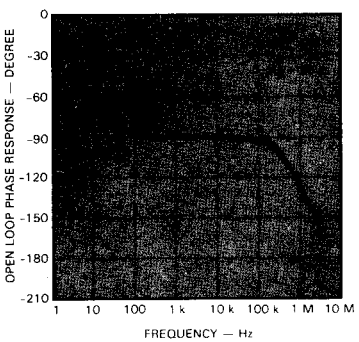

Fig. 6

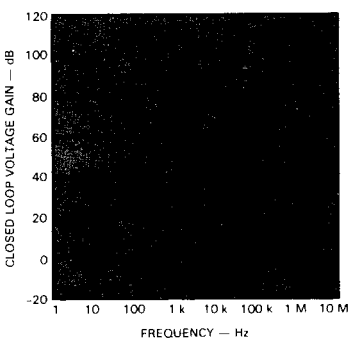

Fig. 7

op amps

The last two articles in this series will explain how to check op amp parameters to find the most efficient and cost-saving device to meet operational amplifier specifications.

DESIGN STEPS FOR INVERTING AMPLIFIERS

by Moise Hamaoui

This series to date has discussed the most important op amp parameters and offered guidelines for choosing the right op amp for a particular application. Now, how do these guidelines translate into practical amplifier design? The final two articles will present some simple steps leading to four basic requirements for designing op amp amplifier circuits—inverting this month, non-inverting next month. Reference is made to the previous issue(s) of Progress that contains the discussion of the parameter considered in each step.

Inverting Amplifier Specifications

First, of course, is to establish circuit specifications that are necessary for the application. For this discussion, the following specs were assumed.

Gain = A = -9

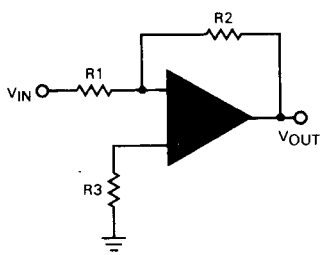

Figure 1

Minimum 3 dB down frequency, f_c = 10 kHz

Maximum input signal amplitude,
$V_1 = 2\ V_{pk\text{-}pk}$

Maximum dc output offset voltage,
$V_{O(max)} = \pm 25$ mV

Input resistance, $R_{IN} = 10\ k\Omega$

DC drift from 0 to 70°, $\Delta V_{O(max)} \leq 15$ mV

Step 1—Circuit Configuration

Using the circuit of *Figure 1,*

$$\frac{V_{OUT}}{V_{IN}} = \frac{-R2}{R1} = A = -9;\ \frac{R2}{R1} = 9 \qquad (1)$$

Step 2—Frequency Response (Progress, May 1974)

The first op amp specification to check is the minimum open loop voltage gain, A_{VOL}, needed to meet the amplifier frequency response requirement. This is easy to do by using the graph in *Figure 2.* Since R2/R1 = 9 then (R2 + R1)/R1 = 10, locate the 10 ratio (20 dB) on the (R2 + R1)/R1 axis. Go up to the 3 dB line and read, on the vertical axis, the minimum A_{VOL} required, 28 dB. Therefore, to insure that amplifier gain

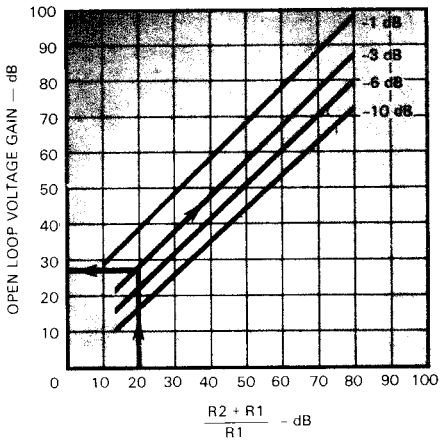

Figure 2

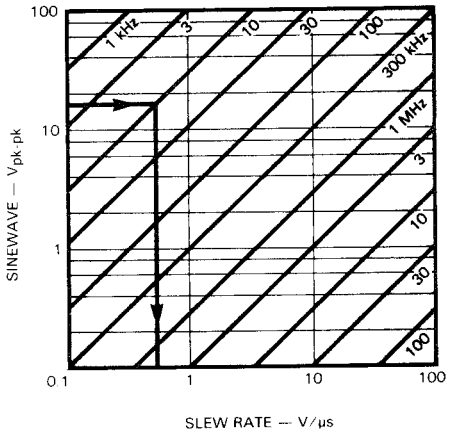

Figure 3

does not fall off by more than 3 dB at f_C, the op amp must have an open loop gain of

First Requirement

$$A_{VOL} \geq 28 \text{ dB at } f_C \text{ (10 kHz)}$$

Step 3—Output Swing (Progress, June 1974)

Since the maximum input signal amplitude is 2 $V_{pk\text{-}pk}$, the maximum output swing will be 18 $V_{pk\text{-}pk}$. Therefore, an op amp is needed with a slew rate fast enough to give 18 $V_{pk\text{-}pk}$ up to 10 kHz. By checking *Figure 3*, it is apparent that an op amp is required with

Second Requirement

$$\text{slew rate} \geq 0.8 \text{ V/}\mu\text{s}$$

Step 4—Maximum DC Output Offset Voltage V_O (Progress, March and April 1974)

The dc output offset voltage, V_O, for the circuit in *Figure 1* is given by the following equations.

For R3 = 0

$$V_O = \left(1 + \frac{R2}{R1}\right) V_{OS} + I_{Bias}\, R2 \qquad (2)$$

For R3 = R1 in parallel with R2

$$= \frac{R1\, R2}{R1 + R2}$$

$$V_O = \left(1 + \frac{R2}{R1}\right) V_{OS} + R2\, I_{OS} \qquad (3)$$

where V_{OS} = input offset voltage

I_{Bias} = input bias current

I_{OS} = input offset current

Unless the output offset voltage spec is very wide, it is usually more economical to add R3 than use a very low input bias current op amp. For the example in this discussion, R3 = R1 in parallel with R2. From *Equation 3*, it can be seen that the V_O value will be low when R2 is small; therefore the smallest possible value should be chosen for R2.

For the inverting configuration, the input resistance R_{IN} is at least R1 (Progress, July 1974). Therefore, choose R1 so that

$$R1 \geq R_{IN} \geq 10\ k\Omega \qquad (4)$$

From *Equations 1* and *4*, R2/R1 = 9 and R1 $\geq$ 10 kΩ ; therefore when R1 is 10 kΩ , R2 = 90 kΩ and R3 = 9 kΩ. *Equation 3* becomes

$$V_O = (1 + 9)\, V_{OS} + (90 \times 10^3)\, I_{OS}$$

Thus, an op amp is needed such that V_{OS} and I_{OS} give

Third Requirement

$$10\, V_{OS} + (90 \times 10^3)\, I_{OS} \leq 25 \text{ mV} \leq V_{O(max)}$$

To simplify the search for an op amp to meet this requirement, look first for one that has the following specs.

$$V_{OS} < \frac{V_{O(max)}}{10} \text{ or } < \frac{25}{10} \text{ mV}$$

$$I_{OS} < \frac{V_{O(max)}}{90 \times 10^3} \text{ or } < 270 \text{ nA}$$

Step 5—Drift

Drift is given by

Fourth Requirement

$$\Delta V_O = 10 \Delta V_{OS} + (90 \times 10^3) \Delta\, I_{OS} \leq V_{O(max)} \text{ (15 mV)}$$

where ΔV_{OS} and $\Delta\, I_{OS}$ are the changes in input offset voltage and input offset current over the 0 to 70° temperature range.

Step 6—Final Hints in Choosing the Right Op Amp

It is usually best to start by finding the op amps that meet the first and second requirements; this will eliminate many. Then check the good ones with the third and fourth requirements starting with the lowest cost op amp. There are usually other specifications such as supply voltage and current, supply rejection, load current, etc., that should be considered. However, the op amps that meet the four requirements will narrow down the field of choice to only a few; they can then be checked further to see if they meet the rest of the specifications.

op amps

DESIGN STEPS FOR NON-INVERTING AMPLIFIERS

This completes our series on the most important op amp parameters, their significance in applications, and how to put them to use when selecting the best op amp for a particular amplifier design.

by Moise Hamaoui

The design steps for non-inverting amplifiers are similar to those for inverting amplifiers. As in the discussion last month on inverting amplifier design, reference is made to the previous issue(s) of Progress that contains the explanation of the parameter considered in each step.

Non-Inverting Amplifier Specifications

For this discussion, the following specifications were assumed.

Gain = A = 10
Minimum 3 dB down frequency, f_c = 10 kHz
Maximum input signal amplitude, $V_1 = 2\,V_{pk\text{-}pk}$

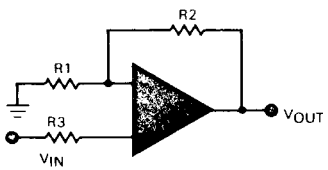

Figure 1

Input resistance, R_{IN} = 5 MΩ min
Maximum dc output offset voltage,

$$V_{O(max)} = \pm 25\ mV$$

DC drift from 0 to 70°,

$$\Delta V_{O(max)} \leq 15\ mV$$

Step 1 — Circuit Configuration

In the circuit of *Figure 1,*

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + R1}{R1} = A = 10 \qquad (1)$$

Step 2 — Frequency Response (Progress, May 1974)

As with inverting amplifier design, the first op amp specification to check is the minimum open loop voltage gain,

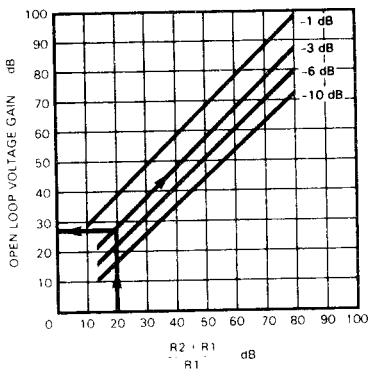

Figure 2

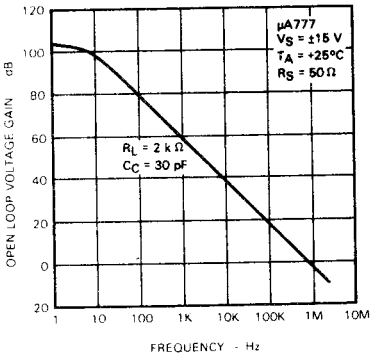

Figure 3

A_{VOL}, needed to meet the amplifier frequency response requirement. This is easy to do by using the graph in *Figure 2*. Since (R2 + R1)/R1 = 10, locate the 10 ratio (20 dB) on the (R2 + R1)/R1 axis. Go up to the 3 dB line and read, on the vertical axis, the minimum A_{VOL} required, 28 dB. Therefore, to insure that amplifier gain does not fall off by more than 3 dB at f_c, the op amp must have an open loop gain of

First Requirement

$$A_{VOL} \geq 28 \text{ dB at } f_c \text{ (10 kHz)}$$

Examination of the open loop voltage gain versus frequency curves on various op amp data sheets will quickly determine which devices will meet this requirement. *Figure 3* is a good example. An op amp with a gain bandwidth product of 25,000 (28 dB x 10 kHz) will do the job, assuming the op amp has just one pole.

Step 3 — Output Swing
(Progress, June 1974)
Since the maximum input signal amplitude is 2 $V_{pk\text{-}pk}$, the maximum output swing will be 20 $V_{pk\text{-}pk}$. Therefore, an op amp is needed with a slew rate fast enough to give 20 $V_{pk\text{-}pk}$ up to 10 kHz. By checking *Figure 4*, it is apparent that an op amp is required with

Second Requirement

$$\text{slew rate} \geq 0.85 \text{ V/}\mu\text{s}$$

Step 4 — Input Resistance
(Progress, July 1974)
The input impedance for the non-inverting configuration is given by

$$Z_{IN} = Z\left(1 + \frac{A_{VOL}}{1 + \frac{R2}{R1}}\right) \qquad (2)$$

where Z is the op amp input impedance and R3 ≪ Z.

The op amp for this design must satisfy the amplifier input impedance requirement of 5 MΩ up to at least 10 kHz. In step 2, it was determined that the op amp must also have an A_{VOL} of no less than 28 dB (or 25 V/V) at 10 kHz. Therefore, the required op amp must have an input impedance at 10 kHz of at least the following.

Third Requirement

$$Z \geq \frac{Z_{IN}}{1 + \frac{A_{VOL}\text{ (10 kHz)}}{1 + \frac{R2}{R1}}} = \frac{5\text{ M}\Omega}{1 + \frac{25}{10}} = \frac{5\text{ M}\Omega}{3.5}$$

$$Z \geq 1.4\text{ M}\Omega$$

From curves, such as that of *Figure 5*, of input resistance and input capacitance as a function of frequency, it is easy to select an op amp to meet the input impedance requirement.

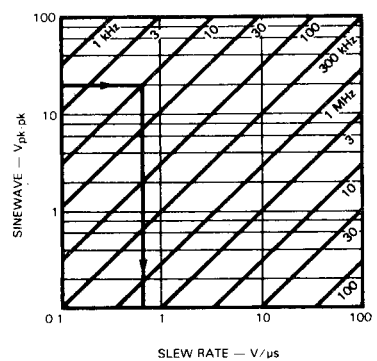

Figure 4

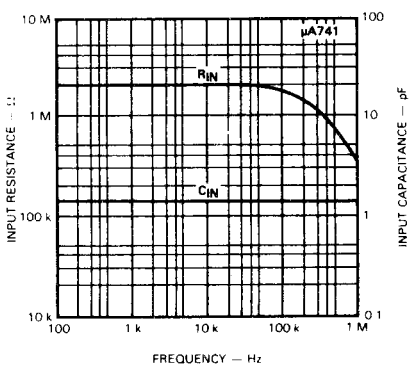

Figure 5

Step 5 — Maximum DC Output Offset Voltage, V_O
(Progress, March and April 1974)
The dc output offset voltage, V_O, for the circuit in *Figure 1* is given by the following equations.

For R3 = 0

$$V_O = (1 + \frac{R2}{R1}) V_{OS} + I_{Bias} R2 \qquad (3)$$

For R3 = R1 in parallel with R2

$$= \frac{R1\ R2}{R1 + R2}$$

$$V_O = (1 + \frac{R2}{R1}) V_{OS} + R2\ I_{OS} \qquad (4)$$

where V_{OS} = input offset voltage
I_{Bias} = input bias current
I_{OS} = input offset current

Unless the output offset voltage spec is very wide, it is usually more economical to add R3 than use a very low input bias current op amp. For the example in this discussion, R3 = R1 in parallel with R2. From *Equation 4*, it can be seen that the V_O value will be low when R2 is small; therefore the smallest possible value should be chosen for R2. From *Equations 1* and *2*,

$$\frac{R1 + R2}{R1} = 10 \text{ and } R3 \ll Z$$

Therefore, choose R1 = 10 kΩ ; then R2 = 90 kΩ and R3 = 9 kΩ and *Equation 4* becomes

$$V_O = (1 + 9) V_{OS} + (100 \times 10^3) I_{OS}$$

Thus, an op amp is needed such that V_{OS} and I_{OS} give

Fourth Requirement

$$10 V_{OS} + (100 \times 10^3) I_{OS} \leq 25 \text{ mV} \leq V_{O(max)}$$

To simplify the search for an op amp to meet this requirement, look first for one that has the following specs.

$$V_{OS} < \frac{V_{O(max)}}{10} \text{ or } < \frac{25}{10} \text{ mV}$$

$$I_{OS} < \frac{V_{O(max)}}{100 \times 10^3} \text{ or } < 250 \text{ nA}$$

Step 6 — Drift
Drift is given by

Fifth Requirement

$$\Delta V_O = 11\ \Delta V_{OS} + (100 \times 10^3)\ \Delta I_{OS}$$

$$\leq \Delta V_{O(max)} (15 \text{ mV})$$

where ΔV_{OS} and ΔI_{OS} are the changes in input offset voltage and input offset current over the 0 to 70° temperature range.

Final Hints in Choosing the Right Op Amp
It is usually best to start by finding the op amps that meet the first and second requirements; this will eliminate many. Then check the good ones with the third, fourth and fifth requirements starting with the lowest cost op amp. There are usually other specifications such as supply voltage and current, supply rejection, load current, etc., that should be considered. However, the op amps that meet the five requirements will narrow down the field of choice to only a few; they can then be checked further to see if they meet the rest of the specifications.