<B> 1 <D><R>
This device has initialization data which follows the Main Array data
in User Memory.
<B> 2 <D><R>
To program the Security Bit(s) of this device the Security fuse flag(s)
must be enabled.
<B> 3 <D><R>
This device has initialization data which follows the Main Array data in
User Memory. It also has an asynchronous/synchronous output enable bit
which follows the initialize word data in User Memory. Data for this bit
should be set at 00 for asynchronous mode, or 01 for synchronous mode.
Other data will generate a program or verify error.

<B> 4 <D><R>
This device has initialization data at device address 2000 hex,
following the Main Array. It also has an architecture byte at device
address 2001 hex. The following table shows the architecture data for
the three modes of operation.

Asynchronous operation   address 2001, value 00 hex
Synchronous operation   address 2001, value 01 hex
Initialize word operation   address 2001, value 02 hex
<B> 5 <D><R>
Set device block size to 4000 hex.
<B> 6 <D><R>
Security bit programming may be enabled in the Program
Memory Device Options screen; this overrides the Mask Option Register
(MOR) security bit value in User Memory. Note that there are two menu
selections for the 68705S3: mask set 1TJ6 identifies parts produced
before 1987, and mask set 0A20T identifies parts produced since January
1987.
<B> 7 <D><R>
This device's memory map is offset to User Memory Address 0000 hex. If your
data file contains a memory map that corresponds directly to the memory map
of the device then you will need to adjust the I/O Address Offset during the
loading of your data file. The I/O Address Offset must be set such that your
data is translated to User Memory Address 0000 hex.
<B> 8 <D><R>
This device's memory array begins at address 80 hex. The programmer
will automatically transfer data from User Memory to the device by the
required offset. If the data block begins at User Memory 0 hex, it will
be translated to device address 80 hex during a program operation.
Conversely a load operation will transfer the data block from device
address 80 hex to User Memory address 0.
Consult the Manufacturer's specifications for information about the
device memory map.
<B> 9 <D><R>
This device contains a special sector(s) which may be referred to by various
manufacturers as: SecSi sector, Hidden ROM, Protection Register, etc. This
specialty sector is One Time Programmable, trying to reprogram this sector may
cause programming errors. If you are reprogramming this device please make
sure this sector is disabled in the "SECTOR CONFIGURATION" table. Please read
the associated application notes for details.
<B> 10 <D><R>
The address block for this device is defined with the configuration
byte at location 103F hex (low nibble only). The EEPROM is located at
address B600 to B7FF hex. The two ROM blocks are at addresses BF40 to

BFFF and E000 to FFFF hex.
<B> 11 <D><R>
This device does not support block limits. Memory locations not defined
as EPROM or EEPROM are set to zero. The configuration byte, located at
address 103F, specifies the starting address of the EEPROM memory and
enables/disables the COP system watch dog timer.

The upper nibble of the configuration byte defines the most
significant bit of the starting address of the EEPROM memory.
If the configuration byte is set to 3F hex, then the EEPROM
starting address is 3800 hex (3000 hex + 800 hex). Note that the
upper nibble of the configuration byte cannot be set to B hex.

The lower nibble of the configuration byte defines the
enable/disable state of the COP system watch dog timer.
This nibble can only be set to F hex (disable) or B hex (enable).
<B> 12 <D><R>
To enable Sector or Boot Block Protection the individual Sector(s) or
Boot Block(s) must be enabled in the "SECTOR CONFIGURATION" table and
the 'Program Security fuse 1' must be Enabled.
<B> 13 <D><R>
For proper device operation, you may need to install a 0.1uF
bypass capacitor onto the adapter between device power and
ground pins.
<B> 14 <D><R>
Data to be programmed to device begins at address 0000H in programmer
user ram (corresponds to device address FC0000H). Ensure that
program data in user ram is allocated correctly. Special purpose
memory map is described in device specification. Ensure that
reserved locations are filled with required data.

To program Uprom bits, set "Program Configuration" flag (Program screen)
and edit ram location 20000H(x16)/40000(x8) as follows:

                    DEI   BIT2
                    DED   BIT3
                    OSC1   BIT6
                    OSC2   BIT7

Then, set corresponding bit in ram to 1.

To program loc bits, set "Program security fuse 1" flag
(programming screen). Ensure that desired data is in correct
ram location for CCB0.
<B> 15 <D><R>
Option register bits are programmed by entering data into the byte
immediately following the main array data. To program a bit, enter
a zero into the corresponding bit location as follows:
        Bit 0 ---- Eprom Protect
        Bit 1 ----   Ram Protect
        Bit 2 ----   XTAL Osc Option
        Bit 3 ----   Auto Latch Dsbl
        Bit 4 ----   WDT Perm Enable
        Bit 5 ----   Low Freg Osc
        Bit 6 ----   HVD Kill bit
To program the Eprom Protect bit and the HVD Kill Bit, the 'Program
Security Fuse' flag in the programming screen must be set to 'Y' as

well.

<B> 16 <D><R>
Due to ram limitations on the Unisystem programmers, this device
has been partitioned into several equal 32Mbit quadrants. More
details regarding this issue is available in the following on
line application note: 4meg_mem.txt
To make the appropriate menu selections use the following references:

* 8MBytes x16 device mapped into two User RAM memory partitions:
suffix L = Device addresses 0 -> 1FFFFF hex (0->3FFFFF for 8-Bit)
suffix U = Device addresses 200000 -> 3FFFFF hex (400000->7FFFFF for 8-Bit)

* 16MBytes x16 device mapped into two User RAM memory partitions:
```
                   I/O addr     Memory begin  User data    Device address
Menu selection: offset:        address:       size:        range:
suffix A0:      0 hex          0 hex          200000 hex   0        -> 1FFFFF hex
suffix A1:      400000 hex     0 hex          200000 hex   200000 -> 3FFFFF hex
suffix A2:      800000 hex     0 hex          200000 hex   400000 -> 5FFFFF hex
suffix A3:      C00000 hex     0 hex          200000 hex   600000 -> 7FFFFF hex
```

NOTE: 8-Bit devices the User Data Size and Device Address Ranges are doubled
<B> 17 <D><R>
Pins 9, 21, 37, 42, 43 and 48.
<B> 18 <D><R>
Device has Security Data and User Data features (enable in
PROGRAM DEVICE Options screen). User Data bytes are at address 801 and 802 hex.

<B> 19 <D><R>
To use this device, early versions of UniSite must be modified to
ensure that UniSite complies with programming specifications. Data I/O
will modify UniSite model numbers 901-0058-001 through 901-0058-006
free of charge. Contact Data I/O Customer Support for further
information.
<B> 20 <D><R>
Main array fuses are 512 through 1535. Polarity fuses are 2053 and 2054.
Remaining are phantom fuses (Load resets to zero). Checksum in JEDEC will
reflect phantom fuses but Program and Verify will be unaffected.
<B> 21 <D><R>
The window on these devices must be covered with an opaque label
during any operation!!!
<B> 22 <D><R>
Cross Programming support for GAL devices are listed in the Cross
Programming section of the Device List.
<B> 23 <D><R>
This device contains two separate EPROM areas, one for Instruction
information and the other for Data. The Instruction memory space is
address 0 to 7FF hex; the instruction data consists of 4 bytes, three
information bytes followed by a null byte.

The Data memory space is address 800 to BFF hex; data is oriented in
reverse order with address BFF hex as the first byte and address 800
hex as the last address. This format is compatible with the NEC 77P20
assembler. See NEC's 77P20 data book for more information.
<B> 24 <D><R>
Security bit programming may be enabled in the Program Memory Device
Options screen. The locations 9-B hex, D-F hex, 18-3F hex, and the most

significant byte of C hex are reserved for special functions and are not programmable. These locations will always load as FFFF hex or FF hex for location 00C. If data is entered at these locations, a verify error occurs, but data will not be programmed into the device.

The least significant byte of location C hex is the Chip Configuration byte, which is programmable. The two most significant bits of this location are the lock bits which can only be programmed if the Security Bit programming is enabled from the Program Device Options screen. Consult the Manufacturer's specifications for further information. This device does not need to have the Byte Swap Option enabled.
<B> 25 <D><R>
This device is a microcontroller with two security options. Currently, only one of the two security options may be implemented per device.

The first security option protects against in-circuit reads. This option is selected from the program screen. The second security option is activated by programming device addresses 782 hex and 783 hex with data 20 hex and FE hex respectively. This prevents the part from entering program mode.

Addresses 782 hex and 783 hex may also be used for normal data, however, once data is programmed at these addresses, you must erase the device before attempting another program operation.
<B> 26 <D><R>
This device has special programmable registers that can be programmed by entering data at locations following the Main Array. The CLR register is located at device address 8000 hex. The SFR register is located at device address 8001 hex. The SFRLR register is located at device address 8002 hex. Refer to the manufacturer's spec sheet for the correct data pattern (leave all undefined bits as 1s).

If the EPROM array and the SFR registers are programmed to overlap, the programmer will fill the overlapped section in RAM with zeros.
<B> 27 <D><R>
This device has a data format very similar to that described in footnote 23. The major difference is in the partitioning of the EPROM space. Instruction data memory space is at 0 to 1FFF hex. Data memory space is at 2000 to 27FF hex with the first data word at address 2000 hex.
<B> 28 <D><R>
This programmer does not fully support all structured test cases for this device.
<B> 29 <D><R>
Any of the three security options can be implemented for this device (Encryption Array data, Security Bit 1 or Security Bit 2). You can select the security options from the PROGRAM DEVICE Options screen. Once any of the security options have been programmed into the device, no further programming is allowed.

Illegal operations will generate one of these error messages:

A. Encryption Array Already Programmed - A programming operation has been attempted after the Encryption Array has been programmed.

B. Security Fuse Programmed or Bad Device - A programming operation has been attempted after security bit 1 has been programmed.

C. Security Fuse Violation - A programming operation has been
attempted after security bit 2 has been programmed. This error will
also be generated for a load or verify operation.

D. Test Fuse Programming Error - This error will be displayed
if there is a programming error in the Encryption Array.

Data in the programmer's User Memory is partitioned as follows:

    MAIN ARRAY DATA   0 through 7FF hex
    ENCRYPTION ARRAY DATA   800 through 80F hex

Enter Encryption Array data by editing the appropriate address in User
Memory.

After the Encryption Array is programmed, device data will no longer
match data in User RAM. Encryption Array and Security Bit data cannot
be read from the device.
<B> 30 <D><R>
Security bit programming may be enabled in the PROGRAM MEMORY DEVICE
Options screen.

The device's memory map starting at address 2000 hex is offset to User
Memory address 0000 hex. Fill first 10000 hex bytes in User Ram with
FF hex before file downloading. Partial device operation is not
allowed.

Locations B, D-F, 20-3F and the most significant bytes of A and C hex
are reserved for special functions and are not programmable, These
addresses will always load as FFFF hex (FF hex for addresses 00A and
00C). If data is entered at these addresses, a verify error occurs,
but the data will not be   programmed into the device.

The least significant byte of address A hex is the PPW byte, which is
programmable. The least significant byte of address C hex is the Chip
Configuration byte, which is programmable. The two most significant
bits of this location are the lock bits which can only be programmed if
the Security Bit programming is enabled from the Options screen.
Consult the manufacturer's specifications for further information.

The most significant byte of address 000C must be set to 20 hex.
<B> 31 <D><R>
This device does not support Illegal Bit Test or Blank Check.
Set Illegal Bit Test and Blank Check to (N) in the Program
Device Screen.
<B> 32 <D><R>
This device contains a User Electronic Signature (UES) array.
Programming this array is optional. For some devices two menu
selections may be available, one with the UES(or U) suffix and
one without. If there is a menu selection with UES(or U) then
this menu selection allows you to program all device data
including the UES data.

If your data file does NOT contain UES data, and you are trying
to use the UES supported menu selection, you will need to download
the data file to the programmer using format 92(JEDEC Kernel mode.)

NOTE: This is only recommended for data files targeted for the
specific device.

NOTE: If a non-compatible JEDEC data file is down loaded to the
programmer one of the following errors will be displayed:
"File not initialized." or "Incompatible User Data."

<B> 33 <D><R>
This device contains extra fuses which are automatically configured by
the programmer. If these extra fuses fail to program, an error occurs.
However, since these fuses are not part of the fuse map, an
underblow/overblow operation will not indicate their presence.
<B> 34 <D><R>
NOTE: These parameters apply to your PPI Capacitor blocks and
not the device pins.
<B> 35 <D><R>
The security fuse flag must be enabled in order to program/enable the
Permanent Protection feature of the device.
<B> 36 <D><R>
This device has a Software Data Protection (SDP) mode. To have SDP
enabled during programming, the Software Data Protect option must be
enabled. To set Software Data Protect in TaskLink/PromLink, select
the "Enable Special Data" option under Setup/General Parameters. For
Terminal users, this flag is set in the PROGRAM DEVICE Options screen.
If this option is not enabled during programming the SDP mode will be
disabled after programming.
<B> 37 <D><R>
If you attempt to re-program this device after programming the security
fuse, a Device Over-Current Fault error may be generated and there is a
potential that the device may be damaged.
<B> 38 <D><R>
This device has initialization data that follows the Main Array located
at device address 800 hex. The device also has an architecture byte
located at 801 hex. The following table shows the architecture data for
the four modes of operation.

Asynchronous Enable, Asynchronous Initialize 801 hex = FF hex
Synchronous Enable, Asynchronous Initialize 801 hex = FE hex
Asynchronous Enable, Synchronous Initialize 801 hex = FD hex
Synchronous Enable, Synchronous Initialize 801 hex = FC hex
<B> 39 <D><R>
Data I/O programmers require a .DIO binary file (format 10) to
program Actel devices. This file can be generated using Actel's
Action Logic System software. After downloading the file to
the programmer do not change the User Data Size in the program
screen. For more information you can contact Data I/O Customer
Support and request the Actel Programming Application Note.
<B> 40 <D><R>
The algorithm for this device does not support Preload vectors.
<B> 41 <D><R>
Pins 14, 15, 28, 29, 42, 44
<B> 42 <D><R>
Pin 1 of the device must be placed in the lower left corner of the socket.
<B> 43 <D><R>
Device has 12 bit data word which is represented as
16 bit data for the programmer. Unused bits are
loaded from the device as zeros, ignored during

Verify operation, and automatically set to zeros
during programming.

Security bit programming may be enabled in the Program
Memory Device Options screen. Oscillator selection bits
cannot be reprogrammed if they were configured by the
factory (OTP devices only).

When assembling source file, use output option that
produces merged 8 bit Intellec Hex object file (INHX8M)
then download to programmer by selecting the
Intel Intellec 8/MDS translator (code 83).
<B> 44 <D><R>
This device is thinner than most JEDEC type PLCC devices, therefore an LCC
Spacer may be required in order to insure proper contact is made between the
device and programmer's hardware interface. A device insertion error occurs
when the device makes poor contact with the programmer's hardware interface.
Contact Data I/O Customer Support for information regarding LCC Spacer Kits.
<B> 45 <D><R>
This device has a differential cell array. Any unprogrammed location is in
an undetermined state. Loading an unprogrammed device will produce
inconsistent checksums. Verify operations are valid only after the device
has been programmed. Some differential cell devices support a special
blank check routine. If blank check is supported, attempts to reprogram a
non-blank device will generate an illegal bit error.

Although setting block limits is allowed, it is recommended that the
entire device be programmed to avoid ambiguous states.
<B> 46 <D><R>
Partial device operations are not allowed on this device. If your data
file is smaller than the device size, make sure that the extra
locations in User RAM are filled with the blank state (FF hex).
<B> 47 <D><R>
The data file used to program this device contains the security option
data. The Security option will not be programmed into the device unless
it is enabled from the Programming Options screen.
<B> 48 <D><R>
This device has an asynchronous/synchronous output enable bit that
follows the Main Array data in User Memory. The outputs are enabled
synchronously when programmed to 1.
<B> 49 <D><R>
This device contains an Electronic ID. If an ID error occurs, the wrong
device is selected or the version of this device is not supported. A
software update may be required. Contact Your Customer Support
Representative for more information.

Any shorts test is not supported on the UniSite programmer.
<B> 50 <D><R>
This device does not support the test code/checksum and test signature
features.
<B> 51 <D><R>
Data in the Programmer's User Memory is partitioned as follows:

```
                                      87C508
                          89C420      87C51RC2
              87C5112     87C51RB2    87C528
              87C52X2     87C51U2     5962-9056401XA
```

```
                         87C51GB   87C54X2   87C58        87CE560
                         87x51xA   87x51xB   87x51xC      87C51RD
                         87x52     87x54     87x58        87C51RD2

                         -------   ---------  ---------   -----------
  MAIN ARRAY DATA        0000-1FFF 0000-3FFF 0000-7FFF   00000-0FFFF
  ENCRYPTION ARRAY DATA  2000-203F 4000-403F 8000-803F   10000-1003F
```

 X = C or L; Such as 87C52 or 87L52
<B> 52 <D><R>
This device is a microcontroller with Security Bit programming
capability. Security Bit programming may be enabled in the Program
Memory Device Options screen. (No Uprom bit programming in UniSite 3.0
or 2900 1.2.)

The device's memory map starting at address 2000 hex is offset by 2000
hex bytes to start at the User Memory address 0000 hex. Because of
differences in assemblers, fill first 10000 hex bytes in User Ram with
FF hex before file downloading. Partial device operation is
not allowed.

This device also has address locations in the programmable array area
that are reserved for special functions and are not programmable. These
addresses are B, D-F and 2F-3F hex. These locations will always load as
FFFF hex. If data is entered in User RAM at these locations, a verify
error occurs, but no data will be programmed at those locations.

Address C hex is also reserved. The most significant byte of C hex is
always programmed to 20 hex. If data other than 20 hex is entered in
User RAM at this location, a verify error occurs, but data 20 hex will
be programmed.

The least significant byte of address C hex is the Chip Configuration
byte, which is programmable. The two most significant bits of this
location are the lock bits, which can be programmed only by selecting
the Security Bit programming option in the PROGRAM Options screen.
Consult the Manufacturer's specifications for further information.

The User Ram is showed in words as default. It may be more convenient
to select Data Word Width = 8 and then follow memory map in Intel's
User's Guide.
<B> 53 <D><R>
This device contains a security fuse, however, the option is currently
not supported. If you attempt to program the security fuse manually,
the part will secure. However, reprogramming will no longer be
possible.
<B> 54 <D><R>
This device does not support upload, output to disk, fill
RAM, Edit data or Blank check. Disable the "Blank Check"
option, located on the Programming Options screen, to avoid
invalid non-blank and illegal-bit errors.
<B> 55 <D><R>
This device does not support output to disk, Fill RAM, Edit data or
Blank check. Disable the "Blank Check" option, located on the
Programming Options screen, to avoid invalid non-blank and illegal-bit
errors.

This programmer supports POF files generated by the MAXPLUS (TM Altera)
```

development system software version 2.5 or later.

Some POF files contain "don't care" data that is calculated into the
data checksum. If you perform a Load operation after programming a
downloaded file, the checksum may be slightly different.
<B>  56  <D><R>
This device has an architecture byte at address 8000 hex. Set the
appropriate bits to 1 to program the desired features into the device.
Set all unused bits in the architecture byte to 0.

ADDR        BIT        FUNCTION        DEVICES SUPPORTING FEATURE

8000 hex  2          ALE polarity    Cypress 7C277 and 7C279
8000 hex  1          ALE enable      Cypress 7C277 and 7C279
8000 hex  0 (LSB)    SYNC enable     Cypress 7C277
<B>  57  <D><R>
The data files generated for PSD devices may contain data at non-programmable
locations.  In order to get the correct device checksum you may need to enable
the "Use Algorithm Checksum" feature in TaskLink.

Security Bit (SECA) is programmed only if the security fuse flag is enabled.

To ensure proper download of PSD data file, set download options as follows:
    I/O Translation Format  99
    I/O address offset        0
    Memory begin address      0
    User data size            0
<B>  58  <D><R>
Pins 8, 24
<B>  59  <D><R>
Pin 44
<B>  60  <D><R>
This device has very specific memory map format requirements.  Please read the
associated application notes for details before performing device operations.
<B>  61  <D><R>
To program the encryption array feature you must set the Special Data #1 flag
to Y in TaskLink or the "Program XNOR data" flag to Y in Terminal mode.
<B>  62  <D><R>
The Lattice adapter used to program this device also requires a second
connector board called the Lattice "28-pin Converter" (Lattice Part
Number "pDS4102-28P2SAB"). The "28-pin Converter" is used in conjunction
with Lattice pDS4102-xxxx and PA-xxxx adapters.
<B>  63  <D><R>
To program the protection register lock bit you must enable or set to Y the
"Program security fuse" flag.  Please read the associated application notes
for further details.
<B>  64  <D><R>
pin 11, 27, 32, 50, 51, 65, and 66
<B>  65  <D><R>
Set device begin address and device block size to 4000 hex.
<B>  66  <D><R>
This device has three security options that can be enabled by setting the
corresponding Security fuse flag or set of flags:

Program Security fuse 1: Lock Bit 1
Program Security fuse 2: Lock Bit 2
Program Security fuse 3: Lock Bit 3

```
Program Lock Bits
------------------------
      LB1    LB2    LB3
      ---    ---    ---
1     U      U      U       No program lock features
2     P      U      U       Further programming of device memory is disabled
3     P      P      U       Further programming and verify is disabled
4     P      P      P       Further programming, verify and external execution
                           is disabled
```

(U) un-programmed
(P) programmed
<B> 67 <D><R>
Place jumper JP1 on adapter to 64. Set device
begin address to 800 hex and device block size to 1800 hex.
<B> 68 <D><R>
For enabling security fuse flags in TaskLink for windows(TLwin)
or TaskLink for DOS(TLdos) you must set the appropriate Security
Option value as described below. Setting these values is done
under the Programmer Properties menu selection(TLwin) or the
General Parameters menu selection(TLdos).

Enabling security fuse flags in TaskLink for windows or TaskLink
for DOS where devices have up to and including 3 security fuses:

To set all of the security fuse flags use option value 3.
To set only the First security fuse set security option to 4.
To set only the Second security fuse set security option to 5.
To set only the Third security fuse set security option to 6.

```
  Option        Security Fuse(s)
  Value         Programming       Fuse(s)       Data =
  --------------------------------------------------------
  0             Disabled          All           0
  1             Disabled          All           1
  2             Enabled           All           0
  3             Enabled           All           1
  4             Enabled           First         1
  5             Enabled           Second        1
  6             Enabled           Third         1
```

For enabling special data in TaskLink for windows(TLwin) or
TaskLink for DOS(TLdos) select the appropriate special data
flag under the Programmer Properties menu selection(TLwin)
or the Special Features menu selection(TLdos)
<B> 69 <D><R>
Place jumper JP1 on adapter to 64.
<B> 70 <D><R>
Consult the Manufacturer's specifications for further information.
<B> 71 <D><R>
Set device begin address to 1000 hex and device block size 3000 hex.
<B> 72 <D><R>
Enable "Program security fuse 3" flag to program Hardware Write Protection.
<B> 73 <D><R>
Lock bit 1 (write protect) is not supported.
<B> 74 <D><R>

Security fuse 1: Write Protects the device.
Security fuse 2: Read/Write Protects the device.
<B> 75 <D><R>
This device has programmable locations with specific data format
requirements. You will find this data referred to in DATA I/O
Application Notes by one of the following terms:
Special Device Feature, Configuration Byte(Word), Option Byte(Word)

To program this device specific data in TaskLink you must set the
Special Data #1 flag to Y.
To program this device specific data in Terminal mode set the "Program
Configuration" flag to Y.
<B> 76 <D><R>
Pins 44, 34, 12
<B> 77 <D><R>
Set device block size to 1000 hex.
<B> 78 <D><R>
No continuity test or empty socket test are performed on this device. If you
receive a programming error please validate device is correctly oriented in
socket before performing any further device operations.
<B> 79 <D><R>
For more information, the following application notes(or files) can be
downloaded from the Data I/O Web Site or FTP site:

        atm_dev.txt ---- for Atmel devices
        dal_dev.txt ---- for Dallas devices
        rtr_dev.txt ---- for Ramtron devices
        sai_dev.txt ---- for Saifun devices
        spa_dev.txt ---- for Spansion devices
        stm_dev.txt ---- for STMicroelectronics devices
        xil_dev.txt ---- for Xilinx devices

These files will be updated periodically. To download the files use:
ftp://ftp.dataio.com/appnotes/
<B> 80 <D><R>
Pins 8, 32
<B> 81 <D><R>
To enable this device's Security/Protection features you must enable the
'Program Security fuse' flag. This device supports several specific
protection configurations, selection of a specific protection configuration
can be made using the "SECTOR CONFIGURATION" table. Please note that the
highest level of protection will be the default configuration if a specific
protection configuration is not selected.
<B> 82 <D><R>
Enable the following flags to program the device's Protection/Security Bits:
Program Security fuse 1: Block Protect 0 (BP0)
Program Security fuse 2: Block Protect 1 (BP1)
Program Security fuse 3: Block Protect 2 (BP2) (NOTE: Where applicable)

Enabling the "Erase EE device" option will remove all block protection.
<B> 83 <D><R>
The "R" in the menu name defines this support as a reverse pin-out device.
Therefore the Pin#1 mark on the device will not match to Pin#1 mark on the
adapter. To insert the device correctly please make sure device Pin#1 is
180 degrees from the pin#1 marker on the adapter.
<B> 84 <D><R>
This menu selection is for the obsolete hardware configuration. To use the

current hardware configuration please select the alternate menu selection.
<B> 85 <D><R>
Pins 18, 52
<B> 86 <D><R>
Device has phantom fuses in the JEDEC fuse map (ignored
during Program and Verify operations). Fuses will load as ones.
Device must be erased before re-programming to avoid error.
<B> 87 <D><R>
Examples of a revision numbers: "410-xxxx-002", "410-xxxx-003", etc...
<B> 88 <D><R>
Examples of a revision numbers: "715-xxxx-002", "715-xxxx-003", etc...
<B> 89 <D><R>
The "_O" menu selection defines this support as the un-revised or obsolete
hardware or algorithm support solution. Please use alternate menu selection
if you are programming this device for the first time, or contact Data I/O
Customer Support for a new support solution.
<B> 90 <D><R>
pin 50, 51
<B> 91 <D><R>
Enable "Program protect reg." flag to program Hardware Write Protection.
<B> 92 <D><R>
Switches on socket adapter (see socket adapter operational manual)
allow individual devices on card to be programmed.
Programmer block size will default to size of an individual device.

<B> 93 <D><R>
Sector operations are set up under the "SECTOR CONFIGURATION" table. This
table allows the user to select specific sector operations such as Erase,
Program, or Protect. The following directions will assist you in navigating
to this table relative to your programmer interface:
For the TaskLink user:
The "SECTOR CONFIGURATION" table is located in the "Sector" tab under
"Programmer Properties" dialog box.
For the Hiterm/Terminal user:
The "SECTOR CONFIGURATION" table is located in the "Device Configure" screen.

The algorithm supports individual sector control for program, Erase and
protection. Use flags "Erase", "Program" and "Protect" corresponding to
each sector.
1. When "Erase" flag of any sector is set to "YES" then irrespective
   of protect status, at next erase operation the sector will get erased
   and protect status will become "Unprotected".
2. After Programming the protect status will be set to the "Protect status
   flag" value.
3. The "Load" operation reads the protect status and updates the Protect
   status flags.
4. Programming a protected sector is not allowed. Attempting to program
   a protected sector may produce a programming error.
<B> 94 <D><R>
This device does not allow programming of a Non-Blank device.
The programmer performs a Blank check as part of the Program
operation.
<B> 95 <D><R>
Device has one or more architecture bits contained in one byte at
address 10000 hex. Set the appropriate bits to 1 to program desired
features into device:

```
ADDR        BIT       FUNCTION        DEVICES SUPPORTING FEATURE


10000 hex  7(msb)    CS2 polarity    Cypress 7C289
10000 hex  6         CS1 polarity    Cypress 7C289
10000 hex  5         WAIT polarity   Cypress 7C289
10000 hex  4         WAIT timing     Cypress 7C289
10000 hex  3         ALE polarity    Cypress 7C289
10000 hex  2         ALE enable      Cypress 7C289
10000 hex  1         Address setup   Cypress 7C289
10000 hex  0(lsb)    SYNC enable     Cypress 7C287
```
<B> 96 <D><R>
Device requires a socket adapter to interchange pins 1 and 4
between device and ZIF socket.
<B> 97 <D><R>
-
<B> 98 <D><R>
-
<B> 99 <D><R>
To enable the "Protected Boot-Block Overide" feature:
- In TaskLink you must set the Special Data #1 flag.
- In Terminal mode set the "Reset Clock" flag to "Y".
<B> 100 <D><R>
Set device size to 4000 hex.
<B> 101 <D><R>
1,2,4,7,10
<B> 102 <D><R>
The "Erase EE device" option MUST be enabled when programming this device.
<B> 103 <D><R>
Data bits 5-7 should be set to ones at all
address locations. Refer to manufacturer spec sheet for
correct data pattern.
<B> 104 <D><R>
Set device size to 4000 hex. Data bits 5-7
should be set to ones at all address locations. Refer to
manufacturer spec sheet for correct data pattern.
<B> 105 <D><R>
-
<B> 106 <D><R>
-
<B> 107 <D><R>
-
<B> 108 <D><R>
Block limits are not supported for this device. The entire memory
array will be erased automatically during a programming operation.
<B> 109 <D><R>
At address locations 0 to FFF hex, data bits 4-7 should be set to ones.
At address locations 1000 to 1FFF hex, data bits 5-7 should be set to
ones. Refer to the manufacturer's spec sheet for the correct data
pattern.
<B> 110 <D><R>
-
<B> 111 <D><R>
-
<B> 112 <D><R>
-
<B> 113 <D><R>
-
```

<B> 114 <D><R>
To program the first 128K, select bank 0.
Maximum device size is 20000 hex. To program the last 64K, select bank
1. Maximum device size is 10000 hex.
<B> 115 <D><R>
-
<B> 116 <D><R>
-
<B> 117 <D><R>
-
<B> 118 <D><R>
Device uses 3.0V on VCC for Load, Program, and Verify
operations. VCC voltages applied during two-pass Verify
are 3.0V and 3.5V.
<B> 119 <D><R>
Structured testing is not supported for this device on the ChipSite
module.
<B> 120 <D><R>
This device's memory map has a starting address of 1000 hex(x16 address,)
which is an offset of 2000 hex bytes from the start of User Memory address
0000 hex. This is due to differences in assemblers that generate files for
this device.   You must fill the first 10000 hex bytes in User Ram with FF
hex before downloading your data file to avoid possible programming problems
NOTE: Partial device operation is not allowed.

When in the editor the User Ram is shown in word wide device address format.
It may be more convenient to select Data Word Width = 8 and then follow
memory map in Intel's User's Guide.

This device has address locations in the programmable array area that are
reserved for special functions and are not programmable. These addresses are
100A hex, 100B hex, 102F->103F hex, and the least significant bytes of
100E hex and 100F hex. Fill these locations in User RAM with FF hex.

Fill the most significant bytes of 100C hex, 100D hex , 100E and 100F hex
in User RAM with 20 hex.

The least significant byte of 100C hex (the CCB byte) is programmable.
The two most significant bits of this location are programmable lock bits,
which can be programmed only by selecting the Security Bit programming
option in the PROGRAM Options screen.

To program the CCB1 and Security Key bytes (the least significant byte
of 100D hex and all bytes of address 1010-1017 hex) consult the
manufacturer's specifications.
<B> 121 <D><R>
!!!!USE ONLY FOR FX-CORE DEVICES!!!! FX core devices can be distinguish
from older 87C51/87C51FA/87C51FB devices via the topside tracking
number (FPO number)marked on the part. The topside tracking number on
FX core devices will end with a letter 'A'. For more information call
INTEL.

Any of the four security options can be implemented for this device
(Encryption Array data, Security Bits 1, 2 or 3). The security options
can be selected from the PROGRAM DEVICE Options screen. The encryption
array has data in User Memory.

Data in the Programmer's User Memory is partitioned as follows:

```
                   87C511
DEVICE             87C51 (FX)      87C51FA (FX)    87C51FB (FX)
------------       ------------    ------------    -------------
MAIN ARRAY         0 - 0FFFh       0 - 1FFFh       0 - 3FFFh
ENCRYPT. ARRAY     1000 - 103Fh    2000h - 203Fh   4000h - 403Fh
```

Enter Encryption Array data by editing the appropriate address in User
Memory.

After the Encryption Array is programmed, device data will no longer
match data in User RAM. Encryption Array data cannot be read from the
device.
<B> 122 <D><R>
-
<B> 123 <D><R>
-
<B> 124 <D><R>
-
<B> 125 <D><R>
This device must have the Device Begin Address set to zero, for partial
programming to function properly
<B> 126 <D><R>
This device must have the Device Begin Address set to zero, and the
Device Block Size is set to an even number, for partial programming to
function properly
<B> 127 <D><R>
-
<B> 128 <D><R>
-
<B> 129 <D><R>
Some devices may generate intermittent programming errors (low yields).
If this occurs, repeat the program operation. Data I/O is currently
working with the semiconductor manufacturer to improve yields.
<B> 130 <D><R>
This algorithm's data file memory map does NOT map directly to the memory map
recommended for this device. For details regarding the differences between
this algorithm's data file memory map and the memory map recommended by the
semi manufacturer please refer to the corresponding DATA I/O application note.
<B> 131 <D><R>
This device has a non-contiguous memory map. To insure the integrity
of the programmer's checksum, the unused and/or un-programmable memory
locations in user RAM must be set to zero prior to loading a device
or downloading a data file. For more information of using RAM Fill
please refer to TaskLink online help, or your programmer manual.

Consult the Manufacturer's specifications for further information.
<B> 132 <D><R>
The illegal-bit and blank check operations are only executed on the
EPROM array.
<B> 133 <D><R>
The device memory space is partitioned as follows :

```
        ARRAY          TYPE              ADDRESS
   ------------    ------------      ------------
   INSTRUCTION    PROGRAMMABLE        0-1FFF hex
```

```
   RESERVED         UNPROGRAMMABLE   2000-4FFF hex    fill with FF hex
   DATA             PROGRAMMABLE     4800-4FFF hex
```

Instruction and data arrays have unused bit locations which must be
set to ones. This should be done by your development tools.
Refer to the device specification sheet for more information.

<B> 134 <D><R>
The device memory space is partitioned as follows :

```
        ARRAY          TYPE            ADDRESS
     ------------   ------------     ------------
   INSTRUCTION    PROGRAMMABLE         0-3FFF hex
   RESERVED       UNPROGRAMMABLE    4000-4FFF hex    fill with FF hex
   DATA           PROGRAMMABLE      4800-4FFF hex
```

Instruction and data arrays have unused bit locations which must be
set to ones. This should be done by your development tools.
Refer to the device specification sheet for more information.

<B> 135 <D><R>
Set device block size to 5000 hex.
<B> 136 <D><R>
-
<B> 137 <D><R>
-
<B> 138 <D><R>
Use in-module adapter (part number 615-1548-002 or greater) for
in-module programming.
<B> 139 <D><R>
The selected device has 2 algorithms available. The algorithm 705P9
should be used for devices with the mask 0D33N or later. The algorithm
705P9-D54E should be used for devices with the mask 0D54E.

The devices with mask 0D54E have an error in the boot loader which will
not allow the device to perform the following functions properly: load,
illegal-bit check and blank check. If the default 2 pass verify is not
used as the number of verify passes, please insure that the number of
verify passes is set to a minimum of 1.
<B> 140 <D><R>
The programmer's user RAM corresponds directly to the memory map of
the device, please refer to the device data sheet for details.
<B> 141 <D><R>
This device contains an Electronic ID. If an ID error occurs, the wrong
device is selected or different version of this device is selected. Two
different algorithms are available, 1810T and 1810T-NEW. If both
algorithms yield "DEVICE ID error" contact DATA I/O Customer Service.
<B> 142 <D><R>
This device is a microcontroller with Security and User Data
features. Enable the security bit or User Data bytes in the
PROGRAM DEVICE Options screen. The User Data Bytes(Program
Signature) are available at address 1001 and 1002 hex.

NOTE: If you want to perform a Program, Verify, or Illegal-Bit
      check on the User Data feature(Program Signature), you
      must enable this feature in the PROGRAM DEVICE Options
      screen.
```

```
<B>  143  <D><R>
If the default 2 pass verify is not used as the number of verify
passes, please insure that the number of verify passes is set to a
minimum of 1.
<B>  144  <D><R>
Data in the Programmer's User Memory is partitioned as follows:


Main array       0 - 3FFF hex
Unused bytes     4000h - 400C, 400E hex
ECON6            400D hex                (ROM0, RAM0 bits)
ECON7            400F hex                (security bits )


The ECON6 or ECON7 have misverified, if a 'Device verification error'
occurs during Verify, Blank check or Illegal bit check. To determine
which fuse has failed, load the device and view locations ECON6 and
ECON7 User memory locations.
<B>  145  <D><R>
Data in the Programmer's User Memory is partitioned as follows:


Main array       0 - 0FFF hex
ECON             1000 hex
<B>  146  <D><R>
-
<B>  147  <D><R>
The programmer does not support the "Software Data Protection" feature
during programming if the data word width is set to 16-bit or greater.


To use the "Software Data Protect" feature for word widths greater than
or equal to 16-bits, use the following procedure:


- Program the device/s with 16-bit(or larger) data word
  width and "Software Data Protection" disabled.
- Change data word width back to 8-bit.
- Load the programmed device.
- Re-program the device with "Software Data Protection"
  enabled.
<B>  148  <D><R>
For test vectors to run successfully on this device, the  JEDEC pin
swap function "P" needs to be used.  The JEDEC file should be modified
by inserting 4 lines after the last fuse number and before the first
vector:


Example:


L163073 1*
L163082 1*
L163091 1*       <-- last fuse number in JEDEC file
P 15 5 14 4 13 3 12 2 1 11 10 22 21 26 25 30 29 34 33 38 37
   42 41 46 45 49 50 60 51 61 52 62 53 63 54 64 55 65 56 66
   57 67 68 58 59 47 48 43 44 39 40 35 36 31 32 27 28 23 24
   20 19 9 18 8 17 7 16 6*
V0001 01NHXXHHX0HH0XHNHHXNHH11HH10HH11NX1XNX11XX0XXXXXXXNXXXN
       XXXXXXXXXXXXNX*    <-- first vector in JEDEC file
<B>  149  <D><R>
-
<B>  150  <D><R>
-
```

```
<B>  151  <D><R>
The Intel 85C22V10 algorithm is a 22V10 compatible device with superset
features. To determine the correct algorithm to use, view the JEDEC
file you wish to program and match the QF field to the following menu
entries:

QF=5848
-select the 85C22V10 algorithm under the Intel main menu.

QF=5828
-select the 22V10 or the IPLD22V10 algorithm under the Intel main menu.
 or
-select the 85C22V10 as a 22V10 algorithm under the Intel XPGM menu.

QF=5838
-select the 85C22V10 as a 22VP10 algorithm under the Intel XPGM menu.

QF=5892
-select the 85C22V10 as a 22V10UES algorithm under the Intel XPGM menu.
 The 85C22V10 does not support the UES bits, so these bits will be
 ignored in the JEDEC.
<B>  152  <D><R>
-
<B>  153  <D><R>
Currently, only EPROM protect option is supported. All bytes  on
secured device are read as FF hex. Secured device passes blank check,
but fails during programming.
<B>  154  <D><R>
This device requires socket adapter YANO2020A which has been discontinued by
the manufacturer. We are working with the manufacturer to determine if there
is a replacement adapter.
<B>  155  <D><R>
-
<B>  156  <D><R>
-
<B>  157  <D><R>
Not using ECC function, set device block size to 8000 hex.
Using ECC function, set device block size to A005 hex.
Set unused bits in ECC area to ones. Refer to device spec
sheet for more information.
<B>  158  <D><R>
-
<B>  159  <D><R>
-
<B>  160  <D><R>
-
<B>  161  <D><R>
-
<B>  162  <D><R>
Set device block size to A005 hex, if use ECC function.
Set unused bits in ECC area to ones. Refer to
device spec sheet for more information.
<B>  163  <D><R>
-
<B>  164  <D><R>
Set device block size to 2000 hex.
<B>  165  <D><R>
```

```
-
<B>  166  <D><R>
-
<B>  167  <D><R>
-
<B>  168  <D><R>
-
<B>  169  <D><R>
-
<B>  170  <D><R>
Data in programmer User Memory is partitioned as follows:

  NOT IMPLEMENTED          0 through 07FF hex
  RESERVED                 0800 through 087F hex
  PROGRAMMABLE             0880 through 0F9F hex
  RESERVED                 0FA0 through 0FEF hex
  PROGRAMMABLE             0FF0 through 0FF7 hex
  RESERVED                 0FF8 through 0FFB hex
  PROGRAMMABLE             0FFC through 0FFF hex
<B>  171  <D><R>
Data in the programmer's User Memory is partitioned as follows:

  CONFIG. BYTE            - 003F hex
  UNUSED                 - 0000 through 0D7F hex
  EEPROM ARRAY DATA      - 0D80 through 0FFF hex
<B>  172  <D><R>
Data in the programmer's User Memory is partitioned as follows:

  CONFIG. BYTE                      - 103F hex
  EEPROM ARRAY DATA      - FE00 through FFFF hex
<B>  173  <D><R>
This device has an electronically erasable array. When re-programming
this device, enable the "Erase before program" option.
<B>  174  <D><R>
In the  configuration register (at address 103F hex) only bit #2 (NOCOP) is read
able.
Therefore the register can obtain only two values if read.
      1.  FF hex  ----  COP  disabled
      2.  FB hex  ----  COP  enabled
<B>  175  <D><R>
Data in the programmer's User Memory is partitioned as follows:

  CONFIG. BYTE           - 003F hex
  EEPROM ARRAY DATA      - 0D80 through 0FFF hex
  EPROM  ARRAY DATA      - A000 through FFFF hex if 711K4/KA4
                         - 8000 through FFFF hex if 711KA2
                         - N/A if mask versions

  The Config. byte is electronically erasable
  (and may not be blank when device shipped from the factory).
<B>  176  <D><R>
Data in the programmer's User Memory is partitioned as follows:

  User EPROM             - 0F00 through 1F00 hex
  User Vectors           - 1FF0 through 1FFF hex
<B>  177  <D><R>
-
```

```
<B>  178  <D><R>
Consult the Manufacturer's specifications for further information
about values of the Configuration byte.
<B>  179  <D><R>
-
<B>  180  <D><R>
-
<B>  181  <D><R>
If using AR (Address register), set device block size to 4002 hex.
Else, set device block size to 4000 hex. Refer to device spec sheet
for more information.
<B>  182  <D><R>
-
<B>  183  <D><R>
-
<B>  184  <D><R>
-
<B>  185  <D><R>
-
<B>  186  <D><R>
-
<B>  187  <D><R>
-
<B>  188  <D><R>
When re-programming this device, disable the "Erase EE device" option
on the program screen by typing N. The device is erased automatically
during programming.

Data in the programmer's User Memory is partitioned as follows:

  DEVICE             EEPROM              EPROM
  ------          -------------      -------------
  370C610            none         7000 - 7FFF hex
  370C642            none         6000 - 7FFF hex
  370C710       1F00 - 1FFF hex   7000 - 7FFF hex
  370C722       1F00 - 1FFF hex   6000 - 7FFF hex
  370C742       1F00 - 1FFF hex   6000 - 7FFF hex
  370C756       1E00 - 1FFF hex   4000 - 7FFF hex
  SE371C7A7FN   1F00 - 1FFF hex   2000 - 5FFF hex, 6000 - 7FFF hex
  SE370758FZ    1F00 - 1FFF hex   2000 - 5FFF hex, 6000 - 9FFF hex
<B>  189  <D><R>
Data in the programmer's User Memory is partitioned as follows:

  RESERVED                      0 through 007F hex
  PROGRAMMABLE               0080 through 0F9F hex
  RESERVED                   0FA0 through 0FEF hex
  PROGRAMMABLE               0FF0 through 0FF7 hex
  RESERVED                   0FF8 through 0FFB hex
  PROGRAMMABLE               0FFC through 0FFF hex
<B>  190  <D><R>
-
<B>  191  <D><R>
The Clock Detect Enable bit for this device is enabled by programming
address 2016 hex of the device with the value DE hex. To program
address 2016 hex for this device, edit ram with a word width of 16 and
enter a DE hex in the LSB of location 0B hex.
<B>  192  <D><R>
```

Blank Check must be enabled for this device to program properly.
<B> 193 <D><R>
This device has address locations in the programmable array that are
not programmable, but must be set. To manually set these locations,
edit the programmer's User memory and fill the following locations:

```
User Memory                          Addresses
Address                              corresponding to
(16-bit data)        Fill Data      Device's memory map
--------------------------------------------------------
0E-0F hex            FFFF hex        201C-201F hex
2F-3F hex            FFFF hex        205E-207F hex
    0C hex           20xx hex              2019 hex
    0D hex           20xx hex              201B hex
```

xx - don't care

If this is not done, verify errors may occur.

The least significant byte of C hex (2018 hex of the part) is
the CCB0 byte and is programmable. The two most significant bits of this
byte are lock bits, which can only be programmed by selecting the
Program Security Fuse option in the PROGRAM options screen.
<B> 194 <D><R>
When Loading Ram from a "Master Device" a checksum conflict may occur.
This can be prevented by performing a FILL FUSE MAP operation under
the EDIT DATA menu before performing the LOAD operation.
<B> 195 <D><R>
Device is marked as HW on the bottom portion of this device.
<B> 196 <D><R>
Device is marked as HW on the top portion of this device.
<B> 197 <D><R>
This device has address locations in the programmable array that are
not programmable, but must be set. To manually set these locations,
edit the programmer's User memory and fill the following locations.

```
User Memory                          Addresses
Address                              corresponding to
(16-bit data)        Fill Data      Device's memory map
--------------------------------------------------------
2F-3F hex            FFFF hex        205E-207F hex
    0F hex           xxFF hex              201E hex
    0C hex           20xx hex              2019 hex
    0D hex           20xx hex              201B hex
    0E hex           20xx hex              201D hex
    0F hex           20xx hex              201F hex
```

xx - don't care

If this is not done, verify errors may occur.

The least significant byte of C hex (2018 hex of the part) is
the CCB0 byte and is programmable. The two most significant bits of this
byte are lock bits, which can only be programmed by selecting the
Program Security Fuse option in the PROGRAM options screen.
<B> 198 <D><R>
Device has two non-programmable areas,

address 0000 to 3FEF hex and 3FF6 to 3FFF hex. User data for these
locations should be set to FF hex. Refer to device spec sheet for more
information.
<B> 199 <D><R>
-
<B> 200 <D><R>
-
<B> 201 <D><R>
To enable Low Noise Mode, enable security fuse 1
in the PROGRAM options screen.

To secure the device, enable security fuse 2 in the PROGRAM
options screen (some load instructions will be
disabled).

<B> 202 <D><R>
Device has programmable reset polarity data which follows the Main Array
Data in User Memory. All four configuration bytes at these location must
be set as follows:

```
Core Device Name   Address Location     Data for setting the Reset Polarity
----------------   -----------------    -----------------------------------
1718                  8DChex ->   8DFhex  00h = active LOW; FFh = active HIGH
1736/37LV36          11B8hex ->  11BBhex  00h = active LOW; FFh = active HIGH
1765/37LV65           2000hex ->   2003hex  00h = active LOW; FFh = active HIGH
17S05
17128/37LV128         4000hex ->   4003hex  00h = active LOW; FFh = active HIGH
17S05L(XL)
17S10/17S10L(XL)
17256/17S20           8000hex ->   8003hex  00h = active LOW; FFh = active HIGH
17S30
17512/17S40          10000hex -> 10003hex  00h = active LOW; FFh = active HIGH
1701/17S100          20000hex -> 20003hex  00h = active LOW; FFh = active HIGH
17S150/17S50
1702                 40000hex -> 40003hex  00h = active LOW; FFh = active HIGH
1704                 80000hex -> 80003hex  00h = active LOW; FFh = active HIGH
```

Core Device Name is defined as the menu name minus the prefix and/or
postfix information on that name; such as D, E, L, EL(X), and for the
most part L(XL), etc...

NOTE: The following device(s) are the exception to this rule:
17S05L(XL)
<B> 203 <D><R>
This device has a programmable control word, or words, at the end
of the main data array. Refer to the device data sheet for specific
architecture information and locations of any unused bits.

Unused bits are always read from the device as zeros. Setting user
RAM data to anything other than zero for unused bits will not affect
correct programming, but will generate program/verify errors.

Partial device operations are not allowed on this device.
Data files that are loaded into user RAM must include the data for
the control word to avoid errors.
<B> 204 <D><R>
Data in the programmer's User Memory is partitioned as follows:

```
                       68HC705K1
                       ---------

   RAM, UNUSED             -   000 - 1FF hex      fill with 00 hex
   MOR                     -         17 hex       programmable
   USER EPROM              -   200 - 3EF hex      programmable
   TEST ROM, COP           -   3F0 - 3F7 hex      fill with 00 hex
   USER VECTORS            -   3F8 - 3FF hex      programmable
   PEPROM (personality)    -   400 - 47F hex      64 bytes programmable


                       68HC05K1
                       ---------

   RAM, UNUSED             -   000 - 1FF hex      fill with 00 hex
   MOR                     -         17 hex       mask, fill with 00 hex
   USER EPROM              -   200 - 3EF hex      mask, fill with 00h
   TEST ROM, COP           -   3F0 - 3F7 hex      fill with 00 hex
   USER VECTORS            -   3F8 - 3FF hex      mask, fill with 00h
   PEPROM (personality)    -   400 - 47F hex      64 bytes programmable


The PEPROM resides in programmer's User Memory as follows :

 400 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00      row0
 410 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00      row1
 420 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00      row2
 430 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00      row3
 440 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00      row4
 450 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00      row5
 460 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00      row6
 470 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00      row7

      c0 c1 c2 c3 c4 c5 c6 c7
```

The PEPROM map corresponds to the map of the Motorola programmer.
Data for locations marked as xx can be 00 hex or 01 hex. Locations
marked as 00 should be filled with 00 hex.
The checksum is calculated over all 480 hex Memory locations!
<B> 205 <D><R>
Data is programmed into the device in the Least Significant Bit(LSBit) to
Most Significant Bit format (LSBit to MSBit). If you have questions
regarding this format please contact the semi-vendor for details. For
support for programming this device in the Most Significant Bit to Least
Significant Bit format (MSBit to LSBit) please read the associated application
notes for details.
<B> 206 <D><R>
-
<B> 207 <D><R>
Set device block size to C000 hex.
<B> 208 <D><R>
Set device block size to F680 hex.
<B> 209 <D><R>
Set switch position to C on the socket adapter.
<B> 210 <D><R>
-

```
<B>  211  <D><R>
Set device begin address and block size to
8000 hex. Set JP1 on PCA4774G02 to 1M (101).
<B>  212  <D><R>
Set device begin address to 14000 hex and
block size to C000 hex. Set JP1 on PCA4774G02 to 1M (101).
<B>  213  <D><R>
Set device begin address to 18000 hex and
block size to 8000 hex. Set JP1 on PCA4708G02 to 1M (101).
<B>  214  <D><R>
Set device begin address to 14000 hex and
block size to C000 hex. Set JP1 on PCA4708G02 to 1M (101)
<B>  215  <D><R>
Device requires socket adapter PCA4990 (available from the device manufacturer).
<B>  216  <D><R>
The stand-alone VERIFY is not available for this device.  However, a
PROGRAM VERIFY occurs during programming.

A LOAD operation will display the following information without writing
over the data in ram:

      1) ALS DESIGN CHECKSUM -

         Actel's design file checksum (not to be confused with the
         Data I/O ram image checksum) which is generated by the
         design software and programmed into the silicon signature
         field of the device.

      2) SIGNATURE -

         User ID that is defined as part of the design and programmed
         into the silicon signature field of the device.
<B>  217  <D><R>
This algorithm requires a 44 SOIC to 40 DIP adapter. The sources and part
numbers are:

California Integration Technology (916)626-6168 #CIC-44PS-40D-B6-YAM
Emulation Technology (408)982-0660 #AS-44-40-04S-6YAM
<B>  218  <D><R>
The device is erased automatically before programming. Set Erase EE Device
in the PROGRAM options screen to 'N'.
<B>  219  <D><R>
Data bits 6-7 should be set to ones at all address locations.
Refer to the manufacturer's spec sheet for the correct data pattern.
<B>  220  <D><R>
-
<B>  221  <D><R>
-
<B>  222  <D><R>
Set device block size to 6000 hex.
<B>  223  <D><R>
-
<B>  224  <D><R>
-
<B>  225  <D><R>
-
<B>  226  <D><R>
```

-
<B> 227 <D><R>
-
<B> 228 <D><R>
Set device begin address to 6000 hex and block size to 2000 hex.
<B> 229 <D><R>
-
<B> 230 <D><R>
Any of the three security options can be implemented for this device
(Encryption Array data, Security Bit 1 or Security Bit 2). You can
select the security options from the PROGRAM DEVICE Options screen. The
encryption array has data in User Memory. Once any of the security options
have been programmed into the device, no further programming is allowed.

Illegal operations will generate one of these error messages:

A. Encryption Array Already Programmed - A programming operation has
been attempted after the Encryption Array has been programmed.

B. Security Fuse Programmed or Bad Device - A programming operation
has been attempted after security bit 1 has been programmed.

C. Security Fuse Violation - A programming operation has been
attempted after security bit 2 has been programmed. This error will
also be generated for a load or verify operation.

D. Test Fuse Programming Error - This error will be displayed
if there is a programming error in the Encryption Array.

Data in the programmer's User Memory is partitioned as follows:

  MAIN ARRAY DATA   0 through 3FF hex
  ENCRYPTION ARRAY DATA   400 through 40F hex

Enter Encryption Array data by editing the appropriate address in User
Memory.

After the Encryption Array is programmed, device data will no longer
match data in User RAM. Encryption Array data cannot be read from the
device.
<B> 231 <D><R>
This is a high speed device and may require High Speed Logic Drivers
and/or Compensated Vector test enabled during structured testing. Refer to
programmers manual for more information on High speed logic drivers and
Compensated vector test.
<B> 232 <D><R>
-
<B> 233 <D><R>
-
<B> 234 <D><R>
The data to be programmed to the device is offset to 0000h in the
User RAM, which corresponds to the device address 2000h.

Address(in words)	Address(in bytes)	Intel Required Data:
0000h - 0009h	0000h through 0013h	interrupt vectors (lower)
000Ah	0015h and 0014h	FFh, FFh (reserved)

```
         000Bh              0017h   and   0016h    FFh, FFh (also see note #1)
         000Ch              0019h   and   0018h    **h, CCB or CCB0 byte
         000Dh              001Bh   and   001Ah    **h, **h or CCB1 byte
         000Eh              001Dh   and   001Ch    **h, FFh  (reserved)
         000Fh              001Fh   and   001Eh    **h, FFh  (reserved)
  0010h - 0017h             0020h through 002Fh    security key
  0018h - 001Fh             0030h through 003Fh    interrupt vectors (upper)
  0020h - 002Eh             0040h through 005Dh    PTS vectors
  002Fh - 003Fh             005Eh through 007Fh    all FFh (reserved)
```

Locations marked as **h are also reserved locations and it is the
user's responsibility to fill these locations with the required data.
Consult the Manufacturer's specifications for further information.

Note 1: To enable CDE (clock detect enable bit) fill these locations
with 0Ch, DEh. Refer to the device spec. sheet for detailed
information (CDE bit is implemented only on some 196XX family
members).

To secure the device, enable Security bit programming in the Program
Memory Device Options screen. If this feature is enabled, lock bits
of CCB (CCB0) are to be programmed regardless of the value CCB (CCB0)
byte.

User Ram data is shown in words by default. This may be changed to
bytes if needed.

This device does not need to have the Byte Swap Option enabled
(UniSite version 2.5 or later).
<B> 235 <D><R>
Use this algorithm only for version B silicon or higher. When embedding
fuse information in the hex file, it must be stored at address FE00 hex.

To enable a feature, set the appropriate bit in the User's RAM at FE00
hex to '0'. Reserved (resvd) locations are read as '1'.

```
  bit# ... |  9  |  8  ||  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
  ---------|-----|-----||-----|-----|-----|-----|-----|-----|-----|-----|
   fuse ... |  1  |  1  ||resvd|FPMM1|resvd|FPMM0|FWDT1|FWDT0|FOSC1|FOSC0|
```

To secure the device, bit #6 in the User's RAM at FE00 hex must be set
to '0' and the Security bit programming must be enabled in the Program
Memory Device Options screen.
Consult the Manufacturer's specifications for further information.
<B> 236 <D><R>
To secure the device, enable the security fuse from the Program Memory
Device Options screen.

All operations (read, verify, blank check, ...) on a secured device
will cause erasing of the EEPROM and the configuration byte. The
device will not be reusable if the EPROM is not blank.
<B> 237 <D><R>
Data for device is organized into User RAM as follows: Main
Array data, four words of User ID (identification), and a
configuration word.

Device has a 14 bit data word, represented as 16 bit data

for the programmer. The following bits are not used: bits 14 and 15
throughout the Main Array, bits 8-15 in the User ID, and bits 5-15 in
configuration word. All unused bits will be loaded from the device to
User RAM as zeros and are ignored during the verify operation. During
programming, unused bits should be set to zeros.

Enable security bit programming from Program Device menu.

When assembling source file, output as a merged 8 bit Intellec Hex
object file (INHX8M). The object file can then be downloaded to the
programmer by selecting the Intel Intellec 8/MDS translator (code 83).

NOTE: The EEPROM Data Memory Feature is not supported for 16C84
<B> 238 <D><R>
Devices with the E98K mask set should use the menu entry 705P6_E98K.
This algorithm uses 2 pass programming.

Devices with the E20Y mask use a 1 pass programming algorithm.
<B> 239 <D><R>
This device has a clock feature that is accessible from the last 8
bytes of the user RAM array. Refer to the Manufacturer's specification
for details.

To change the clock values:

1. Select the More-Edit-Edit screen

2. Set the most significant bit (the Write bit in the control byte)
to "1".

3. Set the next seven Clock bytes to the desired Seconds, Minutes,
Hour, Day, Date, Month and Year values according to the
Manufacturer's specification.

4. Enable the programming by setting the "Reset Clock" option in the
PROGRAM DEVICE Options screen to "Y".

The value of the clock is updated automatically during each Load operation.
<B> 240 <D><R>
This device has two One Time Protect-able Boot Blocks. Enabling Boot Block
protection locks the Boot Blocks so that Boot Block data CANNOT be
reprogrammed or erased! These Boot Blocks are located at the beginning and
end of the device memory map. Please see device specific data sheet for
details regarding the address range of each Boot Block.

Enable "Program security fuse 1" flag to lock the first Boot Block.
Enable "Program security fuse 2" flag to lock the second Boot Block.
NOTE: Problems may result in attempting to re-program devices which have
      their Boot Blocks locked.
<B> 241 <D><R>
-
<B> 242 <D><R>
This device does not support block limits.
<B> 243 <D><R>
Erase operation erases the entire contents of device.
<B> 244 <D><R>

```
-
<B>  245  <D><R>
Set device begin address to 2000 hex. and device block size to   6000
hex.
<B>  246  <D><R>
-
<B>  247  <D><R>
-
<B>  248  <D><R>
-
<B>  249  <D><R>
This devices memory space is partitioned as follows :

ARRAY             TYPE            ADDRESS
--------------- --------------- ---------------
LOWER DATA      PROGRAMMABLE    0000-1FFF hex
RESERVED        UNPROGRAMMABLE  2000-3FFF hex    fill with FF hex
UPPER DATA      PROGRAMMABLE    4000-5FFF hex
RESERVED        UNPROGRAMMABLE  6000-7FFF hex    fill with FF hex

Lower and upper data arrays have unused bits which must be set to ones.
Data generated from your development tools should support this format
with no manual intervention.
<B>  250  <D><R>
-
<B>  251  <D><R>
-
<B>  252  <D><R>
-
<B>  253  <D><R>
-
<B>  254  <D><R>
-
<B>  255  <D><R>
-
<B>  256  <D><R>
-
<B>  257  <D><R>
-
<B>  258  <D><R>
-
<B>  259  <D><R>
-
<B>  260  <D><R>
-
<B>  261  <D><R>
-
<B>  262  <D><R>
-
<B>  263  <D><R>
Set device block size to 800 hex.
<B>  264  <D><R>
-
<B>  265  <D><R>
-
<B>  266  <D><R>
-
```

<B> 267 <D><R>
-
<B> 268 <D><R>
Some device designs and vectors may result in a Structured Test Error
or Device Overcurrent during vector testing. Disable Vector test to
identify if the failure is due to structure test. Disabling High Speed
Logic Drivers and/or Compensated Vector Test may also eliminate the
Vector failures.

Refer to the sections in your manual which describe the "High Speed
Logic Drivers", "Compensated Vector Test" and "Serial Vector Test"
options. The use of these features can be helpful in identifying the
cause of vector failures and possibly eliminate those failures. For
more information on this subject, refer to application notes #983-0358
and #983-0372 (available from Data I/O Customer Support).
<B> 269 <D><R>
Erasing and locking individuals blocks can be accomplished by modifying
user memory immediately following the device's memory array.

The format of the configuration array is as follows. The offset is
based from the end of device.

        OFFSET   DESCRIPTION
        ----------- -------------------------------
        0 - 3   configuration ID (ID is 12345678 HEX)
        4 - F   reserved
        10   block 0
        11   block 1
        12   block 2
      (etc ... up to the number of blocks in the part)

After confirming the current configuration ID, the algorithm examines the
configuration bytes to determine which blocks are erased and/or locked.

The format of each byte is:

DO   1 = erase, 0 = no erase
D1   1 = lock, 0 = no lock
D2-D7   reserved

If the ID is incorrect, all blocks are erased and none are locked.
<B> 270 <D><R>
-
<B> 271 <D><R>
Programmable Watchdog Timer is not supported
<B> 272 <D><R>
This device is available in a windowed and non-windowed package.
Use of a windowed device on a handler is not recommended.
<B> 273 <D><R>
The following guidelines should be used to assure selection of the correct
algorithm:

1. Distinguish between device markings beginning with "NM" or
"NMC", regardless of other alpha characters that follow the
device name.

2. If necessary, determine device electronic ID by viewing the ID:

"More commands" / "Device checks" / "Compare electronic ID".

3. Select device algorithm from the menu as follows:

```
Device marking   Electronic ID   Select
-------------     -------         --------
NM27C256          8F04            27C256B
NMC27C256         8FC4            27C256
NM27C512          8F85            27C512A
NMC27C512         8F45            27C512
```
<B> 274 <D><R>
EEPROM is not programmed, verified or read.
<B> 275 <D><R>
D3 of the control word must be set to "1". The algorithm will program
this bit even if user RAM data is set to "0", in which case the programmer
will inform the user of an "invalid architecture word". User RAM will not
be altered.
<B> 276 <D><R>
This algorithm programs both EEPROM and EPROM sections.
To keep EEPROM bytes blank, fill corresponding bytes in
the User's RAM with FF hex.
<B> 277 <D><R>
This algorithm programs EPROM sections only.
<B> 278 <D><R>
-
<B> 279 <D><R>
-
<B> 280 <D><R>
-
<B> 281 <D><R>
-
<B> 282 <D><R>
WARNING: If programming a device with a data file generated for use
with the TMDX3270110 socket adapter please note that the data files
generated for use with the TMDX3270110 socket adapter are NOT directly
compatible with the device you have selected. The adapter swaps the
bytes due to an inverter on A0. Execute the Byte-Data swap function
to swap the bytes into the correct format.
<B> 283 <D><R>
-
<B> 284 <D><R>
Any of the two security options can be implemented for this device
(Encryption Array data, Security Bits programming). The security
options can be selected from the PROGRAM DEVICE Options screen.

The Encryption Array data must be entered into User Memory following
the Main Array data. Below is the memory partition information for
the various devices:

```
                              GMS97C52
                              GMS97L52           87c554
                              87C51FA            87c591
            GMS97C51          87C52              87C54
            87C51             87C552             87C51FB
            87C451            87C575             87L51FB
            87C550            87C652             87C654           87C557
            -----------       -----------       -----------      -----------
```

```
MAIN ARRAY    :     0 - 0FFFh      0 - 1FFFh      0 - 3FFFh      0 - FFFFh
ENCRYPT. ARRAY: 1000 - 101Fh   2000 - 201Fh   4000 - 401Fh   10000-1003Fh


                                  GMS99C58
                   GMS97C54       GMS97C58    GMS97C1051     GMS97L2051
                   ----------    -----------   ----------    ------------
MAIN ARRAY    :     0 - 3FFFh      0 - 7FFFh     0 - 3FFh      0 - 7FFh
ENCRYPT. ARRAY: 4000 - 403Fh   8000 - 803Fh    400 - 41Fh    800 - 81Fh


                   GMS97C56
                  ------------
MAIN ARRAY    :     0 - 5FFFh
ENCRYPT ARRAY :  6000 - 603Fh
```

<B> 285 <D><R>
Prior to performing a Program option, transfer your design file using
format 17 (LOF format). The design file *.LOF file needs to be
zipped using PKZIP v1.1 prior to transferring. The programming
algorithm has embedded verification of the pattern.
<B> 286 <D><R>
This algorithm allows the XC1736D device to be programmed as an
XC1736A. The algorithm will automatically program the RESET
polarity to be active HIGH and will generate checksums that match
those of the XC1736A.

This algorithm WILL NOT program the XC1736A device and WILL NOT
program the RESET polarity of the XC1736D to be active low. To
program the XC1736A, select the 1736A algorithm from the standard
Xilinx device selection menu. To support the programmable RESET
polarity feature of the XC1736D, select the XC1736D algorithm from
the standard Xilinx device selection menu.
<B> 287 <D><R>
This algorithm may not work with devices marked with date codes
earlier than 1994. If you are encountering problems with devices
manufactured before 1994, contact the semiconductor manufacturer.
<B> 288 <D><R>
This algorithm may not work with devices marked with date codes
earlier than 1994. If you are encountering problems with devices
manufactured before 1994, contact your local Data I/O office about
purchasing a PPI-5201 programming adapter.

<B> 289 <D><R>
-
<B> 290 <D><R>
This programmer supports this devices' EPROM protect, RAM protect and RC
oscillator select programming modes, via three security options,
available from the PROGRAM options screen.

To enable these features:

1. To enable the device's EPROM protect, enable security fuse 1 in the
PROGRAM options screen. In this case some load instructions will be
disabled.

2. To enable the device's RAM protect, enable security fuse 2 in the
PROGRAM options screen.

3. To enable the device's RC oscillator, enable security fuse 3 in the PROGRAM options screen.

4. Execute a program operation.
<B> 291 <D><R>
-
<B> 292 <D><R>
To keep EEPROM locations unprogrammed (blank), be sure that the corresponding bytes in programmer's user RAM are filled with FF hex.
<B> 293 <D><R>
To secure the device, change the SEC bit in OPTR to '0'. The part will be secured after programming.
<B> 294 <D><R>
-
<B> 295 <D><R>
-
<B> 296 <D><R>
-
<B> 297 <D><R>
-
<B> 298 <D><R>
-
<B> 299 <D><R>
-
<B> 300 <D><R>
This device has two security bits which are set automatically by the data file. The first security bit is at location 0x021022 in the ACR. The second security bit is at location 0x021023 in the ACR. The security bit is data line D0, for both locations.

For a non-secured device, D0 of location 0x021022 must be set to logic 1 in the data file, and D0 of location 0x021023 must be set to logic 0 in the data file. To secure the device, D0 of location 0x021022 must be set to logic 0 in the data file, and D0 of location 0x021023 must be set to logic 1 in the data file.
<B> 301 <D><R>
The device you have selected, communicates with the programmer through a special cable. Please contact the device manufacture for more information on the cable/adapter.
<B> 302 <D><R>
This device requires an AutoSite with 88 pin drivers.
<B> 303 <D><R>
Select part name 705C5-E40A if the mask set is 2E40A or newer.
Select part name 705C5-D68C if the mask set is 0D68C or older.
<B> 304 <D><R>
(2900 and 3900 only) To insert the socket adapter, push down on the ZIF
 socket handle.
<B> 305 <D><R>
-
<B> 306 <D><R>
The 68HC705J2 is programmed as a 705J1 (emulation mode). To enable this mode, set the J1 in MOR (in the programmer's RAM at address 0700 hex).
<B> 307 <D><R>
-
<B> 308 <D><R>
-

```
<B>  309  <D><R>
The available program area is "4000 hex - FFFF hex".
The data in all other areas should be set to "FF".


Device address             data
-------------------        ---------
 0000 -  3FFF hex          all FF
 4000 -  FFFF hex          user data
10000 - 1FFFF hex          all FF


This adapter has 2 jumper switches. Set JP1="FLASH" and JP2="1M".
<B>  310  <D><R>
The available program area is "8000 hex - FFFF hex".
The data in all other areas should be set to "FF".


  Device address            data
--------------------       ----------
 0000 -  7FFF hex          all FF
 8000 -  FFFF hex          user data
10000 - 1FFFF hex          all FF


This adapter has 2 jumper switches. Set JP1="FLASH" and JP2="1M".
<B>  311  <D><R>
-
<B>  312  <D><R>
-
<B>  313  <D><R>
-
<B>  314  <D><R>
Programming of protect register is not supported for this device.
<B>  315  <D><R>
Set the I/O translation format for this device to 99(Intel HEX-32). This
step is necessary when downloading or uploading files from disk.
<B>  316  <D><R>
To ensure proper downloading of your design file, set the following download
options:


I/O Translation Format   88
I/O address offset         0
Memory begin address       0
User data size             0


To ensure that consistent checksums are reported, perform a
"Fill Ram" operation with FF data prior to downloading your
design file and before performing a LOAD operation.
<B>  317  <D><R>
-
<B>  318  <D><R>
-
<B>  319  <D><R>
Use the following configuration blocks to properly configure the
TestSite for this device(This only applies to UniFam handlers):
     X1 = Configuration block 'B'
     X2 = Configuration block 'C'
     X3 = Configuration block 'B'
     X4 = Configuration block 'A'
<B>  320  <D><R>
```

-
<B> 321 <D><R>
-
<B> 322 <D><R>
-
<B> 323 <D><R>
The JEDEC file for this device may contain E field fuses that are not
yet supported by Hiterm's, High Speed Download mode. Please disable
the High Speed Download option if using either Hiterm or the
HyperTerminal Interface. This feature can be disabled via the
Communications configuration screen. If you choose to leave the High
Speed Download mode enabled while in the Terminal Interface, all E
and U fuses in your data file will be discarded.
<B> 324 <D><R>
This algorithm requires a 56 pin TSOP to 48 pin DIP adapter.
The manufacturers, part numbers, and phone numbers are:

Emulation Technologies
#AS-56-48-02TS-6YAM-S
(408) 982-0660

California Integration Coordinators
#CIC-56TS-48D-B6-YAM-S
(916) 626-6168
<B> 325 <D><R>
This algorithm requires a 56 pin TSOP to 40 pin DIP adapter, The
manufacturers, part numbers, and phone numbers are:

Emulation Technologies
#AS-56-40-05TS-6YAM-S
(408) 982-0660

California Integration Coordinators
#CIC-56TS-40D-E6-YAM-S
(916) 626-6168
<B> 326 <D><R>
Pin 1 of the device must be placed in the upper left corner of the socket.
<B> 327 <D><R>
-
<B> 328 <D><R>
Bit #7 (SECE) in the OPTION register (address 1EFE hex.) must be set to '0'.
The security feature is not fully implemented yet.
<B> 329 <D><R>
This device contains an Electronic ID. If an ID error occurs, the wrong
device is selected or a different version of device is selected.

If all menu entries yield a "DEVICE ID error" contact DATA I/O Customer
Support for assistance.
<B> 330 <D><R>
A standard 7128 POF file can be programmed by the following menu
entries: "7128" or Altera X-PGM menu entry "7128E AS 7128" or
"7128S AS 7128. 7128E POF files can only be programmed with the
"7128E" or "7128S AS 7128E" entry. 7128S POF files can only be
programmed with a "7128S" entry.
<B> 331 <D><R>
Data bits 5 through 7 are not used in this device. All addresses
should have these bits set to one, or a Verify error will occur.

Programming is unaffected. A load operation will load these bits
as ones.
<B> 332 <D><R>
 Data in Programmer's User RAM is partitioned as follow:

                003F hex   config. register (EEPROM cell)
     0D00 hex - 0FFF hex   EEPROM
     4000 hex - FFFF hex   EPROM   (not on 68HC11PH8)
<B> 333 <D><R>
A standard 7192 POF file can be programmed by the following menu
entries: 7192 or Altera X-PGM entries "7192E as 7192" or "7192S as 7192".
7192E POF files can be programmed with "7192E" or "7192S as 7192E".
7192S POF files can only be programmed with a 7192S entry.

<B> 334 <D><R>
-
<B> 335 <D><R>
Pin 1 of the device must be placed in the lower right corner of the socket.
<B> 336 <D><R>
-
<B> 337 <D><R>
Encryption array, lock bit, and configuration byte programming are all
supported on this device. These features can be enabled from the Program
Device screen. The encryption array and configuration bytes have data in
User Memory.

                              87C251SB

   MAIN ARRAY DATA   0-3FFF hex
   ENCRYPTION ARRAY DATA   4000-407F hex
   CONFIGURATION BYTES   4080-4083 hex

Note that these values are all offsets from the memory begin address
field located in the PROGRAM DEVICE options screen. If the memory
begin address is not zero (default) , add the value in this field to the
offset for the appropriate address. Also note that to program special
features, enter data at the appropriate memory locations, and set
the corresponding field in the PROGRAM DEVICE options screen to "Y."
Enabling the security fuses programs the lock bits, "Program XNOR data"
programs the encryption array, and "Program Configuration" programs the
configuration bytes.

After the Encryption Array is programmed, device data will no longer
match data in User RAM. After programming security bits, programming
operations are no longer allowed.
<B> 338 <D><R>
This device requires a special ICD 6233 DIP adapter. Please contact Cypress.
<B> 339 <D><R>
-
<B> 340 <D><R>
The available program area is "0000hex - EE7Fhex". The data in all other
areas should be set to "FF".

        Device address   data
        -------------------   -----------
        0000hex - EE7Fhex   user data

```
      EE80hex - 1FFFFhex    all FF
      ------------------   -----------
<B>  341  <D><R>
-
<B>  342  <D><R>
Performing a LOAD operation may result in the following message:
"Load Error:  Unable to encode device state into POF."
This indicates that the data loaded into the programmer's RAM
is not representable in the POF format.  An example of this
occurs when loading a blank device.
<B>  343  <D><R>
A standard 7160 POF file can be programmed by the following
entries: 7160, or Altera X-PGM menu entries "7160E as 7160"
or "7160S as 7160". 7160E POF files can only be programmed
with "7160E" or "7160S as 7160E".  7160S POF files can only
be programmed with the 7160E menu entry.
<B>  344  <D><R>
A standard 7256 POF file can be programmed by the following menu
entries: 7256, 7256-NEW or Altera X-PGM menu entries "7256E as 7256"
or "7256S as 7256".  7256E POF files can be programmed with "7256E"
or "7256S as 7256E".  7256S or 7256A POF files can only be programmed
with a 7256S or 7256A entry.
<B>  345  <D><R>
-
<B>  346  <D><R>
OPTION BYTE: The Option byte(s) are at the end of the
device memory map.  Please refer to the device data
sheet for number of option bytes, and what each option
bit represents. Enable programming by Selecting "Program
configuration" in the "Program device" screen.

In TaskLink: Make the following selections: Setup menu ->
General Parameters, then select the "ENABLE SPECIAL DATA.",
and set the Security Option to 2 enabling all security fuses.
<B>  347  <D><R>
-
<B>  348  <D><R>
-
<B>  349  <D><R>
-
<B>  350  <D><R>
-
<B>  351  <D><R>
-
<B>  352  <D><R>
For more information, the following application notes(or files) can be
downloaded from the Data I/O Web Site(FTP site.) These files are also
located on your UniFam Software Update CD:

      atmel_uc.txt ---- for Atmel microcontrollers
      atm_avr.txt  ---- for Atmel AVR microcontrollers
      awm_uc.txt   ---- for Atmel Wireless Microcontrollers
      fuj_uc.txt   ---- for Fujitsu microcontrollers
      hit_uc.txt   ---- for Hitachi microcontrollers
      int_uc.txt   ---- for Intel microcontrollers
      mct_uc.txt   ---- for Microchip microcontrollers
      mot_uc.txt   ---- for Motorola microcontrollers
```

```
     nat_uc.txt   ---- for National microcontrollers
     nec_uc.txt   ---- for NEC microcontrollers
     phl_uc.txt   ---- for Philips microcontrollers
     rtc_uc.txt   ---- for Renesas microcontrollers
     siem_uc.txt  ---- for Siemens/Infineon microcontrollers
     stm_uc.txt   ---- for STMicroelectronics microcontrollers
     tex_uc.txt   ---- for Texas Inst. microcontrollers
     tos_uc.txt   ---- for Toshiba microcontrollers
     win_uc.txt   ---- for Winbond microcontrollers
     zil_uc.txt   ---- for Zilog microcontrollers
```

These files will be updated periodically. To download the latest files
go to the following internet site:
ftp://ftp.dataio.com/appnotes/
<B> 353 <D><R>
The security enabled/disabled setting must be included in your data file.
Check location 07F1 hex (MOR register) in the Programmer's User RAM for
the security feature enabled/disabled. If bit #6 is set to '1', the part
will be secured. The secured part reads all locations as 00 hex (as if
it were a blank device).

<B> 354 <D><R>
This device has a security function that, once programmed, all data reads
from the device as '00'. This security fuse function can be enabled
from the Program Device screen.

Users are cautioned that the manufacturer does not guarantee this function.
Concerns about this should be addressed to Hitachi, Ltd.
<B> 355 <D><R>
This device requires a socket adapter available from
Emulation Technology Inc. (408-982-0660).

ISP/PLSI1016*   44 pin PLCC   AS-44-28-02P or
                                AS-44-28-03P
                44 pin TQFP   AS-44-28-01Q
ISP/PLSI1024*   68 pin PLCC   AS-68-28-03P
ISP/PLSI1032*   84 pin PLCC   AS-84-28-02P
                84 pin PGA   AS-84-28-01PG6
                100 pin TQFP   AS-100-28-01Q
ISP/PLSI1048*   120 pin PQFP   AS-120-28-01Q
ISP/PLSI1048C* 128 pin PQFP   AS-128-28-01Q
                133 pin PGA   AS-133-28-01G
ISP/PLSI1016E* 44 pin PLCC   AS-44-28-03P
                44 pin TQFP   AS-44-28-01Q
ISP/PLSI1024E* 68 pin PLCC   AS-68-28-03P
ISP/PLSI1032E* 84 pin PLCC   AS-84-28-02P
                100 pin PGA   AS-100-28-01Q
        100 pin TQFP   AS-100-28-01Q
ISP/PLSI1048E* 128 pin PQFP   AS-128-28-01Q
                133 pin PGA   AS-133-28-01G
ISP/PLSI2032*   44 pin PLCC   AS-44-28-03P
                44 pin TQFP   AS-44-28-01Q
ISP/PLSI2032LV* 44 pin PLCC   AS-44-28-03P
                44 pin TQFP   AS-44-28-01Q
ISP/PLSI2064*   84 pin PLCC   AS-84-28-02P
                100 pin TQFP   AS-100-28-01Q
```

```
ISP/PLSI2096*    128 pin PQFP     AS-128-28-01Q
                 133 pin PGA      AS-133-28-01G
ISP/PLSI2128*    160 pin MQUAD    AS-160-28-01Q
                 176 pin TQFP     AS-176-28-01Q
                 167 pin PGA      AS-167-28-01G
ISP/PLSI3160*    208 pin MQUAD    AS-208-28-04MQ-6
ISP/PLSI3192*    240 pin PQFP     AS-240-28-01Q
ISP/PLSI3256*    160 pin MQUAD    AS-160-28-01Q
                 167 pin PGA      AS-167-28-01G
ISP/PLSI3256A*   160 pin MQUAD    AS-160-28-01Q
                 167 pin PGA      AS-167-28-01G
ISP/PLSI3256E*   304 pin MQUAD    AS-304-28-01Q-6
ISP/PLSI3320*    208 pin MQUAD    AS-208-28-04MQ-6
ISP/PLSI3448*    304 pin MQUAD    AS-304-28-01Q
ISP/PLSI6192*    208 pin MQUAD    AS-208-28-02MQ
I/P2128V-84P*    84  pin PQFP     AS-84-28-05P-6
I/P2128V-100T*   100 pin TQFP     AS-100-28-04Q-6
I/P2128V-176T*   176 pin TQFP     AS-176-28-02Q-6
ISPGDX160*  208 pin MQUAD    AS-208-28-05Q
ISPGDX120*  176 pin TQFP     AS-176-28-03Q
<B>  356  <D><R>
```
The starting address for this device has been offset to 0000 hex in
User RAM. This corresponds to the device address FF2000h.

```
Address(in words)    Address.(in bytes)    Intel Required Data:
---------------      ----------------      ----------------------
 0000h - 0009h     0000h through 0013h     interrupt vectors (lower)
        000Ah     0015h    and    0014h    FFh, FFh (reserved)
        000Bh     0017h    and    0016h    FFh, FFh (also see note #1)
        000Ch     0019h    and    0018h    **h, CCB or CCB0 byte
        000Dh     001Bh    and    001Ah    **h, **h or CCB1 byte
        000Eh     001Dh    and    001Ch    **h, FFh  (reserved)
        000Fh     001Fh    and    001Eh    **h, FFh  (reserved)
 0010h - 0017h     0020h through 002Fh     security key
 0018h - 001Fh     0030h through 003Fh     interrupt vectors (upper)
 0020h - 002Eh     0040h through 005Dh     PTS vectors
 002Fh - 003Fh     005Eh through 007Fh     all FFh (reserved)
```

Locations marked as **h are also reserved locations and it is the
user's responsibility to fill these locations with the required data.
Consult the Manufacturer's specifications for further information.

Note 1: To enable CDE (clock detect enable bit), fill these locations
with 0Ch, DEh. Refer to the device spec. sheet for detailed
information (CDE bit is implemented only on some 196XX family
members).

To secure the device, enable Security bit programming in
the Program Memory Device Options screen. If this feature is enabled,
lock bits of CCB (CCB0) are to be programmed regardless of value
CCB (CCB0) byte.

User Ram is shown in words as default. Byte display mode is also
available.

This device does not need to have the Byte Swap Option enabled.
```
<B>  357  <D><R>
```

```
-
<B>  358  <D><R>
Data in Programmer's User Ram are partitioned as follow:

   Main array in User's RAM          Main array in the device
   ---------------------------       ----------------------------
   0000 hex - 5FFF hex (in words)    0000 hex - BFFF hex (in bytes)


   Shadow registers in User's RAM    Shadow registers in the device
          (in words)                          (in bytes)
   ----------------------------       -------------------------------
         6000 hex - 600F                 F820 hex - F83E hex
<B>  359  <D><R>
-
<B>  360  <D><R>
-
<B>  361  <D><R>
-
<B>  362  <D><R>
If you are using a JEDEC file designed for the 44-pin PLCC package, you
will need to use the JEDEC pin swap function "P" for the test vectors
to run successfully.  The JEDEC file should be modified by inserting
3 lines after the last fuse number and before the first vector:

Example:

L07424 11110111111111101111111111111111111111111111111111*
L07476 00000000000000000000000000000000000000000000000000*
L07528 00000000000000000000000000000000000000000000000000*
E 11111111111111101111111111111000* <-- last fuse number in JEDEC file
P 39 40 41 42 43 44 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
   17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
   36 37 38*
V0001 NLLL0001XXXN0XXXXXXXXXNNXXXXXXXXXXXNXXXXXXXXLN* <-- 1st vector

                               in JEDEC file
<B>  363  <D><R>
If you are using a JEDEC file designed for the 44-pin PLCC package, you
will need to use the JEDEC pin swap function "P" for the test vectors
to run successfully.  The JEDEC file should be modified by inserting
3 lines after the last fuse number and before the first vector:

Example:

L12800 00000000000000110000000000000011*    <-- last fuse number

    in JEDEC file
P 39 40 41 42 43 44 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
   17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
   36 37 38*
V0001 XLLXXXXXXXXCXXXXXXXXXXXXXXXXXXXXXXXX1XXXXXXX* <-- 1st vector

                               in JEDEC file
<B>  364  <D><R>
This device can be programmed either in a carrier pre
lead formed (PPI-0521) or post lead formed (PPI-0546).
```

Please be prepared to supply sample lead formed parts when
ordering a PPI-0546.
<B> 365 <D><R>
-
<B> 366 <D><R>
-
<B> 367 <D><R>
The available program area is "000h-3FFh". In normal operation,
switch SW1 should be set to "N".

To secure the device, use the following steps:
     1) Adapter's SW1 is set to "S" side.
     2) Go through MAIN MENU-More-Device checks-Electronic erase.
     3) Operate Electronic erase.
     4) "Non-Blank" error occurs but security operation is complete.

*Note: If the device is reprogrammed it returns to an unsecured state.

<B> 368 <D><R>
-
<B> 369 <D><R>
-
<B> 370 <D><R>
-
<B> 371 <D><R>
Select the device with extension -0F88 if using 68HC705X4 mask 0F88B.
Select the device with extension -1F88 if using 68HC705X4 mask 1F88B.
<B> 372 <D><R>
This device allows individual partitions to be protected. The
following procedure describes how to secure any of the sixteen
partitions:

1)
 Set protection byte value in corresponding at User Ram address,
 which is described as: "Device Size(DS) + Protection Byte Address".
 The protect or unprotect data values are either set to 01 for
 protected, or set to 00 for unprotected.

 Partition   User Ram address   Protect Data   Unprotect Data
 ---------   ----------------   ------------   --------------

    0   DS + 00   01   00
    1   DS + 01   01   00
    2   DS + 02   01   00

    ...and so on up to...

   15   DS + 15   01   00

 Note: These protection bytes are not part of the Main memory array
 of the device; but they are part of the total device size. This
 allows the algorithm access to this protection data. This also
 means that the protection status will be part of the device checksum.

2)
 Enable the security fuse option on the PROGRAM DEVICE options screen

during program operation, this enables the protection programming
option.

Corresponding Device Sizes(DS):
DS1630AB/Y = 8000 hex
DS1645AB/Y = 20000 hex
DS1650AB/Y = 80000 hex
<B>   373   <D><R>
-
<B>   374   <D><R>
-
<B>   375   <D><R>
-
<B>   376   <D><R>
-
<B>   377   <D><R>
Device has Reset/OE# pin configuration data which follows Main
Array Data in User Memory. The four configuration bytes at this
location must be set as follows -

                         Address
 Device   Location   Data

 17C65/17LV65   2000-2003   00h for reset LOW
                                        FFh for reset HIGH

 17C128/17LV128   4000-4003   00h for reset LOW
                                        FFh for reset HIGH

 17C256/17LV256/17N256   8000-8003   00h for reset LOW
                                        FFh for reset HIGH

 17C512/17LV512/17N512   10000-10003   FFh for reset LOW
                                        00h for reset HIGH

 17C010/17LV010/   20000-20003   FFh for reset LOW
 3LV010/17N010   00h for reset HIGH

 17C020/17LV020   40000-40003   FFh for reset LOW
                                        00h for reset HIGH

 17C002/17LV002/17N002   40000-40003   FFh for reset LOW
                                        00h for reset HIGH

 17LV040/17N040   80000-80003   FFh for reset LOW
                                        00h for reset HIGH
<B>   378   <D><R>
-
<B>   379   <D><R>
Socket adapter has no 1 pin indicator.
For device insertion, refer to adapter users manual.
The available program area is "0000hex - 7FFFhex". The data in all
other areas should be set to "FF".

Device address   Data
--------------------   -----------------
 0000hex - 7FFFhex   User data

```
   8000hex - 1FFFFhex        all    FF
 --------------------        -----------------
<B>  380  <D><R>
The available program area is "0000hex - 7FFFhex".
The data in other areas should be set to "FF".


Device address            Data
 --------------------        -----------------
0000hex -   7FFFhex      User  data
8000hex -  1FFFFhex      all "FF"
 --------------------        --------------------
<B>  381  <D><R>
-
<B>  382  <D><R>
-
<B>  383  <D><R>
This device selection should only be used with the 'A' version devices.

The version information can be deciphered from the part name.
                    Ex. TMC371C7B3ANMT
                                  ^
                                  |
              An 'A' at this position means denotes an 'A' version device



Contact your local TI representative if you need assistance.
<B>  384  <D><R>
The device selection menu option containing the '-F' suffix has been
optimized for performance. If you experience yield problems please
use the non '-F' device menu selection.
<B>  385  <D><R>
-
<B>  386  <D><R>
-
<B>  387  <D><R>
Data for this device is organized in User RAM as follows: Main
Array data, four words of User ID (identification, 2000-2003 Hex)
and a configuration word (2007 Hex).

This device has a 14 bit data word which is represented as 16 bit data
for the programmer.

Bits 4 and 5 of the configuration word are the security fuses.
The options are as follows:


                00     All memory is code protected.
                01     Upper 3/4 of program memory code protected.
                10     Upper 1/2 of program memory code protected.
                11     Code protection off.


On devices that use configuration bits 8-13, they are set by the
algorithm according to what bits 4 and 5 are set to by the user.

The Security Bit can be programmed only by enabling security fuse
feature in Program Device Menu.

When assembling source file, output to a merged 8 bit Intellec Hex
```

object file (INHX8M). The object file that was created can then be
downloaded to the programmer by selecting the Intel Intellec 8/MDS
translator (code 83).
<B> 388 <D><R>
If the PPI adapter called out for this support does NOT have 3 capacitors
installed(see bottom side of adapter,) then you will need to purchase an
updated version of this adapter to program this device. Please contact
your local DATA I/O representative, or technical support group for further
assistance(support@dataio.com.)
<B> 389 <D><R>
-
<B> 390 <D><R>
-
<B> 391 <D><R>
-
<B> 392 <D><R>
-
<B> 393 <D><R>
-
<B> 394 <D><R>
If using a JEDEC file designed for the 44-pin PLCC package, use the
JEDEC pin swap function "P" to translate the test vector data.
The JEDEC file should be modified by inserting 3 lines after the last
fuse number but before the first vector:

Example:

L15040 11101010111101011111101011111101*
E0000000100100011
0100010101100111
1000100110101011
1100110111101111* <-- last fuse number in JEDEC file
P 39 40 41 42 43 44 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
   17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
   36 37 38*
V0001 N0111010000N000101110NNLLLLLLLLL10N000101110N* <-- 1st vector
                                   in JEDEC file
<B> 395 <D><R>
-
<B> 396 <D><R>
-
<B> 397 <D><R>
The Encryption Array is partitioned at 4000h-403Fh in the programmer's
User Memory.

Enable the Watchdog Time Setting by setting the 'Program configuration'
to 'Y'.

After the Encryption Array is programmed, device data will no longer
match data in User RAM. Encryption Array and Watchdog Timer data cannot
be read from the device.
<B> 398 <D><R>
Enable 2 pass verify when programming this device to comply with the
manufacturers' requirements.
<B> 399 <D><R>
It is important to execute another device operation prior to executing a
vector test only, so that the ID is initialized.

```
<B>   400   <D><R>
-
<B>   401   <D><R>
-
<B>   402   <D><R>
This device requires that capacitor block 44C be installed
on the test-site at position X4.
<B>   403   <D><R>
Use the following configuration blocks to properly configure the
test-site for this device:

     X1 = Configuration block '44B'
     X2 = No Configuration block
     X3 = Configuration block '44B'
     X4 = Configuration block '44A'


<B>   404   <D><R>
-
<B>   405   <D><R>
-
<B>   406   <D><R>
-
<B>   407   <D><R>
Structured Test Vector errors may occur with this hardware
configuration.  This may also be seen as a Device over-current
fault that occurs during the vector testing operation. Please
disable vector testing to avoid errors.
<B>   408   <D><R>
-
<B>   409   <D><R>
Encryption array, lock bit, and configuration byte programming are all
supported on this device. Set lock bit (a.k.a. security bit) data from either
the PROGRAM DEVICE options screen, or from the More Commands -> Edit Data ->
Edit Memory tool and editing the proper data bits. The proper data bytes and
bits to edit for the device features are outlined in the following table:


                              87C151SB
                              87C251SB(B/C)
                              ---------
  MAIN ARRAY DATA             0-3FFF hex
  ENCRYPTION ARRAY DATA       4000-407F hex
  SECURITY BIT1 DATA          4080 hex (bit 0)
  SECURITY BIT2 DATA          4080 hex (bit 1)
  SECURITY BIT3 DATA          4080 hex (bit 2)
  CONFIGURATION BYTES         FFF8-FFFF hex


Note that the values for ENCRYPTION and SECURITY are all offsets
from the memory begin address field located in the PROGRAM DEVICE
options screen. If the memory begin address is not zero (default),
add the value in this field to the offset for the appropriate
address. The value for configuration bytes is an absolute address.
Also note that to program special features, enter data at the
appropriate memory locations, and set the corresponding field in
the PROGRAM DEVICE options screen to "Y."  Setting the "Program
security bits" field  programs all lock bits, "Program XNOR data"
programs the encryption array, and "Program Configuration"
```

programs the configuration bytes.

The LOAD DEVICE operation will read the configuration bytes,
overwriting any data in locations FFF8-FFFF hex. To verify or
program these locations, the 'Program configuration' flag must
be set on the PROGRAM DEVICE screen. This flag affects both the
VERIFY DEVICE and PROGRAM DEVICE operations.

After the Encryption Array is programmed, device data will no
longer match data in User RAM. After programming security bits,
programming operations are no longer allowed.

This algorithm is for the B and C step versions of the 87C251SB.
The 'A' stepping is noted by a 'S-SPEC' number (the number
after the part number on the symbol) of 'Q7945'. 'B' and 'C'
step versions will have an spec of 'Q8052' or greater. The
'A' step will not program correctly if this algorithm is used.
This algorithm is also used for the 87C151SB.
<B> 410 <D><R>
-
<B> 411 <D><R>
The Write Protect Register is programmed with the address value of
the first word that is to be protected. All address values equal
to or greater than the value contained in the Protect Register will
be protected from further writes. The value of the Protect Register
can be specified by editing the User RAM location listed in the table
below:

         DEVICE   RAM Location   Maximum Value
         --------   ------------   -------------
         93CS06   20 hex   001F hex
         93CS46   40 hex   003F hex
         93CS47   40 hex   003F hex
         93CS56   80 hex   007F hex
         93CS57   80 hex   007F hex
         93LCS56   80 hex   007F hex
         93CS66   100 hex   00FF hex
         93CS67   100 hex   00FF hex
         93LCS66   100 hex   00FF hex

The contents of the Protect Register will not be programmed
unless the Program Protect Reg. option is set to "Y".

The content of the Protect Register may be secured from any
future writes by setting the Program Security Fuse option
to "Y".
<B> 412 <D><R>
This algorithm is for the 'A' step version of the 87C251SB.

The step is noted by an 'S-SPEC' number which is located
after the part number.

Step Version   S-SPEC
 A   Q7945
 B or C   Q8052' or greater.

The 'B' or 'C' step devices will not program correctly if this

algorithm is used. Select the 87C251SB-BC or 87C251SB-BC-PLC
device menu selection.
<B> 413 <D><R>
-
<B> 414 <D><R>
-
<B> 415 <D><R>
The algorithm programs data from the user's RAM address 0000h - DFFFh
to the device's bank #8. Data from user's RAM address E000h - EFFFh are
programmed to the device's shadow bank.

<B> 416 <D><R>
-
<B> 417 <D><R>
If you are using a JEDEC file designed for the 68-pin PLCC package, you
will need to use the JEDEC pin swap function "P" for the test vectors
to run successfully or disable Vector test. The JEDEC file should be
modified by inserting 4 lines after the last fuse number and before the
first vector:

Example:

L07424 11110111111111101111111111111111111111111111111111111*
L07476 00000000000000000000000000000000000000000000000000000*
L07528 00000000000000000000000000000000000000000000000000000*
E 111111111111111101111111111111000* <-- last fuse number in JEDEC file
P 9 7 5 3 1 67 65 63 61 10 11 8 6 4 2 68 66 64 62 60 12 13
   59 58 14 15 57 56 16 17 55 54 18 19 53 52 20 21 51 50 22
   23 49 48 24 25 47 46 26 28 30 32 34 36 38 40 42 45 44 27
   29 31 33 35 37 39 41 43*
V0001 NLLL0001XXXN0XXXXXXXXNNXXXXXXXXXXNXXXXXXXXLN* <-- 1st vector

                              in JEDEC file
<B> 418 <D><R>
-
<B> 419 <D><R>
-
<B> 420 <D><R>
-
<B> 421 <D><R>
Available program area is "1000 hex - FFFF hex".
Data in all other areas should be set to "FF".

Device address   data
--------------------   ----------------
 0000 -   FFF hex   all FF
 1000 - FFFF hex   user data

Adapter has 2 jumper switches. Set JP1="EPROM" and JP2="1M".
<B> 422 <D><R>
-
<B> 423 <D><R>
The device program memory areas in the PROM mode are as follows:

     0000 hex - 3FFF hex   unused in 87PH20F, programmable in 87PM20F
     4000 hex - 7FFF hex   programmable in 87PH20F and 87PM20F

For 87PH20F set User data size to 4000, Memory begin address to 4000,
Device begin address to 4000, and Device block size to 4000.

For 87PM20F set User data size to 8000, Memory begin address to 0000,
Device begin address to 0000, and Device block size to 8000.
<B> 424 <D><R>
When using UniSite with SITE48HS, the adapter's leads should be extended
more than 10mm to reach the DIP contacts.
<B> 425 <D><R>
Device requires a socket adapter. Two types can be used:
   1. Hitachi HS7043ESH S1H (available from the device manufacturer).
   2. Data I/O H7704XQ144D3201 (available from Data I/O).

For UniSite (SITE48HS DIP module), the leads of Hitachi
adapter should be extended by 10mm to reach DIP contact.
<B> 426 <D><R>
Security Bit programming may be enabled in the Program Memory Device Options
screen.

Program security fuse 1 -> enables DED bit programming
Program security fuse 2 -> enables DEI bit programming
Program security fuse 3 -> enables LOC0/LOC1 programming

The device's memory map starting at address 2000 hex is offset by 2000
hex bytes to start at the User Memory address 0000 hex. Because of
differences in assemblers, fill first 10000 hex bytes in User Ram with
FF hex before file downloading. Partial device operation is
not allowed.

Locations B, D-F and 2F-3F hex are reserved for special functions and
are not programmable. These locations will always load as FFFF hex.
If data is entered in User RAM at these locations, a verify error
occurs, but no data will be programmed at those locations.

Address C hex is also reserved. The most significant byte of C hex is
always programmed to 20 hex. If data other than 20 hex is entered in
User RAM at this location, a verify error occurs, but data 20 hex will
be programmed.

The least significant byte of address C hex is the Chip Configuration
byte, which is programmable. The two most significant bits of this
location are the lock bits, which can be programmed only by selecting
the Security Fuse 3 programming option in the PROGRAM Options screen.
Consult the Manufacturer's specifications for further information.

The User Ram is displayed in words by default. Byte display mode is
also available.
<B> 427 <D><R>
Data for the individual block locking is stored, starting
with block 0, at the end of device memory. A byte of data
is reserved for each block. The LSB of the byte equal to
one (01h) means that the block lock should be programmed.
Data of zero (00h) means that the block lock will not be
set. All bits other than bit zero are ignored. To enable
block locking, the 'Program Configuration' option in the
'Program Device' screen must be set to 'Y'.

The master lock bit can be set by enabling the 'Program
Security Fuse 1' option in the 'Program Device' screen.
<B> 428 <D><R>
If experiencing yield problems, contact Data I/O for a specially
configured cap block.
<B> 429 <D><R>
-
<B> 430 <D><R>
For assistance with sector protection operation please contact
your local DATA I/O representative.
<B> 431 <D><R>
-
<B> 432 <D><R>
-
<B> 433 <D><R>
Use the following configuration blocks to properly configure the
test-site for this device:
     X1 = Configuration block 'C'
     X2 = Configuration block 'B'
     X3 = Configuration block 'C'
     X4 = Configuration block 'B'
<B> 434 <D><R>
-
<B> 435 <D><R>
Locking individuals blocks can be accomplished by modifying
user memory. The configuration array is located directly after the
devices normal memory array. If the device size is 200,000 hex bytes long,
the configuration memory begins at address 200,000 hex.

The format of the configuration array is as follows. The offset is
based from the end of device.

       OFFSET   DESCRIPTION
       ----------- -------------------------------
       0   block 0
       1   block 1
       2   block 2
     (etc ... up to the number of blocks in the part)

     DO   1 = lock, 0 = no lock
     D1-D7   reserved

To enable block locking, the 'Program configuration' flag
in the 'Program Device' menu must be set to 'Y' (Yes). If
the 'Program configuration' flag is set to 'N', block locking
information is ignored.
<B> 436 <D><R>
This device requires that the security fuse be blown in order
for the device to function properly. Before programming the
device, be sure you have made the proper selection to program
the security fuse.
<B> 437 <D><R>
Pin 16
<B> 438 <D><R>
-
<B> 439 <D><R>
-

```
<B>  440  <D><R>
-
<B>  441  <D><R>
-
<B>  442  <D><R>
When programming using a data file residing in the programmer's user
RAM, the data to be programmed into device EPROM must reside in the
first 8000h bytes of user RAM beginning at address 0.  If the entire
8000h byte block is not used then the remainder must be filled with
some useless value, i.e. zero or FF, which is the blank state.  Data to
be programmed into device EEPROM must reside in a 200h byte block of
user RAM beginning at location 8000h.  As with the data to be programmed
into the EPROM, all unused locations must be filled with a useless value.
This can be accomplished using the FILL function under the MORE - EDIT
screen.
<B>  443  <D><R>
Correspondence between the programmer's user RAM and device memory is such
that the first 8000h bytes of the programmer's user RAM starting at location
0 corresponds to the 8000h bytes of device EPROM which begins at location 8000h.

The next 200h bytes of the programmer's user RAM starting at location 8000h
corresponds to the 200h bytes of device EEPROM beginning at address 400h.
<B>  444  <D><R>
-
<B>  445  <D><R>
-
<B>  446  <D><R>
-
<B>  447  <D><R>
-
<B>  448  <D><R>
This is the required algorithm for the following devices with a date code of
9616A or later:
      TIBPAL16R4-15M
      TIBPAL16R6-15M
      TIBPAL16R8-15M
      TIBPAL16L8-15M

This devices die was changed beginning at date code 9616A, and the new die
requires a different algorithm.
<B>  449  <D><R>
-
<B>  450  <D><R>
Data to be programmed to the device is offset to 0000h in User RAM.
This corresponds to device address 2000h.

Address(in words)        Address(in bytes)        Intel Required Data:
---------------          -----------------        ----------------------
  0000h - 0009h          0000h through 0013h      interrupt vectors (lower)
          000Ah          0015h    and    0014h    FFh, FFh (also see note #2)
          000Bh          0017h    and    0016h    FFh, FFh (also see note #1)
          000Ch          0019h    and    0018h    **h, CCB or CCB0 byte
          000Dh          001Bh    and    001Ah    **h, **h or CCB1 byte
          000Eh          001Dh    and    001Ch    **h, FFh  (reserved)
          000Fh          001Fh    and    001Eh    **h, FFh  (reserved)
  0010h - 0017h          0020h through 002Fh      security key
  0018h - 001Fh          0030h through 003Fh      interrupt vectors (upper)
```

```
    0020h - 002Eh          0040h through 005Dh    PTS vectors
    002Fh - 003Fh          005Eh through 007Fh    all FFh (reserved)


**h are also reserved locations and user must fill with the required data.
Consult Manufacturer's specifications for further information.


Note 1: To enable  CDE (clock detect enable bit), fill locations
with 0Ch, DEh.  Refer to the device spec. sheet for detailed
information (CDE bit is implemented only on some 196XX family
members).


Note 2: To program OSC bits fill these locations with:
     2015H     OSC1:OSC0     OSCOUT
     -----     ---------     ------
     FFh       00            divide by 2
     11        01            divide by 1
     44        10            divide by 4


Other values in 2015h will result in no programming of the
OSC bits.  Refer to the device spec. sheet for detailed
information.


Other device options are enabled from the programming screen.
     Program Security Fuse 1: DED programming
     Program Security Fuse 2: DEI programming
     Program Security Fuse 3: programs LOC1/LOC0


To enable Security Key Verification, the byte, after the device size
in user ram, should be set to a non-zero value.


Example:  For the 87C196LB set:
     WORD        BYTE         VALUE
     address     address
     3000h                    XXFFh enable security key verify.
                 6000h        FFh   enable security key verify.
     3000h                    xx00h disable security key verify.
                 6000h        00h   disable security key verify.


Key verification will program the device security locations with data
from user ram if the LOC1/LOC0 bits have not been programmed.


User Ram is displayed in words as default.  Byte display mode is also
available.
<B>   451  <D><R>
-
<B>   452  <D><R>
This algorithm uses 1 msec programming pulses.
Use for older devices.
Replaces algorithms SE370C756FN/FZ and
TSM370C756FN/FZ.
<B>   453  <D><R>
Blank check operation is performed only on EPROM arrays.
<B>   454  <D><R>
This device has a boot block at the beginning of the memory
array that has a programming lockout feature that protects
data from being reprogrammed or erased.  This feature, once
enabled, is permanent and cannot be reset.
```

```
<B>  455  <D><R>
During a Program or Verify operation, ensure that the number of verify
passes is set to 2.
<B>  456  <D><R>
-
<B>  457  <D><R>
-
<B>  458  <D><R>
For ACT3 and 12xxXL FPGA's; generate .DIO file
using Actel Designer FUS2DIO utility, download .DIO to
UniSite or 3900 programmer by selecting translation format 10.

Notes:  1) Set Blank Check to "Y" (enabled) for
           device to program properly.
        2) Do not change User data size field after
           downloading .DIO file.

Actel does not permit a separate post-
programming VERIFY DEVICE operation.

LOAD DEVICE will display the following
information:

      1) ALS Design Checksum -
         (not to be confused with the Data I/O ram image checksum).

      2) Customer Silicon Signature -
         (from .DIO file)

      3) Security Fuse status -
       0 = No Security
         1 = Security Enabled

      4) Program Fuse status -
       0 = Device not programmed
         1 = Device successfully programmed

Contact Data I/O Technical Support to request Actel Programming Application
note (part #983-0318-002).
<B>  459  <D><R>
-
<B>  460  <D><R>
-
<B>  461  <D><R>
-
<B>  462  <D><R>
-
<B>  463  <D><R>
-
<B>  464  <D><R>
-
<B>  465  <D><R>
-
<B>  466  <D><R>
-
<B>  467  <D><R>
-
```

```
<B>  468  <D><R>
-
<B>  469  <D><R>
-
<B>  470  <D><R>
-
<B>  471  <D><R>
-
<B>  472  <D><R>
-
<B>  473  <D><R>
-
<B>  474  <D><R>
-
<B>  475  <D><R>
-
<B>  476  <D><R>
-
<B>  477  <D><R>
-
<B>  478  <D><R>
-
<B>  479  <D><R>
-
<B>  480  <D><R>
-
<B>  481  <D><R>
-
<B>  482  <D><R>
```
This device has 14 bit data words represented as 16 bit data
for the programmer. Data bits 14 and 15 in Main Array and 8-15
in User ID are not used. Unused bits are loaded from the device
as zeros, ignored during Verify operation, and set to zero
during programming.

The Security Bit can be programmed by enabling the security fuse feature
in the Program Device Menu.

When assembling source file, output a merged 8 bit Intellec Hex object
file (INHX8M). Then download to the programmer by selecting Intel
Intellec 8/MDS translator (code 83).

To insure the integrity of the programmer's checksum, the unused memory
locations in user RAM must be set to zero prior to loading a device or
downloading data. Use the Fill Ram option under the More-Edit screen.

Consult the Manufacturer's specifications for further information.
```
<B>  483  <D><R>
-
<B>  484  <D><R>
-
<B>  485  <D><R>
-
<B>  486  <D><R>
-
<B>  487  <D><R>
-
```

```
<B>  488  <D><R>
-
<B>  489  <D><R>
-
<B>  490  <D><R>
-
<B>  491  <D><R>
-
<B>  492  <D><R>
-
<B>  493  <D><R>
-
<B>  494  <D><R>
-
<B>  495  <D><R>
-
<B>  496  <D><R>
-
<B>  497  <D><R>
-
<B>  498  <D><R>
-
<B>  499  <D><R>
-
<B>  500  <D><R>
-
<B>  501  <D><R>
-
<B>  502  <D><R>
```
To secure the device, set at least one location from address FFF6h
to FFFDh in User RAM to other than device blank state
(Do Not leave FFF6h to FFFDh blank).

To perform operations on secured device, put security code in
User RAM locations 0000h to 0007h.

```
<B>  503  <D><R>
```
Bits 0 and 1 in configuration word may be programmed by MCT.
If so, programming device may produce Illegal Bit Error.
Disable Blank Check to program device.
```
<B>  504  <D><R>
-
<B>  505  <D><R>
-
<B>  506  <D><R>
-
<B>  507  <D><R>
-
<B>  508  <D><R>
-
<B>  509  <D><R>
-
<B>  510  <D><R>
-
<B>  511  <D><R>
```

-
<B> 512 <D><R>
-
<B> 513 <D><R>
-
<B> 514 <D><R>
-
<B> 515 <D><R>
-
<B> 516 <D><R>
-
<B> 517 <D><R>
-
<B> 518 <D><R>
The available program area is "0000hex - 7FFFhex". The data in all
other areas should be set to "FF".
<B> 519 <D><R>
-
<B> 520 <D><R>
-
<B> 521 <D><R>
-
<B> 522 <D><R>
-
<B> 523 <D><R>
-
<B> 524 <D><R>
-
<B> 525 <D><R>
-
<B> 526 <D><R>
-
<B> 527 <D><R>
-
<B> 528 <D><R>
-
<B> 529 <D><R>
-
<B> 530 <D><R>
-
<B> 531 <D><R>
-
<B> 532 <D><R>
-
<B> 533 <D><R>
-
<B> 534 <D><R>
-
<B> 535 <D><R>
-
<B> 536 <D><R>
-
<B> 537 <D><R>
-
<B> 538 <D><R>
-
<B> 539 <D><R>

-
<B>   540   <D><R>
-
<B>   541   <D><R>
-
<B>   542   <D><R>
-
<B>   543   <D><R>
-
<B>   544   <D><R>
To eliminate ground bounce, put a .33uF capacitor across
power and ground pins.
<B>   545   <D><R>
-
<B>   546   <D><R>
-
<B>   547   <D><R>
If device fails Verify, switch to one pass verify.
<B>   548   <D><R>
-
<B>   549   <D><R>
Device uses standard 16V8 JEDEC file (QF = 2194).
The PD (sleep mode bit) must be programmed with value "0"
to disable sleep mode. When loading or verifying, the PD or sleep
mode bit must read/verify as "0".
<B>   550   <D><R>
It is recommended that a "Fill fuse map" operation with the
fill variable set to 0 is performed prior to downloading a
design file or performing a "Load" operation. This will
ensure that consistent checksums are reported.
<B>   551   <D><R>
-
<B>   552   <D><R>
Data in User Memory is partitioned as follows:

                        68HC705JP7/JJ7

 USER EPROM   - 0700 - 1EFF hex   programmable
 COPR   1FF0   programmable
 MOR   -   1FF1   programmable
 USER VECTORS   - 1FF2 - 1FFF hex   programmable
 PEPROM (personality) - 2000 - 207F hex   64 bytes programmable

The PEPROM resides in programmer's User Memory as follows :

 2000 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00   row0
 2010 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00   row1
 2020 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00   row2
 2030 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00   row3
 2040 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00   row4
 2050 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00   row5
 2060 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00   row6
 2070 xx xx xx xx xx xx xx xx 00 00 00 00 00 00 00 00   row7

      c0 c1 c2 c3 c4 c5 c6 c7

The PEPROM map corresponds to the map of the Motorola programmer.
Data for locations marked as xx can be 00 hex or 01 hex. Locations
marked as 00 should be filled with 00 hex.

<B> 553 <D><R>
Enable the security fuse option (Y) on the PROGRAM DEVICE
options screen to set BP1 and BP2 bits in the Write Protect
Register.
<B> 554 <D><R>
-
<B> 555 <D><R>
-
<B> 556 <D><R>
-
<B> 557 <D><R>
-
<B> 558 <D><R>
This part uses the extended ATF16V8C JEDEC file (JEDEC QF field = 2195).
The PD or sleep mode bit is specified by the value on JEDEC fuse
number 2194.

<B> 559 <D><R>
-
<B> 560 <D><R>
-
<B> 561 <D><R>
-
<B> 562 <D><R>
-
<B> 563 <D><R>
-
<B> 564 <D><R>
-
<B> 565 <D><R>
-
<B> 566 <D><R>
-
<B> 567 <D><R>
-
<B> 568 <D><R>
-
<B> 569 <D><R>
-
<B> 570 <D><R>
-
<B> 571 <D><R>
-
<B> 572 <D><R>
-
<B> 573 <D><R>
-
<B> 574 <D><R>
-
<B> 575 <D><R>
-
<B> 576 <D><R>

-
<B>   577   <D><R>
-
<B>   578   <D><R>
-
<B>   579   <D><R>
-
<B>   580   <D><R>
-
<B>   581   <D><R>
-
<B>   582   <D><R>
-
<B>   583   <D><R>
-
<B>   584   <D><R>
-
<B>   585   <D><R>
-
<B>   586   <D><R>
-
<B>   587   <D><R>
-
<B>   588   <D><R>
When downloading PSD file (.obj) set the following
options:

          I/O Translation Format   99
          I/O address offset   0
          Memory begin address   0
          User data size   0

NOTE: To get a consistent checksum clear RAM with a zero pattern
before downloading the PSD data file.

Devices are only protected if the security fuse option is selected
in the device programming screen.
<B>   589   <D><R>
-
<B>   590   <D><R>
-
<B>   591   <D><R>
The M37692E8FS-PGA requires the following
adapters: MSV37692-PGA, MITSUBISHI
MICRO INTERFACE(MMI)adapter.

<B>   592   <D><R>
Set data in character generator ROM to "F" hex (lower 4 bits) as follows:

    Device address   Data
------------------------------------   --
00000hex - 11FFFhex   User data
12000hex - 13FFFhex   "XF"   X...User 4BIT data
------------------------------------   --
<B>   593   <D><R>

This device contains a four byte Signature String of
alphanumeric characters. The four bytes will be momentarily
displayed during the "Load" and "Verify" operations. If any
of the four bytes is a non-printing character the Signature
String will not be displayed.

Selecting the "Program security fuse" option will read-secure
the device. Once secured the user can not load, verify,
program, or blank check the device. However, a read-secured
device can be electronically erased. The erased device is no
longer read-secured and can be reprogrammed.
<B> 594 <D><R>
Fuse 5848 is not programmable on this device, and is
retained for JEDEC file compatibility only.
<B> 595 <D><R>
This device contains a User Electronic Signature (UES) array and a
Power Down (PD) bit. Programming the UES array and PD bit is optional.
Three devices are available: one with the "EXT" suffix containing the
UES and PD bits, one with a "U" suffix containing UES bits only, and
one without any suffix containing no UES or PD bits.

The device with the "EXT" suffix programs all the arrays. The device
with the "U" suffix programs the UES array but disables the PD mode.
The device without any suffix disables the UES and PD modes.

When you download a JEDEC file, you will select the device compatible
with the JEDEC file. If the device is not compatible, one of the
following errors will be displayed: File not initialized or
Incompatible user data.
<B> 596 <D><R>
-
<B> 597 <D><R>
-
<B> 598 <D><R>
Available program area is "4000 hex - FFFF hex".
The data in all other areas should be set to "FF".

Set JP1="FLASH" and JP2="1M".
<B> 599 <D><R>
-
<B> 600 <D><R>
-
<B> 601 <D><R>
-
<B> 602 <D><R>
-
<B> 603 <D><R>
-
<B> 604 <D><R>
Configuration byte programming is supported on this device. This feature
can be enabled from the Program Device screen. The configuration bytes
are in the following locations.

```
                              87251A1
                              ---------
  MAIN ARRAY DATA             0-5FFF hex
  ENCRYPTION ARRAY DATA       NOT USED
```

CONFIGURATION BYTES   6080-6083 hex

Note that these values are all offsets from the memory begin address
field located in the PROGRAM DEVICE options screen. If the memory
begin address is not zero (default) , add the value in this field to the
offset for the appropriate address. Also note that to program special
features, enter data at the appropriate memory locations, and set
the corresponding field in the PROGRAM DEVICE options screen to "Y."
Enabling the "Program Configuration" programs the configuration bytes.

<B> 605 <D><R>
Encryption array, lock bit, and configuration byte programming are all
supported on this device. These features can be enabled from the Program
Device screen. The encryption array and configuration bytes have data in
User Memory.

                            87251G1

     MAIN ARRAY DATA   0-3FFF hex
     ENCRYPTION ARRAY DATA 4000-407F hex
     CONFIGURATION BYTES   4080-4083 hex

Note that these values are all offsets from the memory begin address
field located in the PROGRAM DEVICE options screen. If the memory
begin address is not zero (default) , add the value in this field to the
offset for the appropriate address. Also note that to program special
features, enter data at the appropriate memory locations, and set
the corresponding field in the PROGRAM DEVICE options screen to "Y."
Enabling the security fuses programs the lock bits, "Program XNOR data"
programs the encryption array, and "Program Configuration" programs the
configuration bytes.

After the Encryption Array is programmed, device data will no longer
match data in User RAM. After programming security bits, programming
operations are no longer allowed.
<B> 606 <D><R>
-
<B> 607 <D><R>
The selected device has a 14 bit data word that is represented as
16-bit data on the programmer. All unused bits are read from the device as
zeros, ignored during a verify operation, and set to zero during a
program operation.

Set the "Program Security Fuse" in the program device menu to 'Y',
to secure the main array of the device.

Use the output option, that produces a merged 8-bit Intellec Hex
object file (INHX8M). Download the file to the programmer
using the Intel Intellec 8/MDS translator (code 83).
<B> 608 <D><R>
Device has a 14 bit data word which is represented as 16 bit data
for the programmer. All unused bits are loaded from the device as zeros,
ignored Verify, and set to zero during Program.

Bits 4 and 5 of the configuration word are the security fuses.
The options are as follows:

```
                  00      All memory is code protected.
                  01      Upper 3/4th of program memory code protected.
                  10      Upper half of program memory code protected.
                  11      Code protection off.


Program Security Bit by enabling the security fuse
feature in the Program Device Menu.

Use the output option that produces merged 8 bit Intellec Hex
object file (INHX8M) then download to the programmer by selecting
the Intel Intellec 8/MDS translator (code 83).
<B>  609  <D><R>
-
<B>  610  <D><R>
This device has two type TSOP package.
TSOP 40pin is stamped as 29F080-xxPTN.
TSOP 48pin is stamped as 29F080-xxPFTN.
xx means speed.
<B>  611  <D><R>
-
<B>  612  <D><R>
-
<B>  613  <D><R>
-
<B>  614  <D><R>
M37602E8FS-LCC requires the following adapters:
MSV37602-80DO and MITSUBISHI MICRO INTERFACE(MMI)adapter.

Mitsubishi adapter socket opens facing pin #1. If the Mitsubishi
adapter has a jumper, set it to the UniSite configuration.

<B>  615  <D><R>
The Mitsubishi M37510Ex-COB requires the MSV3800-COB and MITSUBISHI
MICRO INTERFACE(MMI)adapters. To position the Mitsubishi
adapter on top of the MMI, place the COB alignment notch
over pin #20 of the MMI adapter.

NOTE: If the Mitsubishi adapter has a jumper, set it to the UniSite
configuration.
<B>  616  <D><R>
The Mitsubishi M37620E8FS-PGA requires MSV37620-PGA and MITSUBISHI
MICRO INTERFACE(MMI)adapters.

If Mitsubishi adapter has a jumper, set it to the UniSite configuration.
<B>  617  <D><R>
Device requires a socket adapter available from
Emulation Technology Inc. (408-982-0660).

-------------------------------------------------
I/P2032V/VE-44P*    44  pin PLCC     AS-44-28-03P
I/P2032V/VE-44T*    44  pin TQFP     AS-44-28-02Q
I2032VE-48T*        48  pin TQFP     AS-48-28-01Q
I/P2096V/VE-128P*  128 pin PQFP     AS-128-28-02Q-6
I/P2096V/VE-128T*  128 pin TQFP     AS-128-28-04Q-6
I/P2128V/VE-84P*    84  pin PQFP     AS-84-28-05P-6
I/P2128V/VE-100T*  100 pin TQFP     AS-100-28-04Q-6
```

```
I/P2128V/VE-160P*   160 pin PQFP    AS-160-28-03Q-6
I/P2128V/VE-176T*   176 pin TQFP    AS-176-28-02Q-6
I2192VE-128T*       128 pin TQFP    AS-128-28-04Q-6
<B>  618  <D><R>
-
<B>  619  <D><R>
-
<B>  620  <D><R>
-
<B>  621  <D><R>
Device needs DIP Switch set in PPI-5705 as follows,
SW1
   Switch name D0  D8  D1  D9  D2  D10 D3  D11
               -----------------------------
       Setting ON  OFF ON  OFF ON  OFF ON  OFF
SW2
   Switch name D4  D12 D5  D13 D6  D14 D7  D15
               -----------------------------
       Setting ON  OFF ON  OFF ON  OFF ON  OFF

NOTE: For FUJ 29F800T and 29F800B if the settings
above result in a Verify error, set D15-D8 to ON.
<B>  622  <D><R>
-
<B>  623  <D><R>
-
<B>  624  <D><R>
For Altera QFP devices, menu selections with 'N' as the last character
such as 7128-Q160N are for QFP devices that are not encased in a
plastic chip carrier.
<B>  625  <D><R>
Structured vector testing not operational at this time.  Please
disregard vector test failures.
<B>  626  <D><R>
Adapter W66EP5316D is a 52pin SDIP socket. Devices should be inserted
on the pin 1 mark in the socket adapter. The lower 10 contacts not used.

To enable data security:
 1)Set the jumper(DASEC) attachment to the "ON" side.
 2)Disable Blank check, Illegal bit check.
 3)Execute program. "Programming error" occurs.
 4)Set the jumper(DASEC) attachment to the "OFF" side after
   executing the data security.
<B>  627  <D><R>
To enable data security:
 1)Set the jumper(DASEC) attachment "ON" side.
 2)Disable Blank check, Illegal bit check.
 3)Execute program. "Programming error" occurs.
 4)Set the jumper(DASEC) attachment "OFF" side after
   executing data security.
<B>  628  <D><R>
-
<B>  629  <D><R>
-
<B>  630  <D><R>
-
<B>  631  <D><R>
```

-
<B> 632 <D><R>
-
<B> 633 <D><R>
-
<B> 634 <D><R>
-
<B> 635 <D><R>
The following list provides information on
making a device menu selection.

ICT DEVICE	FEATURES IN THE DEVICE	MENU SELECTION
22CV10A	STANDARD	22CV10A or 22CV10A-PLC
22CV10A	ENHANCED	22CV10A+ or 22CV10A+PLC
22CV10AZ	STANDARD	22CV10AZ or 22CV10AZ-PLC
22CV10AZ	ENHANCED	22CV10AZ+ or 22CV10AZ+PLC
22LV10AZ	STANDARD	22LV10AZ or 22LV10AZ-PLC
22LV10AZ	ENHANCED	22LV10AZ+ or 22LV10AZ+PLC

<B> 636 <D><R>
The available program area is "0000hex - F77Fhex". The data in all
other areas should be set to "FF".

<B> 637 <D><R>
Device requires SOP44pin->DIP48pin conversion socket adapter
(OKI Electric Industry Co., Ltd.).
<B> 638 <D><R>
-
<B> 639 <D><R>
To enable data security.
 1)Set jumper(DASEC) attachment "ON" side.
 2)Disable Blank check, Illegal bit check.
 3)Execute program. "Programming error" occurs.
 4)Set jumper(DASEC) attachment "OFF" side after
   executing data security.
<B> 640 <D><R>
To enable data security.
 1)Set the jumper(DASEC) attachment to the "ON" side.
 2)Disable Blank check and Illegal bit check.
 3)Execute program. "Programming error" occurs.
 4)Set the jumper(DASEC) attachment to the "OFF" side after
   executing the data security.
<B> 641 <D><R>
Standard 7064 POF file can be programmed by the following entries:
"7064", or Altera X-PGM menu entry "7064S AS 7064". 7064S POF files can
only be programmed with a 7064S entry.
<B> 642 <D><R>
-
<B> 643 <D><R>
Available program area of device is "C080 hex - FFFD hex".
Set the Device begin address and the Device block size as follows:

Device begin address: C080
Device block size: 3F7E

```
<B>   644   <D><R>
-
<B>   645   <D><R>
This device is not reprogrammable.  Please erase device before programming.
<B>   646   <D><R>
-
<B>   647   <D><R>
-
<B>   648   <D><R>
-
<B>   649   <D><R>
-
<B>   650   <D><R>
-
<B>   651   <D><R>
Use the F1500A
<B>   652   <D><R>
Use the 1500A
<B>   653   <D><R>
To ensure that the pin keeper circuits on the 1500A/AL/ABV/ABVL
are enabled/disabled according to requirements, use the
1500A/AL/ABV/ABVL-PLCC/TQFP algorithm with a 1500A/AL/ABV/ABVL JEDEC file.
<B>   654   <D><R>
Data in the programmer's User Memory is partitioned as follows:

  NOT IMPLEMENTED            0 through 07FF hex
  RESERVED                  0800 through 0B9F hex
  PROGRAMMABLE              0BA0 through 0F9F hex
  RESERVED                  0FA0 through 0FEF hex
  PROGRAMMABLE              0FF0 through 0FF7 hex
  RESERVED                  0FF8 through 0FFB hex
  PROGRAMMABLE              0FFC through 0FFF hex
<B>   655   <D><R>
-
<B>   656   <D><R>
This device requires the use of Emulation Technologies
adapter 282801S600-GANG and the PPI adapter 0104
<B>   657   <D><R>
-
<B>   658   <D><R>
For this device package the device must be inserted in the socket
"Dead Bug" style; this means the leads of the package are pointing
up from the socket.  Pin 1 of the device should be in the upper
right corner of the socket.
<B>   659   <D><R>
If you experience intermittent "Overcurrent Errors" we recommend
capacitor block 44B installed on the test-site at position X1 & X3.
<B>   660   <D><R>
Data in the programmer User Memory is partitioned as follows:

  EEPROM                        0 through 007F hex
  PROGRAMMABLE              0080 through 0F9F hex
  RESERVED                  0FA0 through 0FEF hex
  PROGRAMMABLE              0FF0 through 0FF7 hex
  RESERVED                  0FF8 through 0FFB hex
  PROGRAMMABLE              0FFC through 0FFF hex
  RESERVED                  1000 through 100F hex
```

```
      PROGRAMMABLE                  1010 through 17FF hex
      RESERVED                      1800 through 180F hex
      PROGRAMMABLE                  1810 through 1FFF hex


 NOTE: For the 62T42 & 62E42 devices:
   RESERVED                         0 through 007F hex


 NOTE: Support for 62T40 and 62E40 devices requires
 a modified PPI-0507 (has a "-2" for the board revision number).


 <B>  661  <D><R>
 RC calibration value is stored at 3FFh (programmed at the factory).

 This device has a 12 bit data word which is represented as 16 bit data
 for the programmer. All unused bits are loaded from the device as zeros,
 ignored during Verify operation, set to zero during programming.


 To program Security Bit, enable security fuse feature in Program Device Menu.


 Use the output option that produces merged 8 bit Intellec Hex object file
 (INHX8M) then download to the programmer by selecting Intel Intellec 8/MDS
 translator (code 83).
 <B>  662  <D><R>
 RC calibration value is stored at 3FFh (programmed at the factory).

 This device has a 12 bit data word which is represented as 16 bit data
 for the programmer. All unused bits loaded from the device as zeros,
 ignored during Verify, and set to zero during programming.


 To program Security Bit, enable security fuse feature in the Program Device Menu
 .


 Use output option which produces merged 8 bit Intellec Hex
 object file (INHX8M) then download to programmer by selecting
 Intel Intellec 8/MDS translator (code 83).
 <B>  663  <D><R>
 -
 <B>  664  <D><R>
 Device has odd/even parity bits (hidden) associated with all memory locations.
 Parity is calculated "on the fly" for Verify and Program routines.

 NOTE: Parity is calculated and programmed for all locations so a blank
 location will have parity bits set.



 <B>  665  <D><R>
 This device has a 14 bit data word which is combined with two parity bits
 (hidden from user) to form 16 bit data for the programmer. All unused
 bits are loaded from the device as zeros,
 ignored during Verify, and set to zero during programming.


 To program Security Bit, enable security fuse feature in the Program Device Menu
 .


 Use output option which produces merged 8 bit Intellec Hex
 object file (INHX8M) then download to programmer by selecting
 Intel Intellec 8/MDS translator (code 83).
```

<B> 666 <D><R>
Device requires SSOP-70pin to DIP-48pin conversion adapter
(part number OKI SOCKET70S-48, Oki electric industry Co. Ltd.).

For use on UniSite with Site48HS, extend adapter leads by 15mm.

For use on 3900 with 39BASE-0101 and 2900 with 29BASE-0102,
bend lever to either side.

For use on ChipLab/2700/LabSite, set user memory size
to more than 4096 bytes. Memory buffer size greater than
512 bytes is recommended. Bend lever to either side.
<B> 667 <D><R>
-
<B> 668 <D><R>
Damage to device and/or programming errors may occur if newer FX-CORE
devices with a topside tracking number (FPO number) ending with a
letter, such as A,B,C,D,E, F, etc?) is programmed with incorrect
device menu selection. For example, the tracking numbers L0507B20F or
L0506C20A printed below the Intel 87c51/FA/FB part marking would
indicate a FX core Device. If you are working with newer samples, you
are most likely working with FX core parts, the older parts were last
shipped around 1990.
<B> 669 <D><R>
-
<B> 670 <D><R>
-
<B> 671 <D><R>
pin 13
<B> 672 <D><R>
Pin 24
<B> 673 <D><R>
Pins 30, 31
<B> 674 <D><R>
Pin 10
<B> 675 <D><R>
-
<B> 676 <D><R>
PM2 will be programmed to zero when code protect parameters are enabled.
<B> 677 <D><R>
Pins 10, 20, 31
<B> 678 <D><R>
Pins 10, 31, 39
<B> 679 <D><R>
Noise bypass capacitors are required for this device as follows:

Pin 37   100 pF
Pins 4, 16, 24, and 36   0.1 uF

The PPI adapter comes with capacitor sockets (for each pin) pre-installed.

<B> 680 <D><R>
-
<B> 681 <D><R>
CAUTION : OTP Security Page data resides in User RAM 800h - 80Fh.
Location must remain in blank state (FFh) if OTP Security Page is unused.

```
<B>  682  <D><R>
-
<B>  683  <D><R>
To Enable Serial Programming, set PROGRAM XNOR DATA field
on Program Memory Device Option screen to 'N' (to disable, set to 'Y').

<B>  684  <D><R>
Device requires socket adapter H73035Q080D3201 (available from Data I/O).
<B>  685  <D><R>
Device requires socket adapter H73035T080D3201 (available from Data I/O).
<B>  686  <D><R>
-
<B>  687  <D><R>
Device requires socket adapter H7224XQ100D3201 (available from Data I/O).
<B>  688  <D><R>
Device requires socket adapter H7224XT100D3201 (available from Data I/O).
<B>  689  <D><R>
Device requires socket adapter H7265XT120D3201 (available) from Data I/O).
<B>  690  <D><R>
Device requires socket adapter H7212XQ064D3201 (available from Data I/O).
<B>  691  <D><R>
Byte Swap Option may need to be enabled.
<B>  692  <D><R>
-
<B>  693  <D><R>
-
<B>  694  <D><R>
An "Invalid Architecture Word" error will be displayed if the User RAM data
contains an incorrect "RAM Architecture configuration" for this device.
<B>  695  <D><R>
-
<B>  696  <D><R>
Device requires one of following socket adapters:

1, Hitachi HS7042ESHS1H (from device manufacturer).
2, Data I/O H7704XQ122D3201.

In UniSite with SITE48HS DIP module, extend pin leads of Hitachi
HS7042ESHS1H adapter by 10mm.
<B>  697  <D><R>
-
<B>  698  <D><R>
-
<B>  699  <D><R>
_1 Menu Selection: PPI-0266
_2 Menu Selection: PPI-PLCC68
<B>  700  <D><R>
-
<B>  701  <D><R>
-
<B>  702  <D><R>
-
<B>  703  <D><R>
-
<B>  704  <D><R>
Device must be rotated 180 degrees
<B>  705  <D><R>
```

```
-
<B>   706   <D><R>
-
<B>   707   <D><R>
-
<B>   708   <D><R>
DEVICE            DEVICE MEMORY MAP
90T40          0000h -> 3FBFh EPROM
90T40          3FC0h -> 41BFh EEPROM

90E40          0000h -> 3FFFh EPROM
90E40          4000h -> 41FFh EEPROM
<B>   709   <D><R>
-
<B>   710   <D><R>
```

Sector operations are set up under the "SECTOR CONFIGURATION" table. This
table allows the user to select specific sector operations such as Erase,
Program, or Protect. The following directions will assist you in navigating
to this table relative to your programmer interface:
For the TaskLink user:
The "SECTOR CONFIGURATION" table is located in the "Sector" tab under
"Programmer Properties" dialog box.
For the Hiterm/Terminal user:
The "SECTOR CONFIGURATION" table is located in the "Device Configure" screen.

```
<B>   711   <D><R>
```

Problems may be encountered when using this menu selection with certain
newer Altera devices. Data I/O Corp. is aware of these problems and
action is being taken to correct them. If a problem is encountered
please call Data I/O Corp. Customer Support at 1-800-247-5700.

```
<B>   712   <D><R>
```

Sector protect/unprotect operation not supported for this FLASH DIP module.
If module is already sector-protected, module can not be erased.

1)UniSite case
Two similar device names are displayed on menu.
The difference is due to DIP Base identity.

```
Selected name    installed DIP Base
------------    ----------------------
8502F016FA       SITE 48
8501F016FA       SITE 48
8502F016FAHS     SITE 48HS
8501F016FAHS     SITE 48HS
------------    ----------------------
```

2)ChipLab/2700/LabSite case
Set user memory size as follows,

```
DIP Module     User Memory Size(Minimum)
------------   ---------------------
MB8501F016FA   2048 Byte
MB8502F016FA   4096 Byte
------------   ---------------------
<B>   713   <D><R>
```

Data bits 5-7 should be set to 1 at all address locations.
Refer to Hitachi spec sheet for correct data pattern.

```
<B>   714   <D><R>
Available program area is "A080 hex - FFFD hex".
Set device begin address to A080 hex, and device block size to 5F7E hex.
Refer to Mitsubishi spec sheet for details.
<B>   715   <D><R>
Available program area is "4080 hex - FFFD hex".
Set device begin address to 4080 hex, and device block size to BF7E hex.
Refer to Mitsubishi spec sheet for details.
<B>   716   <D><R>
Available program area is "C080 hex - FFFD hex".
Set device begin address to C080 hex, and device block size to 3F7E hex.
Refer to Mitsubishi spec sheet for details.
<B>   717   <D><R>
Available program area is "8080 hex - FFFD hex".
Set device begin address to 8080 hex, and device block size to FFFD hex.
Refer to Mitsubishi spec sheet for details.
<B>   718   <D><R>
-
<B>   719   <D><R>
-
<B>   720   <D><R>
Block Lock-bit function is not supported. Block Lock-bit
can't be set and cleared.
<B>   721   <D><R>
Device requires SOIC-DIP conversion adapter -
part number SOCKET32-32 by OKI Electric Industry Co, Ltd.


<B>   722   <D><R>
Device requires TSOP-DIP conversion adapter -
part number SOCKET32T by OKI Electric Industry Co., Ltd.


<B>   723   <D><R>
Boot block at end of memory array has a programming lockout
feature (once enabled, cannot be reset) to protect data
from being reprogrammed or erased.
<B>   724   <D><R>
-
<B>   725   <D><R>
-
<B>   726   <D><R>
-
<B>   727   <D><R>
Continuity test does not check for a device installed backwards in the socket.
A device installed backwards in the socket can cause an overcurrent error.
<B>   728   <D><R>
Implement Encryption Array security option from PROGRAM DEVICE Options screen.

Enter Encryption Array data into User Memory following the
Main Array data.  Below is the memory partition information for
various devices:


              87C51           87C52
              ------------    ------------
MAIN ARRAY    :    0 - 0FFFh      0 - 1FFFh
```

```
ENCRYPT. ARRAY: 1000 - 103Fh   2000 - 203Fh


<B>  729  <D><R>
Device requires socket adapter OKI 7A1A (exclusive for
OKI 27C4X2XX SO-40pin devices).
<B>  730  <D><R>
-
<B>  731  <D><R>
Device manufacturer requires one pass verify.  It is recommended
that the "Verify passes" option be set to 1 for this device during
programming to avoid redundancy in post programming verify.
<B>  732  <D><R>
Adapter must have a revision number(-003) or greater.
<B>  733  <D><R>
Preload vectors are not supported in the current release.
<B>  734  <D><R>


Data in Programmer's User RAM is partitioned as follow:


              FLASH          EEPRPM          FUSES
           ------------    ------------     -----
AT90S1200    0000h - 03FFh   0400h - 043Fh    0440h
AT90S1200A   0000h - 03FFh   0400h - 043Fh    0440h
AT90S8515    0000h - 1FFFh   2000h - 21FFh    2200h
AT90S8535    0000h - 1FFFh   2000h - 21FFh    2200h
AT90S4414    0000h - 0FFFh   1000h - 10FFh    1100h
AT90S2313    0000h - 07FFh   0800h - 087Fh    0880h
AT90S2323    0000h - 07FFh   0800h - 087Fh    0880h
AT90S2343    0000h - 07FFh   0800h - 087Fh    0880h


To program/reprogram fuses: put the proper data in Programmer's User RAM
fuse location (0440h, 2200h, 1100h, 0880h or ...) and set PROGRAM XNOR DATA
in the Program Memory Device Option screen to 'Y'.
Legal values are: 00h, 01h, 20h and 21h.



<B>  735  <D><R>
-
<B>  736  <D><R>
This device requires OKI's socket adapter.
Part number is OKI SOCKET44T-42 (TSOP-type2-44pin -> DIP-42pin).
<B>  737  <D><R>
Device requires socket adapter H7212XD064D3201 (available from Data I/O).
<B>  738  <D><R>
Device requires socket adapter H7212XT080D3201 (available from Data I/O).
<B>  739  <D><R>
This algorithm's data file memory map a long with it's checksum calculation
procedure DOES NOT match the semi manufacturer's programming tool and
specifications.  If you are programming this device for the first time
please use the other menu selection(if available.)
<B>  740  <D><R>
-
<B>  741  <D><R>
This MCP(FLASh & SRAM) device includes 8Mx16 bit FLASH.
Currently, the block protect function isn't supported.
Also, a block-protected device cannot be erased.
```

```
<B>   742   <D><R>
-
<B>   743   <D><R>
-
<B>   744   <D><R>
The Semi-vendor specifies that Software Data Protection must
be enabled as part of programming this device.  Therefore,
the Software Data Protection feature is not select-able option,
and is always enabled after programming the device.
<B>   745   <D><R>
-
<B>   746   <D><R>
-
<B>   747   <D><R>
-
<B>   748   <D><R>
-
<B>   749   <D><R>
This device requires the use of both a PPI adapter and the following
third party adapter:
<B>   750   <D><R>
This algorithm's data file memory map and associated checksum calculation
procedure matches the semi manufacturer's programming tool and specifications.
In TaskLink, enable "Use Algorithm Checksum" flag for semi manufacturer's
checksum calculation.
<B>   751   <D><R>
Sector protect and unprotect are not supported due to hardware limitation.
Therefore, protected device can't be erased and unprotected.
<B>   752   <D><R>
-
<B>   753   <D><R>
ETI 282803S600-GANG
<B>   754   <D><R>
This device requires OKI's socket adapter. The part number is OKI SOCKET70T-42.

<B>   755   <D><R>
Device requires SSOP-70pin to DIP-48pin conversion adapter
(Part number OKI SOCKET70S-48 or BN-95171A-T-2, Oki electric
industry Co. Ltd.).

For use on UniSite with Site48HS, extend adapter leads by 15mm.

For use on 3900 with 39BASE-0101 and 2900 with 29BASE-0102,
bend lever to either side.

For use on ChipLab/2700/LabSite, set user memory size
to more than 4096 bytes. Memory buffer size greater than
512 bytes is recommended. Bend lever to either side.
<B>   756   <D><R>
Data in the programmer's User Memory for this family of parts
is partitioned as follows:
STATE OF MEMORY        MEMORY MAP          MEMORY MAP          MEMORY MAP
---------------- ------------------ ------------------ ----------------
                 62T53C (2OPT)                         62T65B(1OPT)
                 62T10C,62T15C(2OPT) 62T20C,62T25C(2OPT) 62T60C(2OPT)
                 62T10B,62T15B(1OPT) 62T20B,62T25B(1OPT) 62T65C(2OPT)
---------------- ------------------ ------------------ ----------------
```

```
 RESERVED                 0 -> 087F hex          0 -> 007F hex          0 -> 007F hex
 PROGRAMMABLE          0880 -> 0F9F hex       0080 -> 0F9F hex       0080 -> 0F9F hex
 RESERVED              0FA0 -> 0FEF hex       0FA0 -> 0FEF hex       0FA0 -> 0FEF hex
 PROGRAMMABLE          0FF0 -> 0FF7 hex       0FF0 -> 0FF7 hex       0FF0 -> 0FF7 hex
 RESERVED              0FF8 -> 0FFB hex       0FF8 -> 0FFB hex       0FF8 -> 0FFB hex
 PROGRAMMABLE          0FFC -> 0FFF hex       0FFC -> 0FFF hex       0FFC -> 0FFF hex
 EEPROM                                                             1000 -> 107F hex
 OPTION BYTE(LSB)            1000 hex               1000 hex               1080 hex
 OPTION BYTE(MSB)            1001 hex               1001 hex               1081 hex
 ---------------- ------------------ ------------------ ----------------


                       62T63C(2OPT)
 ---------------- ------------------
 RESERVED                 0 -> 087F hex
 PROGRAMMABLE          0880 -> 0F9F hex
 RESERVED              0FA0 -> 0FEF hex
 PROGRAMMABLE          0FF0 -> 0FF7 hex
 RESERVED              0FF8 -> 0FFB hex
 PROGRAMMABLE          0FFC -> 0FFF hex
 EEPROM                1000 -> 103F hex
 OPTION BYTE(LSB)            1040 hex
 OPTION BYTE(MSB)            1041 hex
 ---------------- ------------------




                       62T30B,62T32B(1OPT)
 ---------------- ------------------
 RESERVED                 0 -> 007F hex
 PROGRAMMABLE          0080 -> 0F9F hex
 RESERVED              0FA0 -> 0FEF hex
 PROGRAMMABLE          0FF0 -> 0FF7 hex
 RESERVED              0FF8 -> 0FFB hex
 PROGRAMMABLE          0FFC -> 0FFF hex
 RESERVED              1000 -> 100F hex
 PROGRAMMABLE          1010 -> 17FF hex
 RESERVED              1800 -> 180F hex
 PROGRAMMABLE          1810 -> 1FFF hex
 EEPROM                2000 -> 207F hex
 OPTION BYTE(LSB)            2080 hex
 OPTION BYTE(MSB)
 ---------------- ------------------
```

(1OPT) = 1 option byte
(2OPT) = 2 option bytes(FORMAT: Lower Address = LSB; Upper Address = MSB)
<B> 757 <D><R>
OPTION BYTE: The Option byte(s) are at the end of the
device memory map. Please refer to the device data
sheet for number of option bytes, and what each option
bit represents. Enable programming by Selecting "Program
configuration" in the "Program device" screen.

In TaskLink: Make the following selections: Setup menu ->
General Parameters, then select the "ENABLE SPECIAL DATA.",
and set the Security Option to 2 enabling all security fuses.
<B> 758 <D><R>

Data in the programmer's User Memory is partitioned as follows:

```
  RESERVED                          0 through 007F hex
  PROGRAMMABLE                   0080 through 0F9F hex
  RESERVED                       0FA0 through 0FEF hex
  PROGRAMMABLE                   0FF0 through 0FF7 hex
  RESERVED                       0FF8 through 0FFB hex
  PROGRAMMABLE                   0FFC through 0FFF hex
  OPTION BYTES                   1000 through 1001 hex
```
<B> 759 <D><R>
To enable Low Noise Mode, enable Security fuse 1
in the Program device screen.

To enable Watch Dog Timer(WDT), enable Program
configuration, or Enable Special Data in the
Program device screen.

To secure the device, enable security fuse 3 in the
Program device screen (some load instructions will be
disabled).

NOTE: These option bits cannot be read on this device.
<B> 760 <D><R>
_1 Menu Selection: PPI-3524
_2 Menu Selection: PPI-0563
<B> 761 <D><R>
Device options can be set by adding a byte of data to the
end of the main array.

```
DEVICE:              86E02xxxx      86E04xxx      86E08xxx
MAIN ARRAY:        0 -> 200 hex  0 -> 400 hex  0 -> 800 hex
CONFIGURATION BYTE:     201 hex       401 hex       801 hex
```

The following format is used to configure the option bits:

```
SETTING:  YES/NO      NAME OF OPTION BIT
---------------------------------------------
BIT 0 =      1/0      Disable TEST Mode Bit
BIT 1 =      1/0      WDT Enable Bit
BIT 2 =      1/0      Autolatch Disable Bit
BIT 3 =      1/0      Low EMI Bit
BIT 4 =      x/x      EPROM Protect Bit
BIT 5,6,7 = x/x       Not Used
```

After placing the configuration byte at the end of the
main array, enable the "Program configuration", or Enable
Special Data in the Program device screen.

To secure the device, enable "Program security fuse" in
the Program device screen (some load instructions will be
disabled).

NOTE: These option bits may not be read correctly if both
the WDT enable, and EPROM protect features are programmed.
<B> 762 <D><R>
This device can be electrically erased and programmed up to 1000
times. Devices that have been erased over 1000 times, may fail the

erase operation.
<B> 763 <D><R>
Set sector preferences in Sector Configuration Table
(Device --> Sector Table)
<B> 764 <D><R>
Do not disable "Compare elec ID".

If an Electronic ID Error does occur, contact Data I/O for the latest
version of the programming algorithm.
<B> 765 <D><R>
-
<B> 766 <D><R>
Data word width of this device is 12 bit, but programmer user Memory is mapped
as 16 bit. 4 MSB's will be ignored in all Operations.
<B> 767 <D><R>
Data in the Programmer's User Memory is partitioned as follows:

```
                     SX28AC
                     ---------
  MAIN ARRAY DATA    0000-07FF
  ID MEMORIES        0800-080F
  FUSE WORD          0810-0810
  FUSEX WORD         0811-0811
```

To Program FUSE WROD and FUSEX WORD, enable "Program configuration" option in
Program Memory Device Options screen. Programmer will ignore the setting of
the CP bit in the FUSE WORD.
<B> 768 <D><R>
Consult the Manufacturer's specifications for further information.
<B> 769 <D><R>
-
<B> 770 <D><R>
To ensure that consistent checksums are reported, perform a
"Fill Ram" operation with FF data prior to downloading your
design file and before performing a device operation.
<B> 771 <D><R>
-
<B> 772 <D><R>
Adapter must have a revision number(-002) or greater.
<B> 773 <D><R>
The selected device has a non-programmable area,
address 0000 to 3FFF hex.

User data for these locations should be set to FF hex.
Or set the device begin address to 4000 hex and the
device block size to 4000 hex.

Refer to the device spec sheet for more information.
<B> 774 <D><R>
this device has a non-programmable area, address 0000 to 3FFF hex.
Set device begin address to 4000 hex and the device block size to
4000 hex, for all operations.

Refer to device specification sheet for more information.
<B> 775 <D><R>
The ID words and the config word have been moved to 2000H and 2007H per
microchip's request. If you are using the old configuration word

location you will need to move these to the new address location.

<B> 776 <D><R>
Block lock function can't be supported due to hardware limitation.
If the device was already locked, the device can't be erased.

This ETI adapter has a jumper switch.
The jumper switch should be set to the "DIP44" side not the "VCC" side.

On 2700 and LabSite , the lever should be bent as escaping ETI adapter.

<B> 777 <D><R>
This PPI adapter shares the same hardware ID as an another PPI.
To validate that you are working with the corrrect PPI, please
remove the PPI from the PPI-BASE and perform a Load operation.
The programmer will prompt you to install a specific PPI, please
validate that you are using the PPI called out by the programmer.
<B> 778 <D><R>
-
<B> 779 <D><R>
When trying to perform a write operation on the device, the address
range should be between 4000H and 7FFFH.If performing a write operation
between 0000H and 7FFFH,the addresses 0000H to 3FFFH should be filled
with FFH.
<B> 780 <D><R>
-
<B> 781 <D><R>
-
<B> 782 <D><R>
-
<B> 783 <D><R>
-
<B> 784 <D><R>
-
<B> 785 <D><R>
Device Block Protection can be enabled as follows:

Security Fuse			Block Protect Start Addresses	
SF3	SF2	SF1	25P40	25P80
0	0	0	none	none
0	0	1	$70000 - $7FFFF	$F0000 - $FFFFF
0	1	0	$60000 - $7FFFF	$E0000 - $FFFFF
0	1	1	$40000 - $7FFFF	$C0000 - $FFFFF
1	0	0	$0 - $7FFFF	$80000 - $FFFFF
1	X	1	$0 - $7FFFF	$0 - $FFFFF
1	1	X	$0 - $7FFFF	$0 - $FFFFF

<B> 786 <D><R>
Four levels of "BLOCK PROTECT" can be implemented for these devices:

Security Fuse Settings				Corresponding Block Protect Addresses		
				25040/043 25LC/AA040	25080; 95080 25LC/AA080	
SF2	SF1	95010	95020	25020 95040	25C040	25C080 25C08; 95P08
0	0	None	None	None		None

```
   0         1        $60->$7F  $C0->$FF     $180->$1FF   $300->$3FF
   1         0        $40->$7F  $80->$FF     $100->$1FF   $200->$3FF
   1         1        $00->$7F  $00->$FF     $00 ->$1FF   $00 ->$3FF


                      25160; 25C160
                      25160; 25C160  25320/C320  25640/LC640
                      25LC160/AA160  25LC320     25AA640
                      24165; X5163   25C32       25C64
  SF2       SF1       25C16; 95160   95320       95640
-------------  -----------   ----------  --------
   0         0        None           None        None
   0         1        $600-7FF       $C00-FFF    $1800-1FFF
   1         0        $400-7FF       $800-FFF    $1000-1FFF
   1         1        $0-7FF         $0-FFF      $0-1FFF


                      25128/C128  25256/C256  25P1024
  SF2       SF1       95128       95256       25P10/A(NEE)
-------------  ----------   ----------  ------------
   0         0        None        None        None
   0         1        $3000-3FFF  $6000-7FFF  $18000-1FFFF
   1         0        $2000-3FFF  $4000-7FFF  $10000-1FFFF
   1         1        $0-3FFF     $0-7FFF     $00000-1FFFF


  SF2       SF1       25P05/A(NEE)  25P20(NEE)
-------------  ------------  -----------
   0         0        None          None
   0         1        $0-FFFF       $30000-3FFFF
   1         0        $0-FFFF       $20000-3FFFF
   1         1        $0-FFFF       $0-3FFFF
```

Enabling the "Erase EE device" option will remove all block protection.

Electrically Erasable PROMs automatically perform an erase operation
during the program operation, therefore, "Erase EE device" is only
required if you are removing all block protection.

NOTE: Devices with the flag "NEE" are NOT Electrically Erasable PROMs,
and require "Erase EE device" option to be enabled when re-programming.
<B> 787 <D><R>
-
<B> 788 <D><R>
This device contains an Electronic ID. If an ID error occurs one of the
following issues may be the cause: The wrong device has been selected,
or the device may NOT be properly positioned in the socket, or you may
have a new version of this device that is not yet supported. Please
contact your Customer Support Representative for more information.

NOTE: If "Compare elec ID" flag is available, it must be enabled(set to "Y")
<B> 789 <D><R>
-
<B> 790 <D><R>
The available program area is "4000 hex - 13FFF hex".
The data in all other areas should be set to "FF".

```
Device address          data
-------------------     ---------
 0000 -  3FFF hex       all FF
```

```
   4000 - 13FFF hex          user data


<B>  791  <D><R>
The device memory space is partitioned as follows :


        ARRAY           TYPE             ADDRESS
     ------------    ------------    ------------
  XROM Space     PROGRAMMABLE         0- 5FFF hex
  RESERVED       UNPROGRAMMABLE   6000- FFFF hex    ignored user data
  YROM Space     PROGRAMMABLE    10000-15FFF hex
  RESERVED       UNPROGRAMMABLE  16000-1FFFF hex    ignored user data


Please refer the manufacturer's data book.
<B>  792  <D><R>
This device contains 3 arrays:
EPROM    64Kbytes      00000-0FFFF  HEX
OSDL     4Kbytes       10000-10FFF  HEX
OSDH     4Kbytes       11000-11FFF  HEX


The OSDH upper nibble(4-bits) is not verified and will always
be programmed to F HEX by the programmer.
<B>  793  <D><R>
Pin 15
Pin 38
<B>  794  <D><R>
PPI-0541 is for the QFP in its carrier
PPI-0545 is for the QFP without its carrier with formed leads. Insert
the device leads up (dead bug).
<B>  795  <D><R>
-
<B>  796  <D><R>
This part has two EPROM rows (0 & 1).  The rows are selected by the
configuration bit in the programming screen.  N = row 0,  Y = row 1.
All operations will be done on the selected row.  Bit 34 is forced
to 0 if row 0 is selected and 1 if row 1 is selected regardless of
the data file (possibly reporting a check sum error on verifies).
When row 1 is selected during a program operation, Row 0 bit 34 is
set. Once row 1 is programmed, the data in row 0 will not be used
in the device operating mode.  Bit 36 (reserved) is forced to 0
when programming, regardless of the data file (possibly reporting
a check sum error on verifies).  Bit 33 (Valid) is only set by the
data file.  If not set, the EPROM tuning cap bits are not used in
operating mode (the shadow register data selects the caps).


Bit 29 is recommended low.
<B>  797  <D><R>
Use only JEDEC Format #91(Full Jedec).
<B>  798  <D><R>
This device contains 2 arrays:
System EPROM            64Kbytes      00000-0FFFF  HEX
Character EPROM(OSD)    4Kbytes       10000-11BFF  HEX


The Character EPROM array from address 11600 HEX to 11BFF HEX needs to
be programmed to either 0x00 or 0xFF.


Warning! The programmer will display a checksum at the end of a file
download and again at the end of a programming operation (when there is
```

no error detected). So when the user changes the RAM content in between
these operations the two checksums may not remain the same. To
avoid this problem set the bytes from address 11600 HEX to 11BFF HEX
to either 0x00 or 0xFF in the file before download, this will ensure
consistent checksums throughout.
<B> 799 <D><R>
-
<B> 800 <D><R>
-
<B> 801 <D><R>
This device has Clock Configurations Bytes. The Clock Configuration bytes
are located in RAM address locations dictated in the Manufacturer's Device
Specification sheet or data sheet; for the specific addresses of these bytes
please refer to the data sheet. To program the Clock Configurations bytes:

In Hiterm: Enable the "Reset Clock" flag to "Y" in the PROGRAM DEVICE screen.

In TaskLink: Enable the "Special Data" flag/check box in the GENERAL
PARAMETER Dialog Box.

NOTE: When the "Stop bit" of this device is NOT set the clock will be free
running. This means that the value of the clock data is updated during each
Load operation. This also means that if you perform a "Verify Only"
operation you will get verify errors on the bytes that store the free running
clock data.
<B> 802 <D><R>
Any of the three security options can be implemented for this device
(Encryption Array data, Security Bit 1 or Security Bit 2). You can
select the security options from the PROGRAM DEVICE Options screen.
Once any of the security options have been programmed into the device,
no further programming is allowed.

Illegal operations will generate one of these error messages:

A. Encryption Array Already Programmed - A programming operation has
been attempted after the Encryption Array has been programmed.

B. Security Fuse Programmed or Bad Device - A programming operation
has been attempted after security bit 1 has been programmed.

C. Security Fuse Violation - A programming operation has been
attempted after security bit 2 has been programmed. This error will
also be generated for a load or verify operation.

D. Test Fuse Programming Error - This error will be displayed
if there is a programming error in the Encryption Array.

Data in the programmer's User Memory is partitioned as follows:

  MAIN ARRAY DATA   0 through FFF hex
  ENCRYPTION ARRAY DATA   1000 through 101F hex

Enter Encryption Array data by editing the appropriate address in User
Memory.

After the Encryption Array is programmed, device data will no longer
match data in User RAM. Encryption Array and Security Bit data cannot

be read from the device.
<B> 803 <D><R>
Partial device operations are not allowed on this device.
<B> 804 <D><R>
-
<B> 805 <D><R>
If your data file is smaller than the device size, make sure
that the extra locations in User RAM are filled with the blank
state(00 hex).
<B> 806 <D><R>
To use socket adapter, extend leads by 20mm.
<B> 807 <D><R>
The available program area is "2000 hex - 11FFF hex (in words)".
The data in all other areas should be set to "FF".

Device address (in words) data
------------------------- ---------
 0000 - 1FFF hex   all FF
 2000 - 11FFF hex   user data

<B> 808 <D><R>
The algorithm supports individual sector control for program, Erase and
protection. Use flags "Erase", "Program" and "Protect" corresponding to
each sector.
1. When "Erase" flag of any sector is set to "YES" then irrespective
   of protect status, at next erase operation the sector will get erased
   and protect status will become "Unprotected".
2. After Programming the protect status will be set to the "Protect status
   flag" value.
3. The "Load" operation reads the protect status and updates the Protect
   status flags.
4. Programming a protected sector is not allowed. Attempting to program
   a protected sector may produce a programming error.
<B> 809 <D><R>
-
<B> 810 <D><R>
Pin 22
<B> 811 <D><R>
The selected device has a non-programmable area,
address 0000 through 5FFF hex.

The user data for this location should be set to FF hex.
Or set the device begin address to 6000 hex and the
device block size to 2000 hex.

Refer to device spec sheet for more information.
<B> 812 <D><R>
-
<B> 813 <D><R>
-
<B> 814 <D><R>
The device name on the package is same as 64F3062F.
But the package of selected device is QFP-100B, it is not same as 64F3062F QFP-1
00A.
Please confirm the marked "RBL" by the device name on the package.
<B> 815 <D><R>
-

```
<B>  816  <D><R>
-
<B>  817  <D><R>
This algorithm's checksum calculation procedure matches the
semi manufacturer's programming tool and specifications. In
TaskLink, the "Use Algorithm Checksum" flag must be enabled.
<B>  818  <D><R>
-
<B>  819  <D><R>
Pin G4
<B>  820  <D><R>
-
<B>  821  <D><R>
-
<B>  822  <D><R>
The device name on the package is same as non V version device.
But the selected device is for the low voltage, you can not use this
on the non V device. Please confirm the marked "V" by the device name
on the package. It is marked near the device lot number.
<B>  823  <D><R>
This device does not support individual sector protect.
Hence if any one of the sector is protected entire chip
gets protected.
<B>  824  <D><R>
The available program area is "4000 hex - 23FFF hex".
The data in all other areas should be set to "FF".

Device address                data
-------------------           ---------
 0000 -  3FFF hex             all FF
 4000 - 23FFF hex             user data
<B>  825  <D><R>
OTP Protection Register data is located in the last sector
of the "Device Configure" table. This Protection Register
sector has a default setting of No for the Programming
and/or Protecting device operations.
<B>  826  <D><R>
Device requires OKI's socket adapter SOCKET48T-48.
<B>  827  <D><R>
Before downloading your data, fill the Programmers User Memory with
00h. To do this, use the FILL RAM option under the MORE-EDIT screen.
<B>  828  <D><R>
Devices 89F54 and 89F58 will be always erased entirely
independent of device configuration.

The checksum for these devices will be affected by
the data in the hole in user memory.
-----------------------------------------
              89F58               89F54
-----------------------------------------
Block 0     $0000-$7fff       $0000-$3fff
Hole        $8000-$efff       $4000-$efff
Block 1     $f000-$fffe       $f000-$fffe
-----------------------------------------

Location $ffff is used to protect block 0 and block 1.
Protecting block 0 will automatically protect block 1.
```

<B> 829 <D><R>
Encryption array, lock bit, and configuration byte programming are all
supported on this device. These features can be enabled from the Program
Device screen. The encryption array and configuration bytes have data in
User Memory.

```
                              87251G2D          87251G1A
                              ---------         ----------
  MAIN ARRAY DATA             0-7FFF hex        0-3FFF hex
  ENCRYPTION ARRAY DATA       8000-807F hex     4000-407F hex
  CONFIGURATION BYTES         FFF8-FFF9 hex     4080-4081 hex
```

Note that these values are all offsets from the memory begin address
field located in the PROGRAM DEVICE options screen. If the memory
begin address is not zero (default) , add the value in this field to the
offset for the appropriate address. Also note that to program special
features, enter data at the appropriate memory locations, and set
the corresponding field in the PROGRAM DEVICE options screen to "Y."
Enabling the security fuses programs the lock bits, "Program XNOR data"
programs the encryption array, and "Program Configuration" programs the
configuration bytes.

After the Encryption Array is programmed, device data will no longer
match data in User RAM. After programming security bits, programming
operations are no longer allowed.
<B> 830 <D><R>
-
<B> 831 <D><R>
-
<B> 832 <D><R>
-
<B> 833 <D><R>

The Write Protect Register is programmed with the address value of
the first word that is to be protected. All address values equal
to or greater than the value contained in the Protect Register will
be protected from further writes (unless erased). The value of the
Protect Register can be specified by editing the User RAM location
listed in the table below:

```
     DEVICE       RAM Location     Maximum Value
     --------     ------------     -------------
     93S46          40 hex          003F hex
     93S56          80 hex          007F hex
     93S66         100 hex          00FF hex
```

The contents of the Protect Register will NOT be programmed
unless the Protect flag for the main array is set to "Y" in
the "Device Configure" screen.

The content of the Protect Register may be secured from any
future writes permanently by setting the Protect flag for the
protection address to "Y" in the "Device Configure" screen and
the Program Security Fuse option set to "Y" in the "Program
device" screen.

<B> 834 <D><R>
-
<B> 835 <D><R>
This device requires the use of 0.1uF bypass capacitor(s). Use
Data I/O P/N 615-1832-001, supplied with your PPI adapter kit.
NOTE: If you are currently using a MatchBook hardware solution to
program your device, you may need to move over to the corresponding
PPI base and PPI adapter programming solution, if available. Please
contact Data I/O customer support for details.

Plug the bypass capacitor(s) into the following pins on the
receptacle of your PPI adapter board:
<B> 836 <D><R>
For correct operation of this device programmer must have at
a minimum 8 MEG RAM.
<B> 837 <D><R>
-
<B> 838 <D><R>
Software Data Protection will be disabled in Erase operation.
<B> 839 <D><R>
PINS 8, 21, 22
<B> 840 <D><R>
Place jumper POS2 on DIO socket adapter for this device.
<B> 841 <D><R>
Place jumper POS1 on DIO socket adapter for this device.
<B> 842 <D><R>
-
<B> 843 <D><R>
-
<B> 844 <D><R>
Customers using the MatchBook hardware configuration and are
experiencing errors during device operations may need to switch
to the corresponding PPI base and PPI adapter for better yield.
<B> 845 <D><R>
The Sector or Block protection feature of this device is a one time
programmable operation. Once these sectors or blocks are protected
the algorithm will not be able to un-protect these sectors or blocks.
If you re-program a device that has had sectors or blocks previously
protected, you will receive programming or verify errors.
<B> 846 <D><R>
-
<B> 847 <D><R>
This device has a complex security schema; See application note for details.
<B> 848 <D><R>
The Protection state of the last sector in this device is a One Time
Programming operation(OTP Protection.) When re-programming this device,
if this sector has been previously protected, please make sure the the
individual sector "Program" flag is set to No.
<B> 849 <D><R>
Sector protection is programmed by blocks composed of one or more sectors,
please see manufacturers data sheet for more details regarding sector group
protection. Setting the sector protection flag for one sector in a sector
group will cause all sectors in that group to be protected.

Hiterm:
Sector protection flags for a sector group will toggle in unison if any
one sector in that group is set.

TaskLink:
Currently group protection can only be determined from a load operation
after performing a program/sector protection operation.
<B> 850 <D><R>
-
<B> 851 <D><R>
-
<B> 852 <D><R>
-
<B> 853 <D><R>
The device name on the package is same as A version device.
But the selected device is for the non A version, it is different
from the socket adapter for the A version's adapter. Please confirm
the non marked "A" by the device name on the package. If it is A version
device, it is marked near the device lot number.
<B> 854 <D><R>
The device name on the package is same as non A version device.
But the selected device is for the A version device, it is different
from the non A version's socket adapter. Please confirm the marked
"A" by the device name on the package. It is marked near the device
lot number.
<B> 855 <D><R>
-
<B> 856 <D><R>
Erase and Program algorithm temporary overrides sector protection. Entire chip
will get erased and programmed irrespective of Y/N settings under erase and
program options on MDD screen and existing sector protection status of the
sectors.
<B> 857 <D><R>
 '_N' at the end of the device name means a new algorithm
 that matches the memory mapping and the checksum calculation
 of the manufacturer's programming tool.
<B> 858 <D><R>
-
<B> 859 <D><R>
-
<B> 860 <D><R>
-
<B> 861 <D><R>
Security bit programming may be enabled in the
Program Memory Device Options screen.

For Programming encryption bytes of Winbond PART #:77E58-PLCC :
1. Program Memory Device Options ->Program XNOR data ->Y
2. Main menu ->More commands ->Edit data ->Edit memory
            ->Address 8001 and 8002 -> Type in Encryption Bytes
<B> 862 <D><R>
-
<B> 863 <D><R>
-
<B> 864 <D><R>
-
<B> 865 <D><R>
Steps for programming the fuse bits

1) Programming -> Program Configuration -> Y

```
2) More Commands -> Edit Data -> Edit Memory -> Jump To Address 800 (Hex)
   Bit 7 = Not Used
   Bit 6 = Not Used
   Bit 5 = Not Used
   Bit 4 = INTCAP Fuse
   Bit 3 = CKSEL3 Fuse
   Bit 2 = CKSEL2 Fuse
   Bit 1 = CKSEL1 Fuse
   Bit 0 = CKSEL0 Fuse


Steps for programming the lock bits

1) Programming -> Program Protect Reg -> Y
2) More Commands -> Edit Data -> Edit Memory -> Jump To Address 801 (Hex)
   Bit 7 = Not Used
   Bit 6 = Not Used
   Bit 5 = Not Used
   Bit 4 = Not Used
   Bit 3 = Not Used
   Bit 2 = Lock Bit 2
   Bit 1 = Lock Bit 1
   Bit 0 = Not Used
```
<B> 866 <D><R>
This device has a one time programmable boot block lockout feature,
enabled by setting the sector protect flag to Y for the boot sector.
The setting of the protect flags of all other sectors are ignored.
During erase and program operations, this boot sector lockout feature is
temporarily overridden, allowing the contents of the protected boot
sector to be altered.
<B> 867 <D><R>
The first and last sector in this device are erased together. If either
one of these sector's erase flag is set the Yes, the other sector will
be erased simultaneously.
<B> 868 <D><R>
The One Time Programmable (OTP) sector(s) will have their program flag set
to N (No) by default in the Sector Configuration Screen. This Program flag
controls the following device operations: Blank Check, Illegal Bit Check,
Program and Verify. To perform these operations this flag must be set to Y.
<B> 869 <D><R>
This device has three security options.
(Encryption Array, Security fuse 1, Security fuse 2).
These options can be set from "Program Device" menu.

A.Enter Encryption Array data into User Memory following the
Main Array data. Below is the memory partition information for
various devices:

```
               87C5101
               ------------
MAIN ARRAY    :    0 - 3FFFh
ENCRYPT. ARRAY: 4000 - 403Fh
```

Once Encryption Array is programmed, device data can not be verified.

B.Security fuse 1 will write protect the device.
C.Security fuse 2 will read/write protect the device.

```
<B>  870  <D><R>
-
<B>  871  <D><R>
 For new designs, please use the algorithm PIC16C64A_N.
 Use the algorithm without "_N" at the end of the device
 name when you need compatibility with the old data files.

 "_N" at the end of the device name means the  new algorithm
 that matches the checksum of the Microchip development tool.
 The positioning of the IDs and the Configuration words fully
 satisfies the Microchip specifications. Also, with the new algorithm
 the user can set or clear the BODEN bit in the Configuration
 register. The old algorithm clears the BODEN as a default.

 For more information about the PIC16C64A_N algorithm, check
 the file "mct_uc.txt" on the Data I/O Web Site or FTP site.
<B>  872  <D><R>
-
<B>  873  <D><R>
Adapter version B or greater is required.
<B>  874  <D><R>
-
<B>  875  <D><R>
Pin 37
<B>  876  <D><R>
Pin 1 of the device must be placed to the left side of the socket.
<B>  877  <D><R>
-
<B>  878  <D><R>
pin 13, 14, 15, 17, 27 and 28.
<B>  879  <D><R>
User memory from      0 to 0FFFF is mapped as Application ROM (APROM)
User memory from 10000 to 10FFF is mapped as Loader      ROM (LDROM)

For programming lock bits,

Program Memory Device Options -> Program Protect Reg. -> Y
and load user memory location 11000.

User memory location 11000 is used as follows :

Bit 0 : Lock Bit
Bit 1 : MOVC Inhibit Bit
Bit 2 : Encryption Bit
Bit 7 : Oscillator Control Bit


<B>  880  <D><R>
-
<B>  881  <D><R>
Pins 46, 37, 27
<B>  882  <D><R>
Altera EPM7096 comes in two variations, EPROM or EEPROM.  To figure out
which one you have please check the speed grade labeled on the device.
The EPROM (OTP) version is represented by -1,-2, or -3. The EEPROM
(electrically erasable) version is represented by -7, -10, -12, or -15.
Choosing the incorrect menu name will result in Electronic ID errors.
```

```
<B>   883   <D><R>
-
<B>   884   <D><R>
Devices 89C54 and 89C58 will be always erased entirely
independent of device configuration.

The checksum for these devices will be affected by
the data in the hole in user memory.
------------------------------------------
               89C58            89C54
------------------------------------------
Block 0       $0000-$7fff      $0000-$3fff
Hole          $8000-$efff      $4000-$efff
Block 1       $f000-$ffff      $f000-$ffff
------------------------------------------

Use Program device --> Program Sec Fuse 1 to program security bit 1
Use Program device --> Program Sec Fuse 2 to program security bit 2
Use Program device --> Program Sec Fuse 3 to program security bit 3

Use Program device --> Program configuration to program ReMap bits
Location $10001 Bit 0 is used for ReMap bit 0
Location $10001 Bit 1 is used for ReMap bit 1

<B>   885   <D><R>
Pins A14, A16, B5, B16
<B>   886   <D><R>
-
<B>   887   <D><R>
-
<B>   888   <D><R>
-
<B>   889   <D><R>
-
<B>   890   <D><R>
Device Memory Map:
Device Name  : T89C51RD2        T89C51RC2/IC2    T89C51RB2
------------   ---------------  ---------------  ---------------
Main Array   : 0x00000-0x0ffff  0x00000-0x07fff  0x00000-0x03fff
XAF          : 0x10000-0x1007f  0x08000-0x0807f  0x04000-0x0407f
HSB          : 0x10080          0x08080          0x04080

XAF-Extra Flash Memory
HSB-H/W Security Byte

To enable HSB programming set "program device"->
"program protect reg." option.

To enable XAF programming set "program device"->
"program configuration" option.

The memory map for XAF is:
Device Name             : T89C51RD2     T89C51RC2/IC2   T89C51RB2
-------------------       ----------     -------------   ---------
Boot status byte        : 0x10000       0x08000         0x04000
Software boot vector    : 0x10001       0x08001         0x04001
copy of HSB             : 0x10004       0x08004         0x04004
```

```
Software security byte  : 0x10005        0x08005          0x04005
Boot reference          : 0x10006        --NA---          --NA---
Copy of MID             : 0x10030        0x08030          0x04030
Copy of DID#1           : 0x10031        0x08031          0x04031
Copy of DID#2           : 0x10060        0x08060          0x04060
Copy of DID#3           : 0x10061        0x08061          0x04061
```

All the other addresses are reserved.
<B> 891 <D><R>
There is no sector protect function for this device.
<B> 892 <D><R>
-
<B> 893 <D><R>
-
<B> 894 <D><R>
This device requires a special DIP-to adapter.
Please contact Manufacturer for details.
<B> 895 <D><R>
-
<B> 896 <D><R>
This device contains a special sector(s) which may be referred to
by various manufacturers as a SecSi sector, or Hidden ROM, or
Protection Register. This specialty sector is not supported for
this device at this time.
<B> 897 <D><R>
Only the first and last sectors can be protected.
<B> 898 <D><R>
-
<B> 899 <D><R>
-
<B> 900 <D><R>
-
<B> 901 <D><R>

```
   The Configuration Bytes are located at following memory
   locations:
   --------------------------------------------------------------
   Device          Status Byte          Boot Vector Byte
   --------------------------------------------------------------
   89C51            1000 hex             1001 hex
   89C52            2000 hex             2001 hex
   89C54            4000 hex             4001 hex
   89C58            8000 hex             8001 hex
   89C51RC+         8000 hex             8001 hex
   89C51RD+        10000 hex            10001 hex
   89C51RB2         4000 hex             4001 hex
   89C51RB2H        4000 hex             4001 hex
   89C51RC2         8000 hex             8001 hex
   89C51RC2H        8000 hex             8001 hex
   89C51RD2        10000 hex            10001 hex
   89C51RD2H       10000 hex            10001 hex
   89C660           4000 hex             4001 hex
   89C662           8000 hex             8001 hex
   89C664          10000 hex            10001 hex
   89C668          10000 hex            10001 hex
   --------------------------------------------------------------
```
<B> 902 <D><R>
Memory Map in User Memory for ATtiny11

```
--------------------------------------

Flash  Memory : $000 To $3FF
Fuse Bits     : $400
Lock Bits     : $401 (Bits 1 and 2 for Lock Bit 1 and 2 respectively)

Steps for Programing Fuse Bits :
----------------------------

1) Use More Commands -> Edit Data -> Edit Memory -> Jump To Address $400

Bit Positions for :
----------------

0 = CKSEL0 Fuse
1 = CKSEL1 Fuse
2 = CKSEL2 Fuse
3 = RSTDISBL Fuse
4 = FSTRT Fuse
5 = Do not care
6 = Do not care
7 = Do not care

Steps for Programming Lock Bits :
-----------------------------

1) More Commands -> Edit Data -> Edit Memory -> Jump To Address $401
2) Programming -> Program Protect Reg -> Y
<B>  903  <D><R>
Pin B5
<B>  904  <D><R>
The STDCBGA menu name means CGBA package, standard pin definition,
least to most significant address lines are A-1,A0,A1...A18.
The ALTCBGA menu name means CGBA package, alternate pin definition,
least to most significant address lines are A0,A1...A19.
Refer to device data sheet for device package pin numbers.
<B>  905  <D><R>
Device must be bottom justified in the socket.
<B>  906  <D><R>
-
<B>  907  <D><R>
Consult the Manufacturer's specifications for further information.
<B>  908  <D><R>
Security bit format for this device is:
Program Security fuse 1: Lock Bit 1
Program Security fuse 2: Lock Bit 2
<B>  909  <D><R>
PPI-0709B (open top socket, recommended)
PPI-0709
<B>  910  <D><R>
Pin 28
<B>  911  <D><R>
These devices contain UES and Customer Configuration Data at the end of the
device main array.  The UES data is always the 4 bytes immediately following
the end of the device main array. The customer configuration data is the
byte immediately after the UES or byte 5 after the end of user data.
```

The following format is used for the UES data and the configuration byte:

18V04/V02:
UES Data memory location: 80000h->80003h/40000h->40003h:
Customer Configuration Data memory location: 80004/40004 hex:
Byte value 0x00: Parallel (Express/SelectMAP) Mode
Byte value 0x01:   Serial (Master/Slave) Mode

18V01/V512/V256:
UES Data memory location: 20000h->20003h/10000h->10003h/8000h->8003h:
Customer Configuration Data memory location: 20004/10004/8004 hex:
Byte value 0x01*: Serial (Master/Slave) Mode   CF set to D4
Byte value 0x02:   Parallel (Express/SelectMAP) Mode   default CF assignment
Byte value 0x03**: Serial (Master/Slave) Mode   default CF assignment
*(note: This option recommended for 20-pin packages in Serial Mode)
**(note: NOT valid on 20-pin packages)

After placing the configuration byte at the end of the UES data,
enable the "Program configuration" flag in the Program device screen.
<B> 912 <D><R>
There are two versions of this device manufactured by AMD. Some versions have
the protection state of the Boot Sectors as One-Time-Programmable (OTP).
Use the algorithm with _ENG suffix for programming the OTP-Boot-Sector-Devices.

<B> 913 <D><R>
Enable Program security fuse to lock the Boot Block(s).
Once a Boot Block is locked, it CANNOT be reprogrammed
or erased! Please consult manufacturers data sheet for
location of the Boot Block(s) in the device's memory map.
<B> 914 <D><R>
-
<B> 915 <D><R>
-
<B> 916 <D><R>
-
<B> 917 <D><R>
The flash memory segment numbers as described in the device data
sheet are different than the sector numbers shown on the Device
Configure screen, but the segments can be recognized by their
address ranges as shown on that screen. Be mindful that the
address ranges shown are in word mode. Multiply by 2 to convert
to byte mode addresses.
<B> 918 <D><R>
-
<B> 919 <D><R>
-
<B> 920 <D><R>
-
<B> 921 <D><R>
Pins 16, 32
<B> 922 <D><R>
Pin 32
<B> 923 <D><R>
Pins 25, 32
<B> 924 <D><R>
This device supports the following PPI adapters:
<B> 925 <D><R>

```
PPI-0536
PPI-0586
<B>  926  <D><R>
-
<B>  927  <D><R>
-
<B>  928  <D><R>
Pin 1 of the device must be placed in the upper right corner of the socket.
<B>  929  <D><R>
-
<B>  930  <D><R>
Device must be top justified in the socket.
<B>  931  <D><R>
For programming this device the adapter will require some modifications.
Please read the associated application notes for details.
<B>  932  <D><R>
-
<B>  933  <D><R>
These devices have programmable reset polarity.  In order to program the Reset
Polarity, a byte of configuration data must be set at the end of the Main
Array's Data in User Memory.  This configuration byte data must be set as
follows in order to program the correct Reset Polarity:
Byte Value = FF; Programs device with Active High Reset Polarity (Default)
Byte Value = 00; Programs device with Active Low Reset Polarity
   17V04:                 Memory Location 80000 hex
   17V02/17S300A:         Memory Location 40000 hex
   17V01/17S200A:         Memory Location 33400 hex
   17S50A/17S100A/17S150A: Memory Location 20000 hex
   17S15A/17S30A:         Memory Location 10000 hex
Place the configuration byte data at the end of Main Array data and then make
sure to enable the "Program configuration" flag in the Program device screen.
<B>  934  <D><R>
Data in the programmer's User Memory is partitioned as follows:

                87C1102A            87C1104A
                87C1202A            87C1204A
                87C1302             87C1304
              -------------       -------------
Main array:   0xF800-0xFFFF       0xF000-0xFFFF
Config 1  :        0x707F              0x707F
Config 2  :        0x707E              0x707E

To program the config bytes, set option

"Program Device->Program configuration" to "Y".

The configuration byte definitions are:

                  Config 1            Config 2
              --------------      --------------
Bit[0] -          RC_opt          4K/2K
Bit[1] -          Low_opt         unimplemented
Bit[2] -          Lock            unimplemented
Bit[3] -          Open DR         unimplemented
Bit[4] -          Open DR         unimplemented
Bit[5] -          POREN           unimplemented
Bit[6] -          unimplemented   reserved
```

```
Bit[7] -          unimplemented     reserved

Bit[2] of Config 1 is lock bit, which can only be programmed
by setting the "Program Security Fuse" option in the
"Program Device" screen to "Y".

Once this bit is programmed, following error message is flashed
if any operation is attempted on the device:
"Security Fuse Programmed or Bad Device"
<B>  935  <D><R>
-
<B>  936  <D><R>
The status register for this device is formatted as follows

    bit  7    6    5    4    3    2    1    0
  ------------------------------------------------------
         R    R    WD1  WD0  BL1  BL0  R    R

WD1,WD0 are watchdog timer bits.
BL1,BL0 are block lock protection bits.
R are read only bits.

   WD1    WD0          Watchdog Time-out
  ----------------   ---------------------------
    0      0             1.4 Seconds
    0      1             600 milliseconds
    1      0             400 milliseconds
    1      1             Disabled
To program the watchdog timer bits edit following ram location and
set the 'Program configuration' to 'Y' in the program device screen.
This option will not program the block protection bits.
Device                RAM location
-------               --------------
X5163                 800 hex


The LOAD DEVICE operation will also load the WD0,WD1,BL0 and BL1
bits from status register and they can be read from ram location
specified above.
Enabling the "Erase EE device" option will disable watch dog time-out.

<B>  937  <D><R>
-
<B>  938  <D><R>
Stand-alone VERIFY is an option for this device. The PROGRAM VERIFY occurs
during programming. This option will require Illegal Bit check be turn on.

<B>  939  <D><R>
-
<B>  940  <D><R>
These devices have customer configuration options.  This data
follows Main Array Data in User Memory.  The configuration byte
at this location must be set as follows to program the polarity.

17V08: Memory Location 100000h:
17V016:Memory Location 200000h:
```

```
Byte = FF: Active High Reset Polarity, Express Mode Disabled, No Busy Pull-down
Byte = F1: Active High Reset Polarity, Express Mode Disabled, Busy Pull-down
Byte = F2: Active High Reset Polarity, Express Mode Enabled, No Busy Pull-down
Byte = F3: Active High Reset Polarity, Express Mode Enabled, Busy Pull-down

Byte = 00: Active Low Reset Polarity, Express Mode Disabled, No Busy Pull-down
Byte = 01: Active Low Reset Polarity, Express Mode Disabled, Busy Pull-down
Byte = 02: Active Low Reset Polarity, Express Mode Enabled, No Busy Pull-down
Byte = 03: Active Low Reset Polarity, Express Mode Enabled, Busy Pull-down
```

After placing the configuration byte at the end of Main Array data,
enable the "Program configuration" flag in the Program device screen.
<B> 941 <D><R>
Pin 20
<B> 942 <D><R>
-
<B> 943 <D><R>
1
<B> 944 <D><R>
Below is the memory partition information for the device:

```
                             DS2502
                             ----------
Main Array               : 0x00-0x7f
ROM bytes                : 0x80-0x87
Security Byte            : 0x88
Status bytes             : 0x89-0x8f
```

To enable status bytes programming, set
"program device"->"program configuration" option to "Y".

To enable security byte programming, set
"program device"->"program protect reg." option to "Y".
<B> 945 <D><R>
These devices have Illegal Bit Check and Blank Check enabled by default.
To speed up programming time, disable these flags in the program options
screen.
<B> 946 <D><R>
PPI-1206 (recommended)
PPI-1201
<B> 947 <D><R>
In case you get the error
"Device specific failure:cannot synchronize to device" or
"No presense pulse detected", please check the device is
inserted properly into the socket and try again.
<B> 948 <D><R>
_2 uses PPI-0529 (recommended)
_1 uses PPI-0505
<B> 949 <D><R>
_1 Menu Selection: PPI-3524 (recommended)
_2 Menu Selection: PPI-3525
<B> 950 <D><R>
_1 Menu Selection: PPI-1210 or PPI-1209(2900 only)
_2 Menu Selection: PPI-1203
<B> 951 <D><R>
Pin 14
<B> 952 <D><R>

-
<B>   953   <D><R>
-
<B>   954   <D><R>
-
<B>   955   <D><R>
-
<B>   956   <D><R>
-
<B>   957   <D><R>
Pin 23
<B>   958   <D><R>
Pin 27
<B>   959   <D><R>

Data in the programmer's User Memory is partitioned as follows:

  MAIN ARRAY DATA   0000 hex - 1FFF hex
  ENCRYPTION ARRAY DATA   2000 hex - 203F hex

 To program the Encryption Array, enter the encryption data at locations
 2000 hex - 203F hex in the Programmer User RAM and set the field "Program
 XNOR Data" in the PROGRAM MEMORY DEVICE screen to "Y".
 After the Encryption Array is programmed, device data will no longer
 match data in User RAM.

 To program the Lock Bits, set fields "Program security fuse" to
 desired state. "Y" means that the lock bit will be blown.
 After programming security bits, programming operations are no
 longer allowed.

 To enable the Watchdog Reset function in the Option Register set
 the "Program configuration" field to "Y".
 Watchdog Timer data cannot be read from the device.
<B>   960   <D><R>
-
<B>   961   <D><R>
With this version of software this device must now use PPI-0265. PPI-0227 is
only compatible with software versions up to and including V6.7.
<B>   962   <D><R>
Pins 1,2,27
<B>   963   <D><R>
pin 32, 50, 65, and 66.
<B>   964   <D><R>
Adapter version B or greater is recommended for this device.
<B>   965   <D><R>
-
<B>   966   <D><R>
Pins 1, 28
<B>   967   <D><R>
-
<B>   968   <D><R>
-
<B>   969   <D><R>
The pin adapter for this device requires an adapter orientation where the
clamshell opens facing the rear of the programmer.
<B>   970   <D><R>

If programming errors occur, use PPI-5205.
<B> 971 <D><R>
-

<B> 972 <D><R>
-
<B> 973 <D><R>
pin 27, 32, 50, 65, and 66.
<B> 974 <D><R>
-
<B> 975 <D><R>
-
<B> 976 <D><R>
-
<B> 977 <D><R>
-
<B> 978 <D><R>
-
<B> 979 <D><R>
Pins 9, 17, 29, 41
<B> 980 <D><R>
Pins 27, 37, 46, 47
<B> 981 <D><R>
During the erase operations, if any of the sectors are previously
protected, it is necessary to erase the lowest Quadrant (L/A0) first.
<B> 982 <D><R>
Enable Software Data Protection by enabling Program security fuse flag.
<B> 983 <D><R>
-
<B> 984 <D><R>
-
<B> 985 <D><R>
pin 11, 32, 50, 51, 65, and 66
<B> 986 <D><R>
-
<B> 987 <D><R>
-
<B> 988 <D><R>
-
<B> 989 <D><R>
-
<B> 990 <D><R>
pin 5, 14, 16, 33, and 47
<B> 991 <D><R>
-
<B> 992 <D><R>
Pins 12, 23, 37
<B> 993 <D><R>
OKI 27V6466-L-TSOP(2) treats lower 32M bit device block.
OKI 27V6466-U-TSOP(2) treats upper 32M bit device block.
For full-programming, two operations are required.

For using on UniSite with Site48HS, extend adapter leads by 15mm.

For using on 3900 with 39BASE-0101 and 2900 with 29BASE-0102,
bend lever to either side.

For using on ChipLab/2700/LabSite, set user memory size
to more than 4096 bytes. Memory buffer size greater than
512 bytes is recommended. Bend lever to either side.
<B> 994 <D><R>
Support of Power Down fuse is not available with this menu selection.
<B> 995 <D><R>
For more information, the following application notes(or files) can be
downloaded from the Data I/O Web Site or FTP site:

        amd_mem.txt ---- for AMD FLASH memory devices
        atm_mem.txt ---- for Atmel FLASH memory devices
        fuj_mem.txt ---- for Fujitsu FLASH memory devices
        int_mem.txt ---- for Intel FLASH memory devices
        shp_mem.txt ---- for Sharp FLASH memory devices
        spa_mem.txt ---- for Spansion FLASH memory devices
        stm_mem.txt ---- for STMicroelectronics FLASH memory devices
        mti_mem.txt ---- for Micron FLASH memory devices
        4meg_mem.txt ---- for Multi-menu named memory devices

These files will be updated periodically. To download the files use:
ftp://ftp.dataio.com/appnotes/
<B> 996 <D><R>
NOTE: Calibration Byte programming Address MUST be set to FFFFFFFF hex to
       AVOID programming the "Oscillator Calibration Byte" into the Main
       Array or EEPROM Array of the device! See Application Notes for details.
<B> 997 <D><R>
-
<B> 998 <D><R>
-
<B> 999 <D><R>
-