



Leaders in device programming, copying, simulation

TECHNICAL CONFERENCE 88

MR MOSTERDIJK

**ELAN MODELS
3000, 4000 & 5000
TECHNICAL
SUMMARY**

KEY FEATURES

GENERAL

Extensive use of Surface Mounted Devices.

Increased Reliability, due to fewer contact problems.

Increased component density.

Compact PCB layout.

Extensive use of ASICs.

Economical and secure implementation of special functions.

Proprietary information remains secure.

Reduced component count.

Master control Unit

CPU - Zilog Z80180.

Built in features include:-

On chip memory management unit.

On chip DRAM Controller.

1M byte directly addressable memory.

64k byte I/O space.

Two DMA channels.

Two full duplex serial ports.

On chip clock generator.

Static RAM.

4k bytes of battery backed RAM.

Used as workspace and to save Configuration settings.

Dynamic RAM.

256K increments up to 2Mbytes.

Keyboard.

Membrane Keypad with Tactile Keys, giving positive feel of operation.

Polled by CPU.

Display.

Alphanumeric Liquid Crystal Display.

2 X 16 Character lines.

NOTE:-

Details on this page are not applicable to the Model 3000

D/A Converter.

Multiplexed with sample and hold for Vcc, Vpp, current monitor and voltage monitor reference settings.

Only one calibration adjustment for all voltage and current settings.

Vpp & Vcc Power Drive.

Closed Loop control of both Vcc and Vpp with feedback from ZIF Sockets, resulting in no voltage droop due to differing numbers of devices inserted in sockets.

ES-PER ASIC

Hardware control of Data flow.

Modifies Data flow according to selected Data word size.

Power Supply Unit.

Switched mode design - Allows compact circuit and efficient, power saving operation.

Included on MCU PCB.

Crowbar overvoltage protection - Avoids damage to circuits should PSU fail to regulate supply.

Power fail detect. - Interrupt to CPU causes system to power down cleanly and save configuration.

ZIFPAC

Vcc & Vpp Monitors.

Programmable Voltage reference for both Vcc & Vpp.

Voltage Monitor polled by CPU.

Programmable Current limiting for both Vcc & Vpp.

Current Monitor generates interrupt to CPU in event of over current detection.

Socket Address

Latching buffer to socket address pins.

Socket address constantly monitored.

Socket Data.

Bi-directional latching buffers to socket data pins.

EF-PER ASIC

Hardware implementation of ancilliary functions, normally performed by software. This allows a massive reduction in the time spent on pre and post programming operations.

Operation Modes:-

Blank Test.

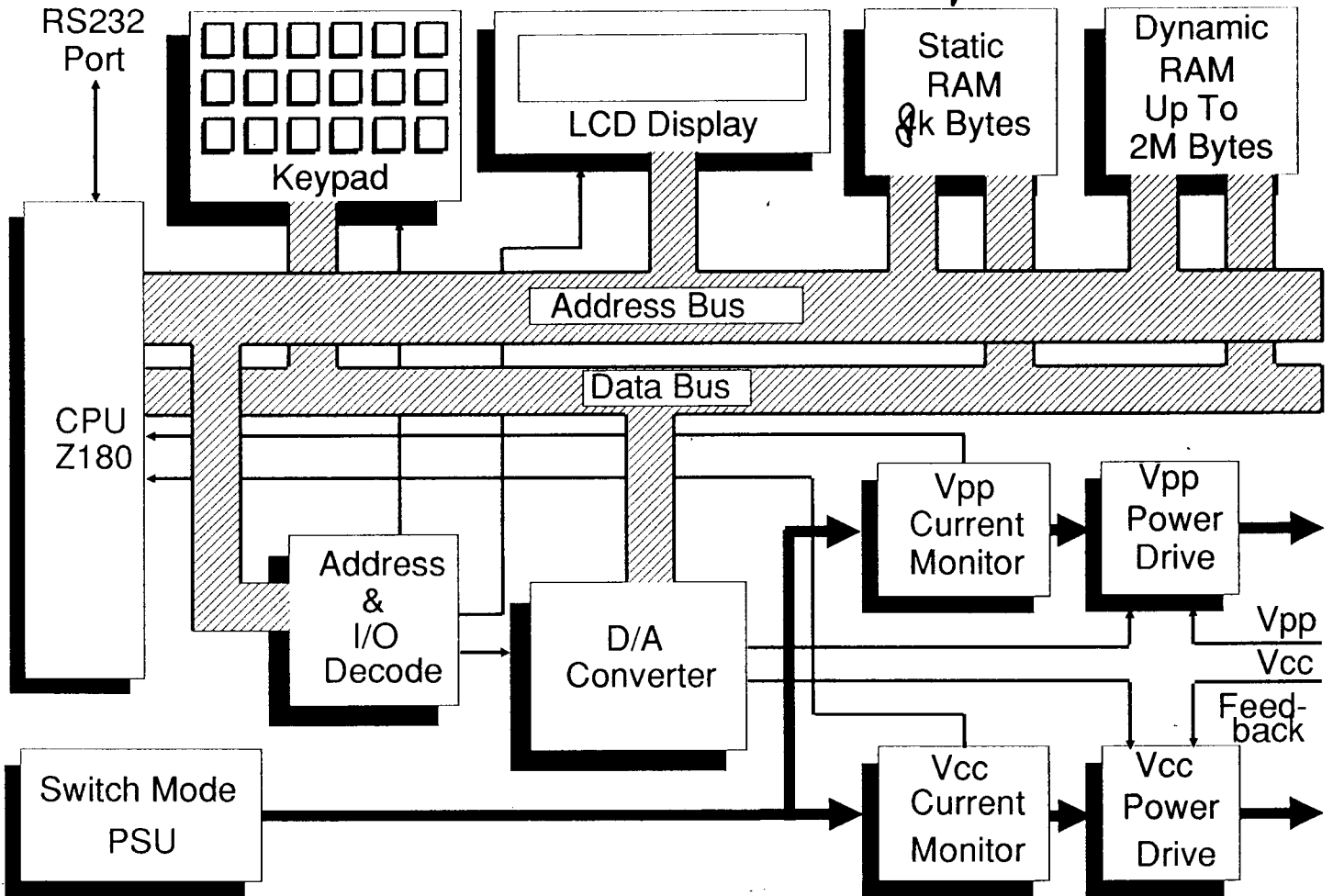
Illegal Bit Test.

Verify.

MCU

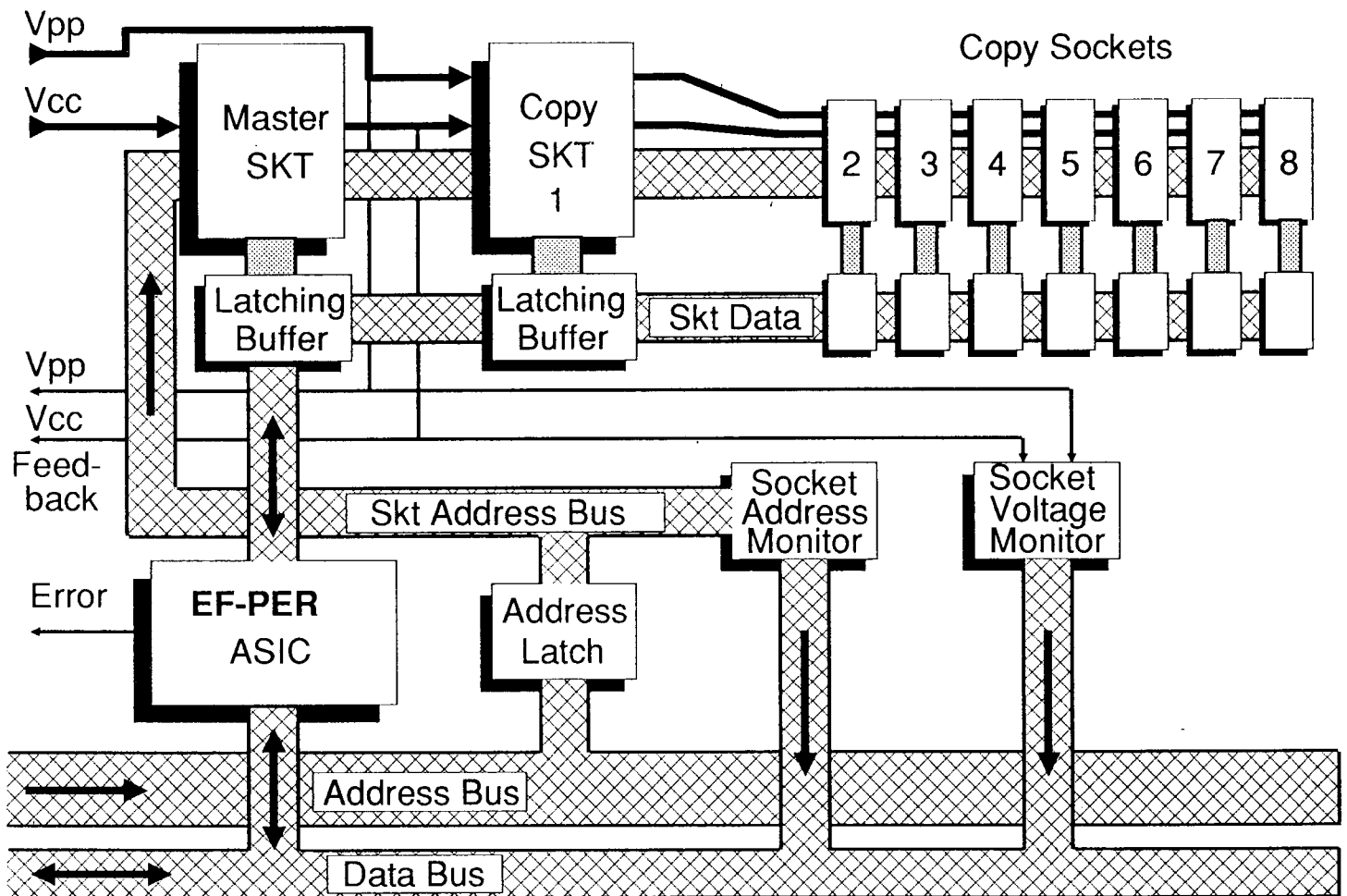
Functional Block Diagram

*add config mem -
firmware*



ZIFPAC

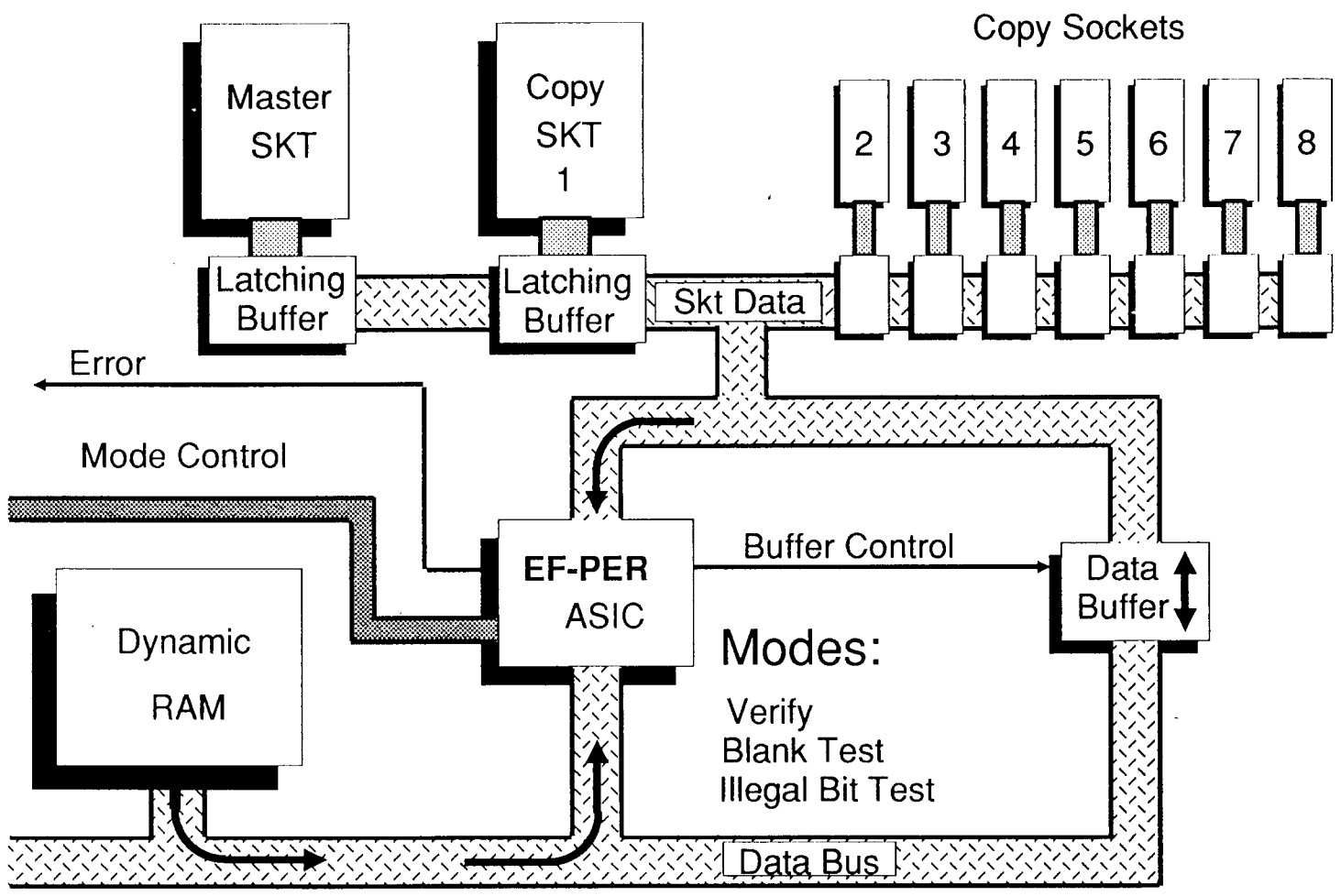
Functional Block Diagram.



ELAB
FORA
Program
Enhancement
Control

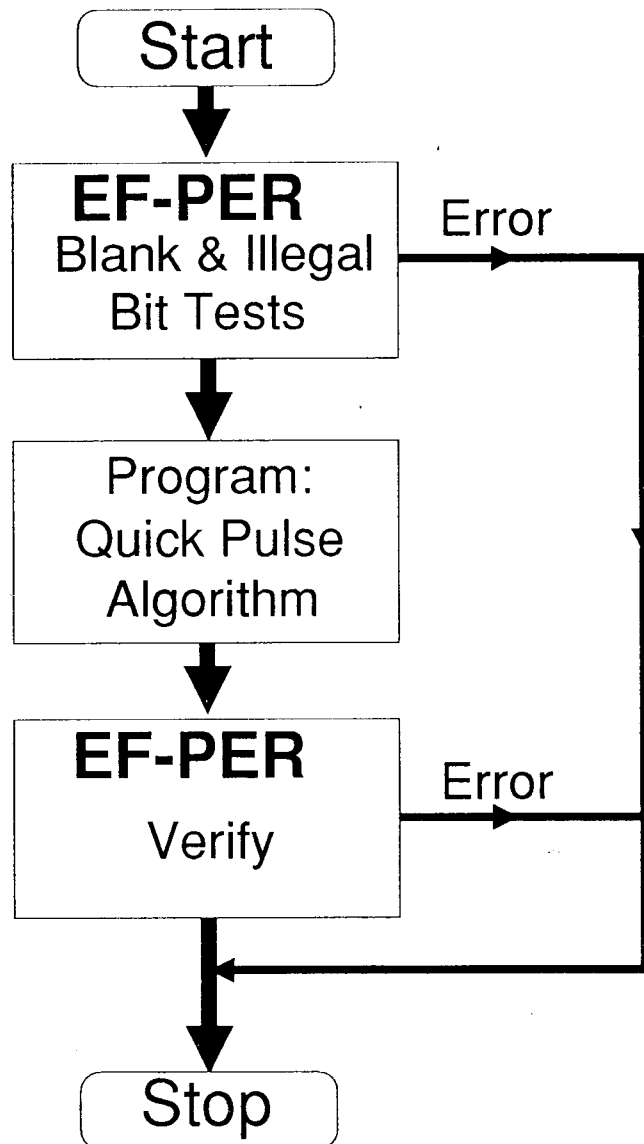
EF-PER

Functional Block Diagram.



EF-PER

Operation Flow Diagram



SKT

ES-PER

532 / 5832 / module

Functional Block Diagram.

