'E' Series Circuit Description

CONTENTS

Clock, Micro-processor & Buffers

IC1 and associated circuitry generates a 2.4 576 MHz crystal controlled clock signal which is used to clock the micro-processor and the baud rate generator on the interface board (where fitted). The micro-processor IC2 is a Z80. The data bus is buffered by IC6 a bi-directional buffer. The data direction is controlled by BRD. IC3,4 & 5 uni-directional buffers buffer the Address Bus and BWR, BRC signals.

Address Decoder, Internal EPROM and Scratchpad RAM.

One section of IC7 decodes the available 64K of addressing into two 32K sections:-

0000 to 7FFF	EPROM & Scratchpad RAM	
8000 to FFFF	External RAM Enable	(RAM)

The other section of IC7 decodes the first 32K address section into four 8K sections:-

0000 to 1FFF	First EPROM	IC8
2000 to 3FFF	Second EPROM	IC9
4000 to 5FFF	Third EPROM	IC10
6000 to 7FFF	Scratchpad RAM	IC11 *

* Only 2K of Scratchpad RAM fitted address 6000 to 67FF supported by Nickel Cadmium battery on PSU board .

The outputs of IC7 control the chip enable of EPROM and Scratchpad RAM selecting one device for a read or write operation in conjunction with BRD or BWR signals.

Port Decoder & latches

IORQ, BRD, BRW signals are gated to produce an I/O write or an I/O read signal which enables pin 1 or 15 of IC12 the port sector decoder. IC12 decodes the I/O port address into four input sections (pins 4,5,6,7) or four output sections (pins 12,11,10,9) all active low. These sections are further decoded where necessary by IC13 (chip select decoder), IC14 (Various input ports), IC15 and IC16 (Various output ports).

Where data outputed to a port has to be stored it is held in latches (IC17,18,19,20).

Chip select decoder

IC13 selects one of the eight Copy sockets during a copy socket read. IC 21C,D selects the Master Socket during a master socket read.

Address Latch.

IC26,27 latch the Port 00 and Port 01 data which is the socket Address LSB and MSB respectively. A common 00 Read signal or a latched Address/Data control signal enables the tri-state outputs of IC26,27.

Variable Access Time Control

The tACC or access time of the EPROM is defined as the time taken for the EPROM to output correct data after the selected address is stable. In the 'E' Series programmers the read strobe is used to enable the Address latch (see above) and from this period of valid address a timing 'window' is generated by a monostable IC34. The period of the pulse generated by the monostable is determined by an R.C time constant. The C content is fixed in C9 but the resistance can be selected via multiplexer IC33. One of eight resistors is selected by the ABC inputs.

It is therefore possible with software control to start off with a wide open 'window', check that the data is read correctly and progressively close the 'window' until the EPROM gives incorrect data.

The output of the monostable enables a transparent latch IC35 on the common Socket Data Bus. IC31A permits the automatic overiding of the Access Time facility when reading the master socket.

Data Latch

IC36 latches the data to be programmed into the EPROMS. This has tri-state outputs controlled by the Latched Address/Data Control signal.

Interface Circuits

Various gates, transistors and relays perform multiplexing or level shifting functions for the multi-use pins on Copy and master sockets.

For EEPROMS a ware shaper circuit centred around IC37 conditions the rise and fall times of Upp.

Relays 2 and 3 each 4 pole change over contacts swtich the pin 20's of the Copy sockets between Chip Select function or Upp (Intel 2732, 2732A and Mostek MK2764).

Display and Piezo Sounder

IC45 latches selection of Code B or Hex display formats on the Display and also drives the piezo sounder.

The 8 digit L.E.D. display is driven by IC44 a multiplexed display driven with internal RAM. IC42 latches the digit blanking (which is not available from IC44 with Hex display format). IC40,41 gate digit blanking to Common Cathode drive transistors Q48 to Q55. The L.E.D. display consists of two 4 digit 7 segment Litronix DL4770 displays.

Keyboard

IC43 inputs the eight push button switches onto the data bus when Port 10 is inputed.

Intelligent Identfier

Relay 5 and associated components permit intelligent interrogation of Eproms by switching Address 9 to +12v in accordance with Intel Specification . Earlier versions of Eproms do not have this facillity and may be destroyed by this action . Software will be incorporated at a latter date to make full use of Intelligent Interrogation when manufacturers produce suitable Eproms.

P.S.U. Monitor

A quad voltage comparitor IC48 is used to check the swtiched +5V level, 21V and 24V. IC50 outputs this data on to the data bus when PORT 12 is inputed.

P.S.U. Circuit

Mains Transformer

A toroidal mains transformer of the following specification is used in 'E' Series programmers :-

Input	Colour Code	Outputs	Colour Code
0v	Blue	0v	Red +
110v	Violet	8v 25mps	Red
120v	Brown		
		0v	Orange
0v	Blue *	24v 21Amp	Orange
110v	Violet *		
120v	Brown *		
Screen	Green/Yellow		

* Small yellow sleeve at transformer end identified this group of windings.
\+ Small white sleeve at transformer end identifies phase of secondary windings.

NOTE that later models have a different Primary Colour Code :- 0v Blue, 110v Violet, 120v White ; 0v Black, 110v Grey, 120v Brown.

+5v Supply

A conventional circuit using a bridge rectifier and series regulator. A switched +5v output is controlled by software to supply the EPROM sockets.

+25v/21v/12v Supplies

The 25v/21v supply is swtiched by Q1. The +12v supply is Fixed regulated by IC1. Q13,14 provide current limiting at 400mA .

Pins 22 Supply

Pins 22 of the EPROM sockets require a wide variety of supply voltages. Q2,3,4,5,6,7 and associated circuitry select 0v,5v,12v, 21v or 25v under software control.

L.E.D. indicators monitor:-

L.E.D.1	Unregulated +24v
L.E.D.2	regulated +12v
L.E.D.3	" " +21/25v
L.E.D.4	" " + 5v

Interface and Memory Board

This board has three functions:-

1. Hex-Keypad.
2. Serial RS232 Input/Output.
3. Random Access Memory.
4. Parallel Input/Output.

1. Hex-Keypad

IC15 an LSI Keyboard decoder chip enables the reading of the 16 hex keys and 4 function Key 5.

2. Serial RS232 Input/Output

The heart of the Serial I/O is the 6402 U.A.R.T IC18. IC13 an eight bit latch holds the baud rate selection (Bits 0,1,2,3) and the remaining bits are used to control parity, stop bits and clear the Data ready flag. IC11 is a four bit latch used to select 7 or 8 data bits and handshaking output Flags. IC10 accepts the master 2.4576 MHz clock and converts this to the required U.A.R.T clocking speed set by IC13. An external clock may also be selected e.g. the external clock generated by the cassette interface unit. This permits accurate tracking of the cassette unit increasing the integrity of operation.

IC18 converts the CMOS signal levels to RS232 levels (approx. +9v). Conversely IC19 converts the RS232 input levels to CMOS levels. The Clear to send and data set ready handshaking inputs are buffered through IC14.

IC17 converts the +12v supply to -9v to provide the negative bias on the RS232 Output lines.

3. Random Access Memory

A maximum of 16K bytes of RAM may be accomodated on the board (IC2,3,4,5,6,7,8,9). A minimum of 8K bytes is fitted (IC2,3,4,5). IC12 enabled by RAM selects one of eight 4016 RAM chips.

4. Parallel Input/Output

IC1 a Z80 P.I.O chip provides two 8 bit parallel I/O ports at T.T.L levels with handshaking control.