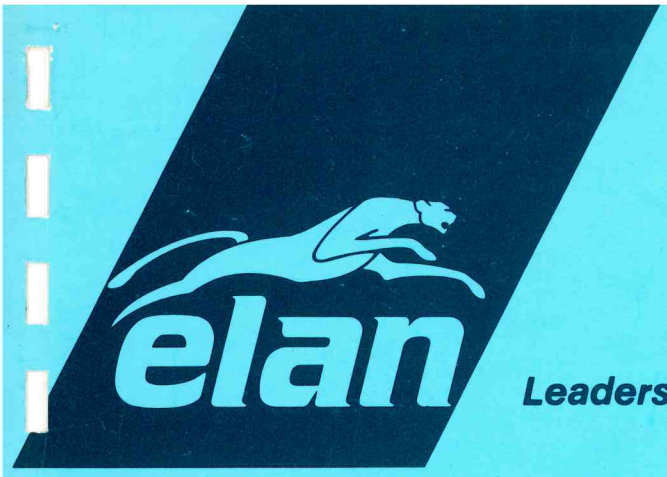


Leaders in device programming, copying, simulation

E-SERIES
MAINTENANCE MANUAL

Elan Digital Systems

'E' Series Circuit Description

CONTENTS

Clock, Micro-processor & buffers	PAGE 1
Address Decoder, Internal Eprom & Scratchpad Ram	"
Port Decode & Latches	"
Chip Select Decoder	"
Address Latch	PAGE 2
Variable Access Time Control	"
Data Latch	"
Interface Circuits	"
Display & Piezo Sounder	"
Keyboard	PAGE 3
Intelligent Identifier	"
P.S.U Monitor	"
P.S.U Circuit : Mains Transformer	"
: +5v Supply	PAGE 4
: +25v/21v/12v Supplies	"
: Pins 22 Supply	"
Interface & Memory Board	"
: 1. Hex-Keypad	"
: 2. Serial RS232 Input/Output	"
: 3. RAM	PAGE 5
: 4. Parallel Input/Output	"

Clock, Micro-processor & Buffers

ICI and associated circuitry generates a 2.4 576 MHz crystal controlled clock signal which is used to clock the micro-processor and the baud rate generator on the interface board (where fitted). The micro-processor IC2 is a Z80. The data bus is buffered by IC6 a bi-directional buffer. The data direction is controlled by BRD. IC3,4 & 5 uni-directional buffers buffer the Address Bus and BWR, BRD signals.

Address Decoder, Internal EPROM and Scratchpad RAM.

One section of IC7 decodes the available 64K of addressing into two 32K sections:-

0000 to 7FFF	EPROM & Scratchpad RAM	
8000 to FFFF	External RAM Enable	(RAM)

The other section of IC7 decodes the first 32K address section into four 8K sections:-

0000 to 1FFF	First EPROM	IC8
2000 to 3FFF	Second EPROM	IC9
4000 to 5FFF	Third EPROM	IC10
6000 to 7FFF	Scratchpad RAM	IC11 *

* Only 2K of Scratchpad RAM fitted address 6000 to 67FF supported by Nickel Cadmium battery on PSU board .

The outputs of IC7 control the chip enable of EPROM and Scratchpad RAM selecting one device for a read or write operation in conjunction with BRD or BWR signals.

Port Decoder & latches

IORQ, BRD, BRW signals are gated to produce an I/O write or an I/O read signal which enables pin 1 or 15 of IC12 the port sector decoder. IC12 decodes the I/O port address into four input sections (pins 4,5,6,7) or four output sections (pins 12,11,10,9) all active low. These sections are further decoded where necessary by IC13 (chip select decoder), IC14 (Various input ports), IC15 and IC16 (Various output ports).

Where data outputed to a port has to be stored it is held in latches (IC17,18,19,20).

Chip select decoder

IC13 selects one of the eight Copy sockets during a copy socket read. IC 32 selects the Master Socket during a master socket read.

Address Latch.

IC26,27 latch the Port 00 and Port 01 data which is the socket Address LSB and MSB respectively. A common 00 Read signal or a latched Address/Data control signal enables the tri-state outputs of IC26,27.

Variable Access Time Control

The tACC or access time of the EPROM is defined as the time taken for the EPROM to output correct data after the selected address is stable. In the 'E' Series programmers the read strobe is used to enable the Address latch (see above) and from this period of valid address a timing 'window' is generated by a monostable IC34. The period of the pulse generated by the monostable is determined by an R.C time constant. The C content is fixed in C9 but the resistance can be selected via multiplexer IC33. One of eight resistors is selected by the ABC inputs.

It is therefore possible with software control to start off with a wide open 'window', check that the data is read correctly and progressively close the 'window' until the EPROM gives incorrect data.

The output of the monostable enables a transparent latch IC35 on the common Socket Data Bus. IC31A permits the automatic overiding of the Access Time facility when reading the master socket.

Data Latch

IC36 latches the data to be programmed into the EPROMS. This has tri-state outputs controlled by the Latched Address/Data Control signal.

Interface Circuits

Various gates, transistors and relays perform multiplexing or level shifting functions for the multi-use pins on Copy and master sockets.

For EEPROMS a ware shaper circuit centred around IC37 conditions the rise and fall times of Upp.

Relays 2 and 3 each 4 pole change over contacts swtich the pin 20's of the Copy sockets between Output Enable function or Upp (Intel 2732, 2732A and Mostek MK2764).

Display and Piezo Sounder

IC45 latches selection of Code B or Hex display formats on the Display and also drives the piezo sounder.

The 8 digit L.E.D. display is driven by IC44 a multiplexed display driven with internal RAM. IC42 latches the digit blanking (which is not available from IC44 with Hex display format). IC40,41 gate digit blanking to Common Cathode drive transistors Q48 to Q55. The L.E.D. display consists of two 4 digit 7 segment Litronix DL4770 displays.

Keyboard

IC43 inputs the eight push button switches onto the data bus when Port 10 is inputed.

Intelligent Identfier

Relay 5 and associated components permit intelligent interrogation of Eproms by switching Address 9 to +12v in accordance with Intel Specification . Earlier versions of Eproms do not have this facillity and may be destroyed by this action . Software will be incorporated at a latter date to make full use of Intelligent Interrogation when manufacturers produce suitable Eproms.

P.S.U. Monitor

A quad voltage comparitor IC48 is used to check the swtiched +5V level, 21V and 24V. IC50 outputs this data on to the data bus when PORT 12 is inputed.

P.S.U. Circuit

Mains Transformer

A toroidal mains transformer of the following specification is used in 'E' Series programmers :-

Input	Colour Code	Outputs	Colour Code
0v	Blue	0v	Red +
110v	Violet	8v 25mps	Red
120v	Brown		
		0v	Orange +
0v	Blue *	24v 21Amp	Orange
110v	Violet *		
120v	Brown *		
Screen	Green/Yellow		

* Small yellow sleeve at transformer end identified this group of windings.
\+ Small white sleeve at transformer end identifies phase of secondary windings.

NOTE that later models have a different Primary Colour Code :- 0v Blue, 110v Violet, 120v White ; 0v Black, 110v Grey, 120v Brown.

+5v Supply

A conventional circuit using a bridge rectifier and series regulator. A switched +5v output is controlled by software to supply the EPROM sockets.

+25v/21v/12v Supplies

The 25v/21v supply is swtiched by Q1. The +12v supply is Fixed regulated by ICI. Q13,14 provide current limiting at 400mA .

Pins 22 Supply

Pins 22 of the EPROM sockets require a wide variety of supply voltages. Q2,3,4,5,6,7 and associated circuitry select 0v,12v, 21v or 25v under software control.

L.E.D. indicators monitor:-

L.E.D.1	Unregulated +24v
L.E.D.2	regulated +12v
L.E.D.3	" " +21/25v
L.E.D.4	" " + 5v

Interface and Memory Board

This board has three functions:-

1. Hex-Keypad.
2. Serial RS232 Input/Output.
3. Random Access Memory.
4. Parallel Input/Output.

1. Hex-Keypad

IC15 an LSI Keyboard decoder chip enables the reading of the 16 hex keys and 4 function Keys.

2. Serial RS232 Input/Output

The heart of the Serial I/O is the 6402 U.A.R.T IC18. IC13 an eight bit latch holds the baud rate selection (Bits 0,1,2,3) and the remaining bits are used to control parity, stop bits and clear the Data ready flag. IC11 is a four bit latch used to select 7 or 8 data bits and handshaking output Flags. IC10 accepts the master 2.4576 MHz clock and converts this to the required U.A.R.T clocking speed set by IC13. An external clock may also be selected e.g. the external clock generated by the cassette interface unit. This permits accurate tracking of the cassette unit increasing the integrity of operation.

IC16 converts the CMOS signal levels to RS232 levels (approx. +9v). Conversely IC19 converts the RS232 input levels to CMOS levels. The Clear to send and data set ready handshaking inputs are buffered through IC14.

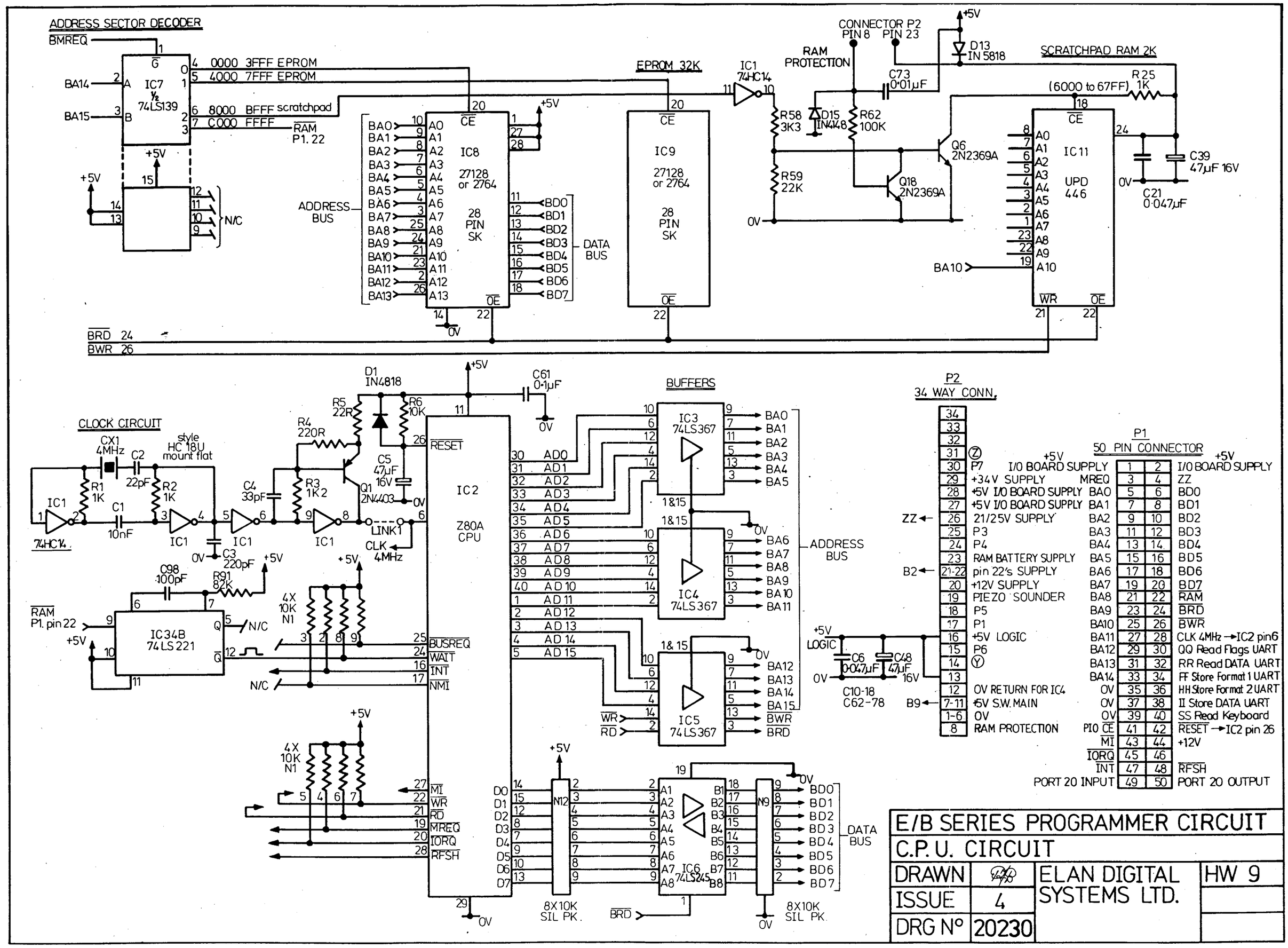
IC17 converts the +12v supply to -9v to provide the negative bias on the RS232 Output lines.

3. Random Access Memory

A maximum of 16K bytes of RAM may be accomodated on the board (IC2,3,4,5,6,7,8,9). A minimum of 8K bytes is fitted (IC2,3,4,5). IC12 enabled by RAM selects one of eight 4016 RAM chips.

4. Parallel Input/Output

IC1 a Z80 P.I.O chip provides two 8 bit parallel I/O ports at T.T.L levels with handshaking control.


ADDRESS SECTOR DECODER
BMREQ
IC7 ½ 74LS139
0000 3FFF EPROM
4000 7FFF EPROM
8000 BFFF scratchpad
C000 FFFF
RAM P1. 22
N/C
EPROM 32K
IC8 27128 or 2764 28 PIN SK
IC9 27128 or 2764 28 PIN SK
ADDRESS BUS
DATA BUS
IC1 74HC14
RAM PROTECTION
CONNECTOR P2 PIN 8 PIN 23
D13 IN 5818
C73 0·01µF
D15 IN4148
R62 100K
R58 3K3
R59 22K
Q6 2N2369A
Q18 2N2369A
SCRATCHPAD RAM 2K
(6000 to 67FF)
R25 1K
IC11 UPD 446
C39 47µF 16V
C21 0·047µF
BRD 24
BWR 26
CLOCK CIRCUIT
CX1 4MHz
C2 22pF
style HC 18U mount flat
R1 1K
R2 1K
C1 10nF
C3 220pF
74HC14
C4 33pF
R3 1K2
R4 220R
R5 22R
R6 10K
D1 IN4818
C5 47µF 16V
Q1 2N4403
LINK1
CLK 4MHz
C61 0·1µF
IC2 Z80A CPU
RESET
BUSREQ
WAIT
INT
NMI
MI
WR
RD
MREQ
IORQ
RFSH
C98 100pF
R91 82K
IC34B 74LS221
RAM P1. pin 22
4X 10K N1
BUFFERS
IC3 74LS367
IC4 74LS367
IC5 74LS367
IC6 74LS245
N12
N9
8X10K SIL PK.
ADDRESS BUS
DATA BUS
P2 34 WAY CONN.
P1 50 PIN CONNECTOR
P7 I/O BOARD SUPPLY
+34V SUPPLY
+5V I/O BOARD SUPPLY
+5V I/O BOARD SUPPLY
21/25V SUPPLY
P3
P4
RAM BATTERY SUPPLY
pin 22's SUPPLY
+12V SUPPLY
PIEZO SOUNDER
P5
P1
+5V LOGIC
P6
OV RETURN FOR IC4
+5V S.W. MAIN
OV
RAM PROTECTION
C6 0·047µF
C48 47µF 16V
C10-18 C62-78
I/O BOARD SUPPLY
MREQ
BA0
BA1
BA2
BA3
BA4
BA5
BA6
BA7
BA8
BA9
BA10
BA11
BA12
BA13
BA14
OV
OV
OV
PIO CE
MI
IORQ
INT
PORT 20 INPUT
ZZ
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
RAM
BRD
BWR
CLK 4MHz → IC2 pin6
QQ Read Flags UART
RR Read DATA UART
FF Store Format 1 UART
HH Store Format 2 UART
II Store DATA UART
SS Read Keyboard
RESET → IC2 pin 26
+12V
RFSH
PORT 20 OUTPUT
E/B SERIES PROGRAMMER CIRCUIT
C.P.U. CIRCUIT
DRAWN
ISSUE 4
DRG N° 20230
ELAN DIGITAL SYSTEMS LTD.
HW 9

PORT SECTOR DECODE

BA4
BA5
IORQ
BRD
BWR

¼ 74LS32 IC21A
¼ 74LS32 IC21B

IC 12 74LS139
IC 12

PORT 20 INPUT STROBE
YY
PORT 20 OUTPUT STROBE

¼ 74LS08 IC 24
P10 CE
P1.51

INPUTS

IC 14 74LS138
BA0 BA1 BA2 BA3 +5V

NN input switches
OO input PSU monitor
PP input PSU monitor
QQ read flags UART
RR read data UART
SS read keyboard
TT
UU

OUTPUTS

IC 15 74LS138

R8 2K2
R9 2K2
IC25 ¼74LS04
EE
FF
HH
II
JJ
KK
LL
MM

IC 16 74LS138

74LS04
IC25
LATCH SA0-SA7
LATCH SA8-SA15
LATCH DATA TO SK's
AA
BB
CC
R10 2K2
DD

CS DECODE

2X 74LS 00

IC 13 74LS138
PORT 08
09
0A
0B
0C
0D
0E
0F

IC22 CS0
IC22 CS1
IC22 CS2
IC22 CS3
IC23 CS4
IC23 CS5
IC23 CS6
IC23 CS7

IC32 74LS138
PORT 00

IC21 74LS32

D2 IN 914
+5V S.W.SUPPLY

IC 24 ¼74LS08
READ MASTER S.K.

IC25 74LS04
BYPASS SPEED CONTROL
COMMON 00 READ

R22 220R
0V

C7 1µF
R7 1K

IC17 74LS 273
IC 19 74LS 273
IC 18 74LS273
IC 20 74LS273

CLEAR CLK
BDO

PORT 04/0 (K)
PORT 04/1 (L)
PORT 04/2 (M)
PORT 04/3 (N)
PORT 04/4 (O)
PORT 04/5 (P)
PORT 04/6 (Q)
PORT 04/7 (R)

PORT 05/0 (S)
PORT 05/1 (T)
PORT 05/2 (U)
PORT 05/3 (V)
PORT 05/4 (W)
PORT 05/5 (X)
PORT 05/6 (Y)
PORT 05/7 (Z)

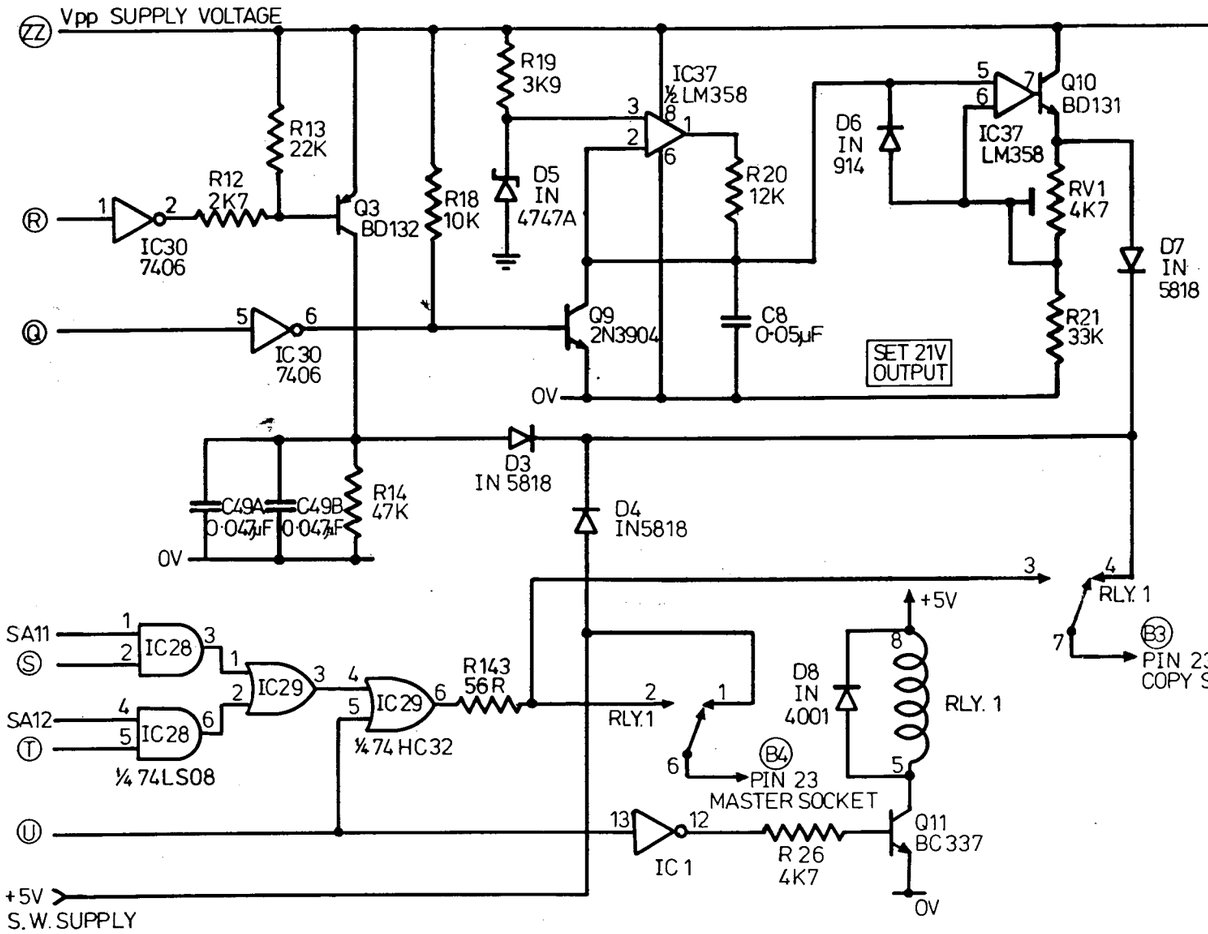
PORT 06/0 (P1)
PORT 06/1 (P2)
PORT 06/2 (P3)
PORT 06/3 (P4)
PORT 06/4 (P5)
PORT 06/5 (P6)
PORT 06/6 (P7)
PORT 06/7 (P8)
TO INTELLIGENT IDENTIFIER

Q0 (D)
Q0 (E)
Q1 (F)
Q1 (G)
Q2 (X2)
Q2 (X1)
Q3 IC 51 pin 13
Q3 N/C

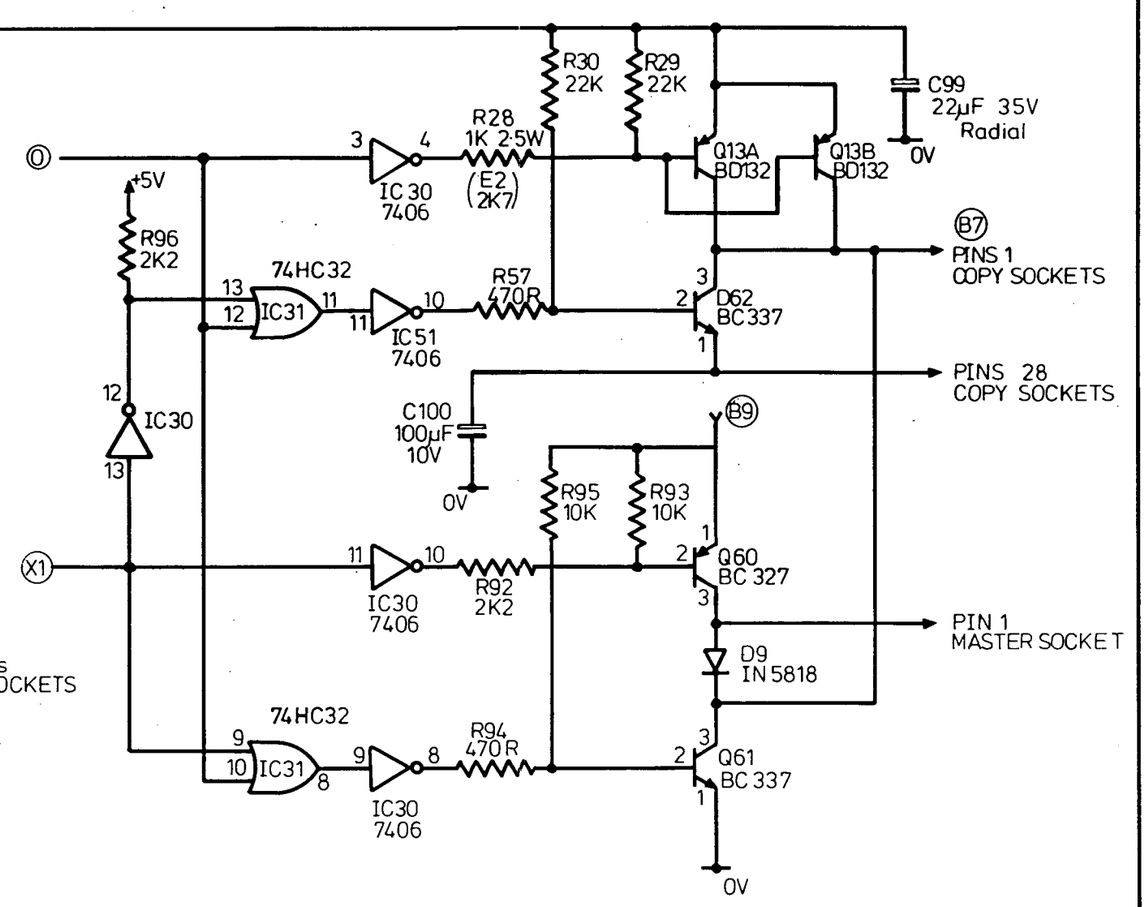
OUTPUT PORT LATCHES

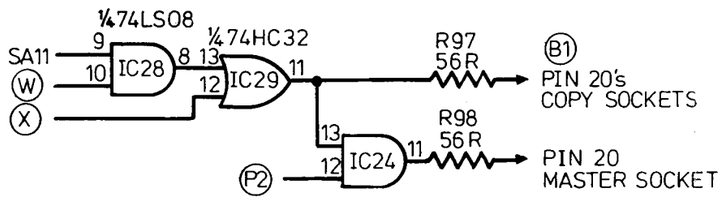
E/B SERIES PROGRAMMER CIRCUIT		
PORT & CS DECODE CIRCUITS		
DRAWN	RJB	ELAN DIGITAL SYSTEMS LTD.
ISSUE	3	
DRG N°	20231	

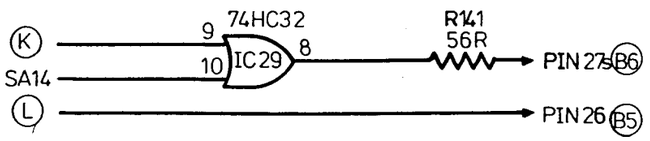
E² Vpp WAVE SHAPER

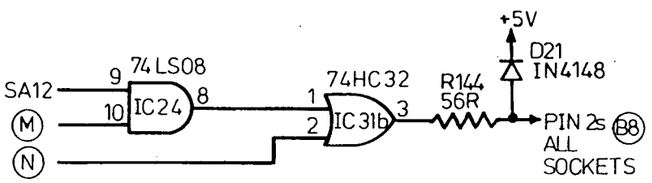


LEVEL SHIFTERS / SWITCHING CIRCUITRY

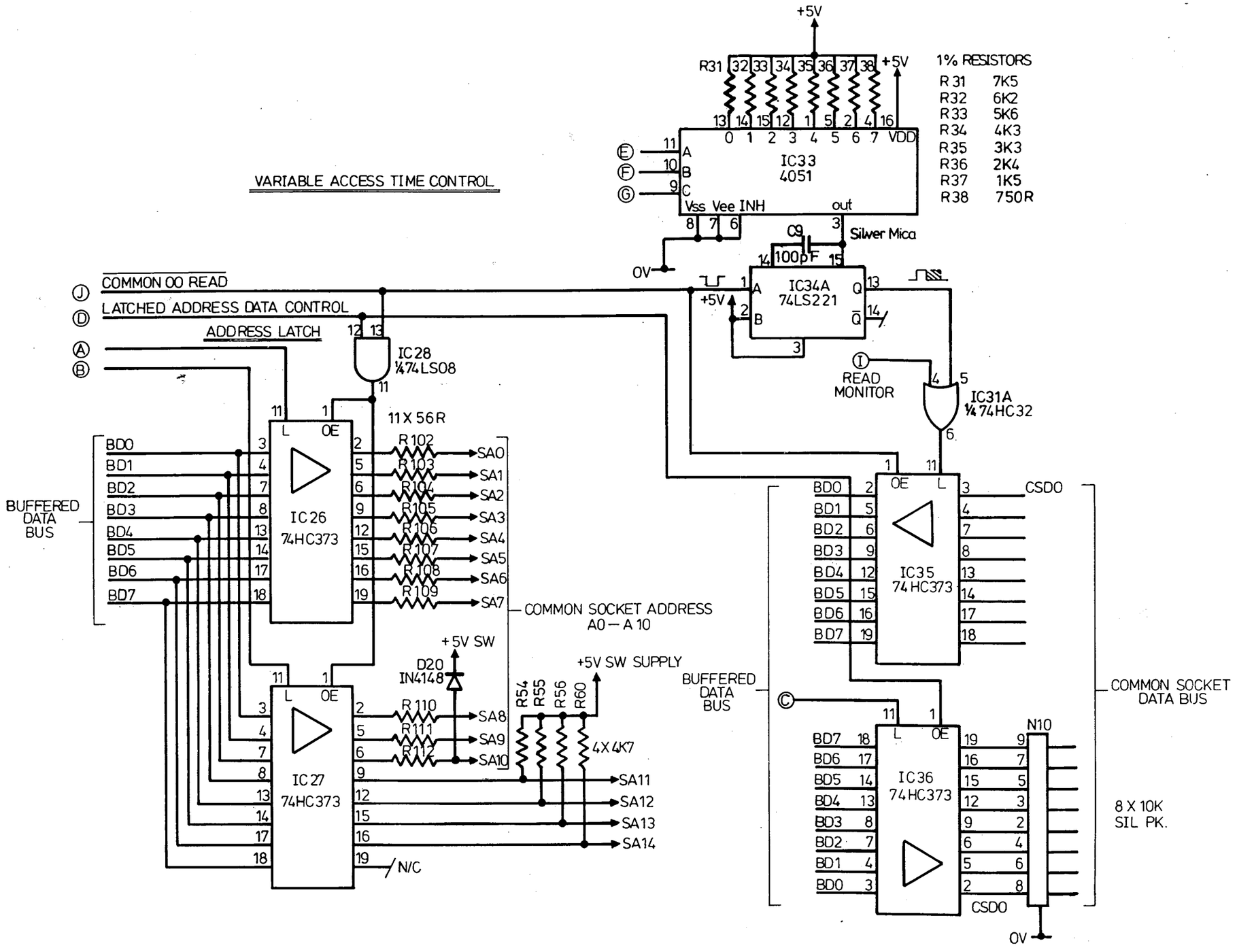








E/B SERIES PROGRAMMER CIRCUIT			
LEVEL SHIFTING CIRCUITS			
DRAWN	[illegible]	ELAN DIGITAL SYSTEMS LTD	
ISSUE	1		
DRG Nº	20232		



E/B SERIES PROGRAMMER CIRCUIT			
ADDRESS LATCH & DYNAMIC ACCESS			
DRAWN		ELAN DIGITAL SYSTEMS LTD	
ISSUE	1		
DRG Nº	20233		

+12V → IC50 pin 16

+5V Logic Supply → RLY 4 FUJITSU FBR 211

(B9) +5V S.W. Main Supply → R39 4K7 → Q14 BC337 → D11 IN4148 → 0V

(B5) → R40 R41 2x OR 22 2·5W

MASTER SK. pin 26 → C71 0·1µF → R24 4K7 → Q17 BC337 → D10 IN 5818 → 0V

MON.1 (M) ← RL4 (1, 5, 2)

(B1) → COPY SKs pins 20

SA13

MON.3 (B7) → COPY SKs pins 1

D18 IN5818 → 0V

150pf 0V

C19 0·1µF 150pf 0V

C31 150pf 0V

Drg. 296/3

R R R R24 3x 1K

N6 1K

C97 0·047µF 0V

MASTER SOCKET

COMMON SK. ADDRESS BUS SA0 to SA10

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10

COMMON SK DATA BUS

R45 R46 R47 R48 R49 R50 R51 R52 8x10R

D0 D1 D2 D3 D4 D5 D6 D7

C20 C30 4x 0·047µF 0V

C81 C82 0V

C59 150pf 0V

C60 150pf 0V

IN4148 D17

R76 330R

BC327 Q58

BC337 Q59

R86 22K R87 22K

R88 1K R89 10K

IC51 7406

COPY SOCKET 1

Mon 2.

C51 150pf C80 C79 2 x 0·047µF

Q57 BC337 R85 4K7 → IC20 pin 12

D16 IN5818

(B2) → C22 C32 4x 0·047µF 0V; C83 C84 0V → COPY SOCKET 2 → PCB 377 pin 12 → C52 150pf 0V → CS1

C23 C33 4x 0·047µF 0V; C85 C86 0V → COPY SOCKET 3 → PCB 377 pin 13 → C53 150pf 0V → CS2

C24 C34 4x 0·047µF 0V; C87 C88 0V → COPY SOCKET 4 → PCB 377 pin 14 → C54 150pf 0V → CS3

C25 C35 4x 0·047µF 0V; C89 C90 0V → COPY SOCKET 5 → PCB 377 pin 15 → C55 150pf 0V → CS4

C26 C36 4x 0·047µF 0V; C91 C92 0V → COPY SOCKET 6 → PCB 377 pin 16 → C56 150pf 0V → CS5

C27 C37 4x 0·047µF 0V; C93 C94 0V → COPY SOCKET 7 → PCB 377 pin 17 → C57 150pf 0V → CS6

150pf C28 C38 4x 0·047µF 0V; C95 C96 0V → COPY SOCKET 8 → PCB 377 pin 18 → C58 150pf 0V → CS7

(B2) → 0·1µF 0V

(P2) pin12 0V RETURN

IC24 pin11

(H)

(B4)

(B3) → COPY SKs pins 23

(B6) → ALL SKs pins 27

(B8) → ALL SKs pins 2

(B2) → COPY SK pins 22

INTELLIGENT IDENTIFIER

SA9

+12V

PIN 24 COMMON

+5V

RLY 5 HAMLIN HE721C05

D14 IN4148

Q7 BC337

R61 4K7 → (P8)

0V

(Y) BD7 BD6 BD5 BD4 BD3 BD2 BD1 BD0

HITACHI 16x1 LCD DISPLAY H2570 XLD

RV4 10K C29 0·047µF

0V R/S

(EE)

IC45 4042

BD3 BD2 BD1 BD0

(P2) PIN 30 OUTPUT

+5V

N2 8x22K

L.H. SWITCH S1

R.H. SWITCH S8

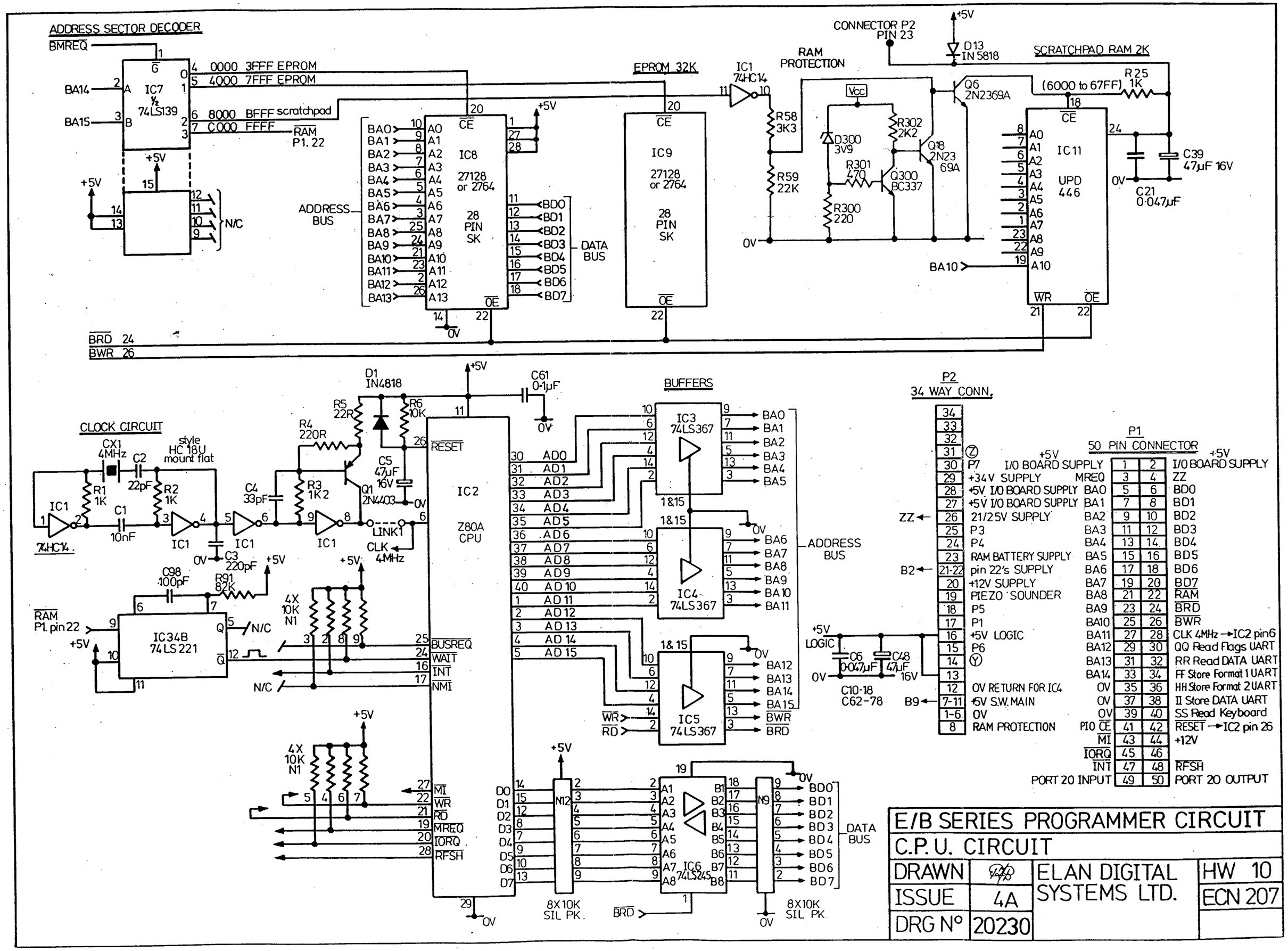
D22 D23 2xIN4148

IC43 74HC240

BD7 BD6 BD5 BD4 BD3 BD2 BD1 BD0

(NN)

E/B SERIES PROGRAMMER CIRCUITS			
MASTER/COPY SKT & DISPLAY CIRCUITS			
DRAWN	AMB	ELAN DIGITAL SYSTEMS LTD	
ISSUE	3		
DRG N°	20234		


ADDRESS SECTOR DECODER
BMREQ
IC7 ½ 74LS139
BA14
BA15
0000 3FFF EPROM
4000 7FFF EPROM
8000 BFFF scratchpad
C000 FFFF
RAM P1. 22
N/C
+5V
IC8 27128 or 2764 28 PIN SK
ADDRESS BUS
DATA BUS
EPROM 32K
IC9 27128 or 2764 28 PIN SK
IC1 74HC14
RAM PROTECTION
R58 3K3
R59 22K
D300 3V9
R301 470
R300 220
R302 2K2
Q300 BC337
Q18 2N23 69A
Q6 2N2369A
CONNECTOR P2 PIN 23
D13 IN 5818
SCRATCHPAD RAM 2K
(6000 to 67FF)
R25 1K
IC11 UPD 446
C39 47µF 16V
C21 0·047µF
BA10
BRD 24
BWR 26
CLOCK CIRCUIT
CX1 4MHz
C2 22pF
style HC 18U mount flat
R1 1K
R2 1K
C1 10nF
C3 220pF
IC1 74HC14
C4 33pF
R3 1K2
R4 220R
R5 22R
R6 10K
D1 IN4818
C5 47µF 16V
Q1 2N4403
LINK1
CLK 4MHz
C61 0·1µF
RESET
IC2 Z80A CPU
C98 100pF
R91 82K
RAM P1. pin 22
IC34B 74LS221
4X 10K N1
BUSREQ
WAIT
INT
NMI
MI
WR
RD
MREQ
IORQ
RFSH
BUFFERS
IC3 74LS367
IC4 74LS367
IC5 74LS367
ADDRESS BUS
C6 0·047µF
C48 47µF 16V
C10-18 C62-78
IC6 74LS245
N12
N9
8X10K SIL PK.
DATA BUS
P2 34 WAY CONN.
P1 50 PIN CONNECTOR
P7 I/O BOARD SUPPLY
+34V SUPPLY
+5V I/O BOARD SUPPLY
+5V I/O BOARD SUPPLY
21/25V SUPPLY
P3
P4
RAM BATTERY SUPPLY
pin 22's SUPPLY
+12V SUPPLY
PIEZO SOUNDER
P5
P1
+5V LOGIC
P6
0V RETURN FOR IC4
+5V S.W. MAIN
0V
RAM PROTECTION
I/O BOARD SUPPLY
ZZ
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
RAM
BRD
BWR
CLK 4MHz → IC2 pin6
QQ Read Flags UART
RR Read DATA UART
FF Store Format 1 UART
HH Store Format 2 UART
II Store DATA UART
SS Read Keyboard
RESET → IC2 pin 26
+12V
RFSH
PORT 20 INPUT
PORT 20 OUTPUT
E/B SERIES PROGRAMMER CIRCUIT
C.P.U. CIRCUIT
DRAWN
ISSUE 4A
DRG Nº 20230
ELAN DIGITAL SYSTEMS LTD.
HW 10
ECN 207

MON 4
MON 3
MON 2
MON 1
R63 24K 1%(pins 23,24V)
R65 24K 1%(pins 1, 24V)
R67 20K 1%(pins 1, 21V)
R69 24K 1% (pins 1, 12V)
R71 20K 1%
R72 3K3 1%
R70 7K5 1%
R68 3K3 1%
R66 3K3 1%
R64 3K3 1%
R73 680R
R74 2K2
set V REF
RV3 4K7
R75 47K
IC46 TL430C (RS 283227)
C74 22µF 6·3V
C106 0·1µF 50V
R134 24K 1%(pins 22, 24V/12·5V)
R137 20K 1% (pins 22,21V)
R138 10K 1%
R139 2K7 1%
C104 390pF
R142 13K 1%
R140 3K3 1%
R135 3K3 1%
C105 390pF
IC 20 pin 16
R147 4K7
Q63 BC 337
R148 4K22 0·5%
IC47 LM339
IC48 LM339
IC52 LM339
SA8
R101 7K5 1%
Vcc
VCC(5V)
VCC(6V)
N8 10K SIL
N11 10K SIL
N7 10K SIL
IC49 4503
IC 50 4503
R84 2K2
R146 2K2
BUFFERED DATA BUS
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
+5V
0V
FF
00

E/B SERIES PROGRAMMER CIRCUIT			
VOLTAGE MONITORING CIRCUIT			
DRAWN	PHD	ELAN DIGITAL SYSTEMS LTD.	
ISSUE	5		
DRG Nº	20235		

PL2
50 PIN
CONNECTOR 2

+5V LOGIC SUPPLY	1	2	+5V LOGIC SUPPLY
MREQ	3	4	ZZ
BA0	5	6	BD0
BA1	7	8	BD1
BA2	9	10	BD2
BA3	11	12	BD3
BA4	13	14	BD4
BA5	15	16	BD5
BA6	17	18	BD6
BA7	19	20	BD7
BA8	21	22	RAM
BA9	23	24	BRD
BA10	25	26	BWR
BA11	27	28	CLK
BA12	29	30	OQ Read flag UART
BA13	31	32	RR Read data UART
BA14	33	34	FF Store format 1 UART
0V	35	36	HH Store format 2 UART
0V	37	38	II Store data UART
0V	39	40	SS Read keyboard
P10 CE	41	42	
M1	43	44	
IORQ	45	46	
INT	47	48	RFSH
PORT 20 INPUT	49	50	PORT 20 OUTPUT

OPTIONAL

CONNECTOR 2

FF	Store Format A
RR	Read Data
QQ	Read Flags
II	Store Output Data
HH	Store Format B
SS	Read Keyboard

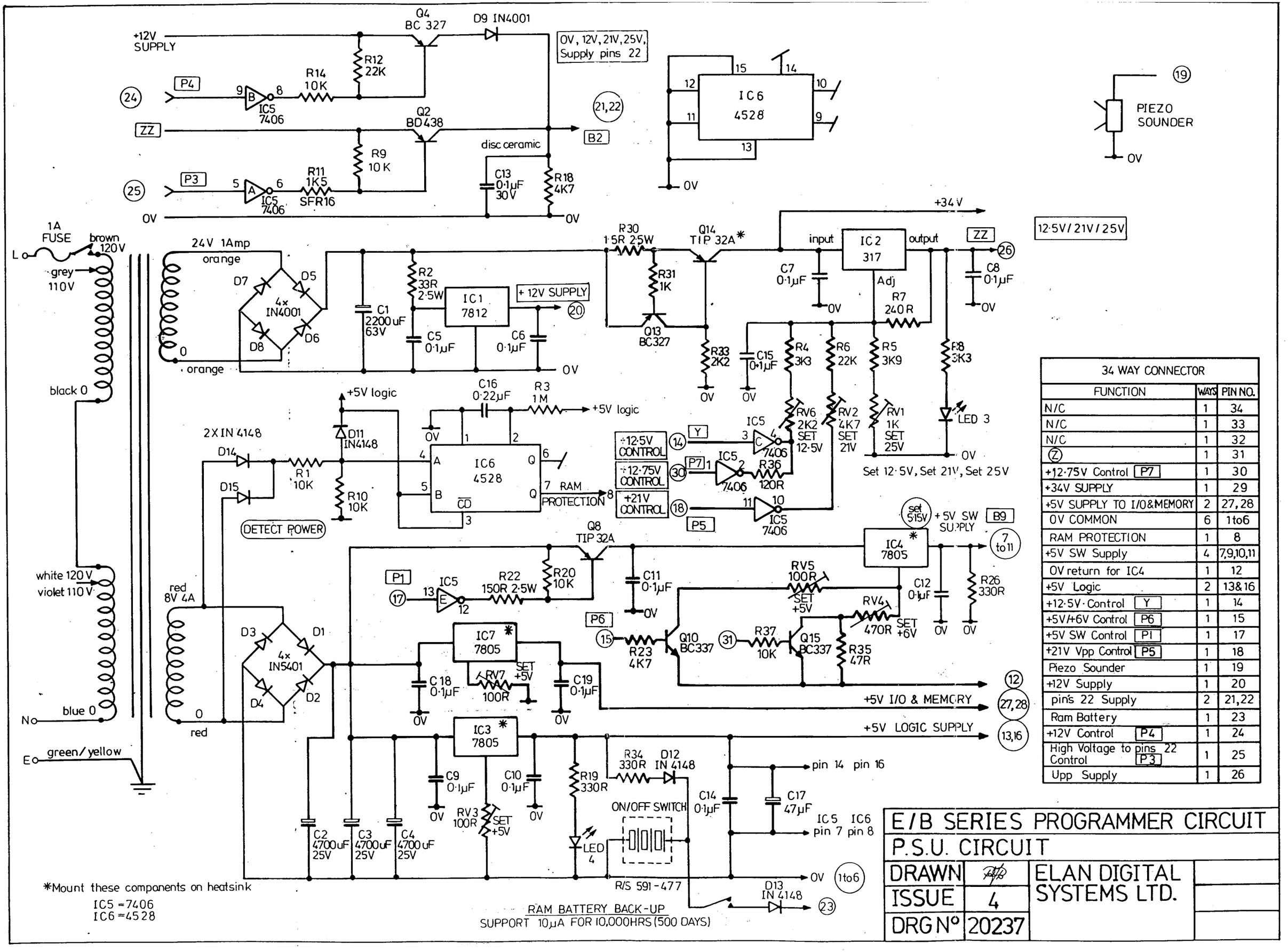
PL3
CONN. 3
25 WAY 'D'

2	Serial Output
4	R.Q.S. Output
20	D.T.R. Output
3	Serial Input
5	C.T.S. Input
6	D.S.R. Input
7	
1	CHASSIS

E B SERIES PROGRAMMER CIRCUITS
DRAM, KEYBOARD & INTERFACE

DRAWN	P.J.L.	ELAN DIGITAL SYSTEMS LTD
ISSUE	3	
DRG Nº	20236	

MBB 7/11/85



34 WAY CONNECTOR		
FUNCTION	WAYS	PIN NO.
N/C	1	34
N/C	1	33
N/C	1	32
Ⓩ	1	31
+12·75V Control P7	1	30
+34V SUPPLY	1	29
+5V SUPPLY TO I/O&MEMORY	2	27,28
0V COMMON	6	1to6
RAM PROTECTION	1	8
+5V SW Supply	4	7,9,10,11
0V return for IC4	1	12
+5V Logic	2	13&16
+12·5V Control Y	1	14
+5V/+6V Control P6	1	15
+5V SW Control P1	1	17
+21V Vpp Control P5	1	18
Piezo Sounder	1	19
+12V Supply	1	20
pins 22 Supply	2	21,22
Ram Battery	1	23
+12V Control P4	1	24
High Voltage to pins 22 Control P3	1	25
Upp Supply	1	26

*Mount these components on heatsink
IC5 = 7406
IC6 = 4528

E/B SERIES PROGRAMMER CIRCUIT
P.S.U. CIRCUIT

DRAWN	AHB	ELAN DIGITAL SYSTEMS LTD.
ISSUE	4	
DRG N°	20237	