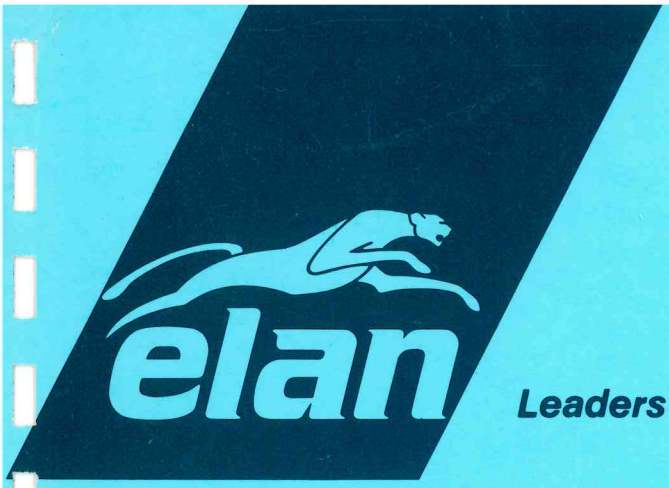

Leaders in device programming, copying, simulation

E2A
E8A
E9A

Elan Digital Systems

E2A, E8A, E9A CIRCUIT DESCRIPTION

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Clock, Micro-processor & Buffers

ICI and associated circuitry generates a 4MH3 MHz crystal controlled clock signal which is used to clock the micro-processor. The micro-processor IC2 is a Z80A. The data bus is buffered by IC6 a bi-directional buffer. The data direction is controlled by BRD. IC3,4 & 5 uni-directional buffers buffer the Address Bus and BWR, BRD signals.

Address Decoder, Internal EPROM and Scratchpad RAM.

One section of IC7 decodes the available 64K of addressing into four 16K sections:-

0000 to 3FFF	First EPROM	IC8
4000 to 7FFF	Second EPROM	IC9
8000 to BFFF	Scratchpad RAM	IC11
C000 to FFFF	Main RAM (Paged)	

Only 2K of Scratchpad RAM is fitted (Address 8000 to 87FF) and supported by Nickel Cadmium battery on PSU board.

The first three outputs of IC7 control the chip enable of EPROM and Scratchpad RAM selecting one device for a read or write operation in conjunction with BRD or BWR signals. The fourth output of IC7 generates the RAM signal which is 'paged' to expand the 16K segment to 128K (see Interface & memory section).

Port Decoder & Latches

IORQ, BRD, BRW signals are gated to produce an I/O write or an I/O read signal which enables pin 1 or 15 of IC12 the port sector decoder. IC12 decodes the I/O port address into four input sections (pin 4,5,6,7) or four output sections (pins 12,11,10,9) all active low. These sections are further decoded where necessary by IC13 (chip select decoder), IC14 (Various input ports), IC15 and IC16 (Various output ports).

Where data outputed to a port has to be stored it is held in latches (IC17,18,19,20).

Chip select decoder

IC13 selects one of the eight Copy sockets during a copy socket read. IC 32 selects the Master Socket during a master socket read.

Address Latch

IC26,27 latch the Port 00 and Port 01 data which is the socket Address LSB and MSB respectively. A common 00 Read signal or a latched Address/Data control signal enables the tri-state outputs of IC26, 27.

Variable Access Time Control

The tACC or access time of the EPROM is defined as the time taken for the EPROM to output correct data after the selected address is stable. In the 'E' Series programmers the read strobe is used to enable the Address latch (see above) and from this period of valid address a timing 'window' is generated by a monostable IC34. The period of the pulse generated by the monostable is determined by an R.C. time constant. The C content is fixed in C9 but the resistance can be selected via multiplexer IC33. One of eight resistors is selected by the ABC inputs.

It is therefore possible with software control to start off with a wide open 'window', check that the data is read correctly and progressively close the 'window' until the EPROM gives incorrect data.

The output of the monostable enable a transparent latch IC35 on the comon Socket Data Bus. IC31A permits the automatic overiding of the Access Time facility when reading the master socket.

Data Latch

IC36 latches the data to be programmed into the EPROMS. This has tri-state outputs controlled by the Latched Address/Data Control signal.

Interface Circuits

Various gates, transistors and relays perform multiplexing or level shifting functions for the multi-use pins on Copy and master sockets.

For EEPROMS a wave shaper circuit centred around IC37 conditions the rise and fall times of Vpp.

Relays 2 and 3 each 4 pole change over contacts switch the pin 20's of the Copy sockets between Output Enable function or Upp (Intel 2732, 2732A and Mostek MK2764).

Pin 1 of Master Socket & Copy Socket 1 have extra circuitry to permit reading & programming of the 27512 device.

Display and Piezo Sounder

IC45 latches selection of Code B or Hex display formats on the Display and also drives the piezo sounder which is situated on PSU board.

The 8 digit L.E.D. display is driven by IC44 a multiplexed display driver with internal RAM. IC42 latches the digit blanking (which is not available from IC44 with Hex display format). IC40,41 gate digit blanking to Common Cathode drive transistors Q48 to Q55. The L.E.D. display consists of two 4 digit 7 segment Litronix DL4770 displays.

Keyboard

IC43 inputs the eight push button switches onto the data bus when Port 10 is inputed.

Intelligent Identifier

Relay 5 and associated components permit intelligent interrogation of Eproms by switching Address 9 to +12v in acordance with Intel Specification. Earlier versions of Eproms do not have this facility and may be destroyed by this action. Software will be incorporated at a latter date to make full use of Intelligent Interrogation when manufacturers produce suitable Eproms.

Power Supply

Mains Transformer

A toroidal mains transformer of the following specification is used in 'E' Series programmers :-

Input		Colour Code	Outputs		Colour Code
0v	:	Blue	0v	:	Red +
110v	:	Violet	8v 5Amps	:	Red
120v	:	White		:	
	:		0v	:	Orange +
0v	:	Black	24v 2Amps	:	Orange
110v	:	Grey		:	
120v	:	Brown		:	
Screen	:	Green/Yellow		:	

General

A conventional circuit with two separate transformer windings providing the +5v supply and the Vpp supply (+25v, +21v and +12.5v). Series regulators are used to regulate the supply to the required voltages. The 'common' connection on the regulators have switched pull down resistors to select different voltage outputs. IC5 has six open collector drivers which interface TTL levels from the port control to the switching levels required by the power supply components.

A Monostable IC6 detects half-cycles of the mains supply giving advance warning (RAM PROTECTION Signal) in the event of power failure.

LED indicators monitor the main +5v logic supply and Vpp output.

+5v Supplies

IC3 supplies the +5v suppy to the logic on the main board.
IC7 supplies the +5v supply to the logic on the Interface and memory board.
IC4 provides +5v or +6v to the EPROM sockets switched on or off by Q8.
Preset potentionmeters provide fine trimming of output voltages.

Vpp Supplies

IC2 supplies the main Vpp power designated ZZ. IC5 gates C & D select +12.5v or 21v or 25v output voltage. Q13, 14 provide current limiting at 500mA.

A separate supply switched through Q4 provides Vpp power for pin's 22 of the EPROMs (2732 or 27512 devices only). Q4 provides +12v only for the erasure of EEPROM devices.

P.S.U. Monitor

Two quad voltage comparitors IC47, 48 are used to check the switched +5v level, 12.5v, 21v and 24v. IC49,50 output this data on to the data bus when PORT 11 or 12 is inputed.

IC46 is a precision voltage reference for the comparitors and its' output is set to 2.90v.

Interface and Memory Board

This board has four functions:-

1. Hex-Keypad
2. Serial RS232 Input/Output
3. Parallel Input/Output
4. Random Access Memory

1. Hex-Keypad

IC23 an LSI Keyboard decoder chip enables the reading of the 16 hex keys and 4 function keys.

2. Serial RS232 Input/Output

The heart of the Serial I/O is the 6402 U.A.R.T. IC27. IC25 an eight bit latch holds the baud rate selection (bits 0,1,2,3) and the remaining bits are used to control parity, stop bits and clear the DATA READY flag. IC26 is a four bit latch used to select 7 or 8 data bits and handshaking output flags. IC24 generates a 2.4576 MHz master clock and converts this to the required U.A.R.T. clocking speed set by IC25. IC29 converts the CMOS signal levels to RS232 levels (approx +- 9v). Conversely IC19 converts the RS232 input levels to CMOS levels. The CTS and DSR handshaking inputs are buffered through IC28.

IC30 converts the +12v supply to -9v to provide the negative bias on the RS232 Output lines.

3. Parallel Input/Output

IC1 a Z80A PIO chip provides two 8 bit parallel I/O ports at T.T.L. levels with handshaking control.

4. Random Access Memory

IC2 an 8203 DRAM controller provides all the interface and control for 128K x 8 DRAM. In standard configuration eight DRAM chips (IC3 to IC10) are fitted each chip holding 64K x 1. Expansion to 128K x 8 can be achieved by plugging in eight more 64K x 1 chips (IC11 to IC18).

Selection of the eight RAM pages is made through IC26 and IC21. The three bits latched in these chips (Y0,1,2) provide the three high order addresses AD 14,15,16 selecting one of eight 16K pages. BRAM signal is the master chip enable to the whole of RAM.

A WAIT state is automatically added to the Z80A read cycle each time a RAM read is requested. One half of IC34 on on the main board generates the WAIT state request from the BRAM signal.

ADDRESS SECTOR DECODER

MREQ
BA14
BA15
74LS139 IC7 ½
0000-3FFF EPROM
4000-7FFF EPROM
8000-BFFF Scratchpad
C000 FFFF RAM
RAM PL22
N/C
BRD
BWR

EPROM 32 K

ADDRESS BUS
DATA BUS
27128 or 2764
28 PIN SK
IC8
IC9
+5V
0V

CONNECTOR P2
PIN 8 RAM PROTECTION
PIN 23
D13 1N5818
SCRATCHPAD RAM 2K
C73 001µ
74LS04 IC1
R58 3K3
D15 IN4148
R62 100K
R25 1K
(6000 to 67FF)
R59 22K
Q6 2N2369A
Q18 2N2369A
UPD 446
IC11
BA10
C21 0·047uf
C39 47uf 16V

P1
50 PIN CONNECTOR

+5V I/O BOARD SUPPLY	1	2	+5V I/O BOARD SUPPLY
MREQ	3	4	ZZ
BA0	5	6	BD0
BA1	7	8	BD1
BA2	9	10	BD2
BA3	11	12	BD3
BA4	13	14	BD4
BA5	15	16	BD5
BA6	17	18	BD6
BA7	19	20	BD7
BA8	21	22	RAM
BA9	23	24	BRD
BA10	25	26	BWR
BA11	27	28	CLK
BA12	29	30	QQ Read Flags UART
BA13	31	32	RR Read DATA UART
BA14	33	34	FF Store Format 1 UART
0V	35	36	HH Store Format 2 UART
0V	37	38	II Store DATA UART
0V	39	40	SS Read Keyboard
P10 CE	41	42	
WT	43	44	
IORQ	45	46	
INT	47	48	RFSH
PORT 20 INPUT	49	50	PORT 20 OUTPUT

CLOCK CIRCUIT

CX1 4MHz
style HC18U Mount Flat
C2 22pF
R1 1K
R2 1K
C1 10nF
C3 220pF
74LS04 IC1
C4 33p
R3 1K2
R4 220R
R5 22R
R6 10K
D1 1N4816
Q1 2N4403
C5 47µF 16V
C61 0·1µF
CLK

BUFFERS

IC3 74LS367
IC6 74LS367
IC5 74LS367
IC6 74LS245
ADDRESS BUS
DATA BUS
8×10K SIL PK. N9

IC2 Z80A CPU
RESET
CLK
BUSREQ
WAIT
INT
NMI
MI
WR
RD
MREQ
IORQ
RFSH

C98 100pf
8K2
IC34B 74LS221
RAM Pl pin 22
4 x 10K N1

P2
34 WAY CONNECTOR

	30-34	
	29	
	28	+5V I/O BOARD SUPPLY
	27	+5V I/O BOARD SUPPLY
ZZ	26	21/25V SUPPLY
	25	P3
	24	P4
	23	RAM BATTERY SUPPLY
B2	21/22	pin 22's SUPPLY
	20	+12V SUPPLY
	19	PIEZO SOUNDER
	18	P5
	17	P1
	16	+5V LOGIC
	15	P6
	14	Ⓨ
	13	
	12	0V RETURN FOR IC4
B9	7to11	+5V S.W. MAIN
	1to6	0V
	8	RAM PROTECTION

+5V LOGIC
0·047µF
47uF 16V
C6 C10 to 18 C62 to 78
C48

E SERIES PROGRAMMER CIRCUIT	
C.P.U. CIRCUIT	
DRAWN	JS
ISSUE	1
DRG No.	296/1

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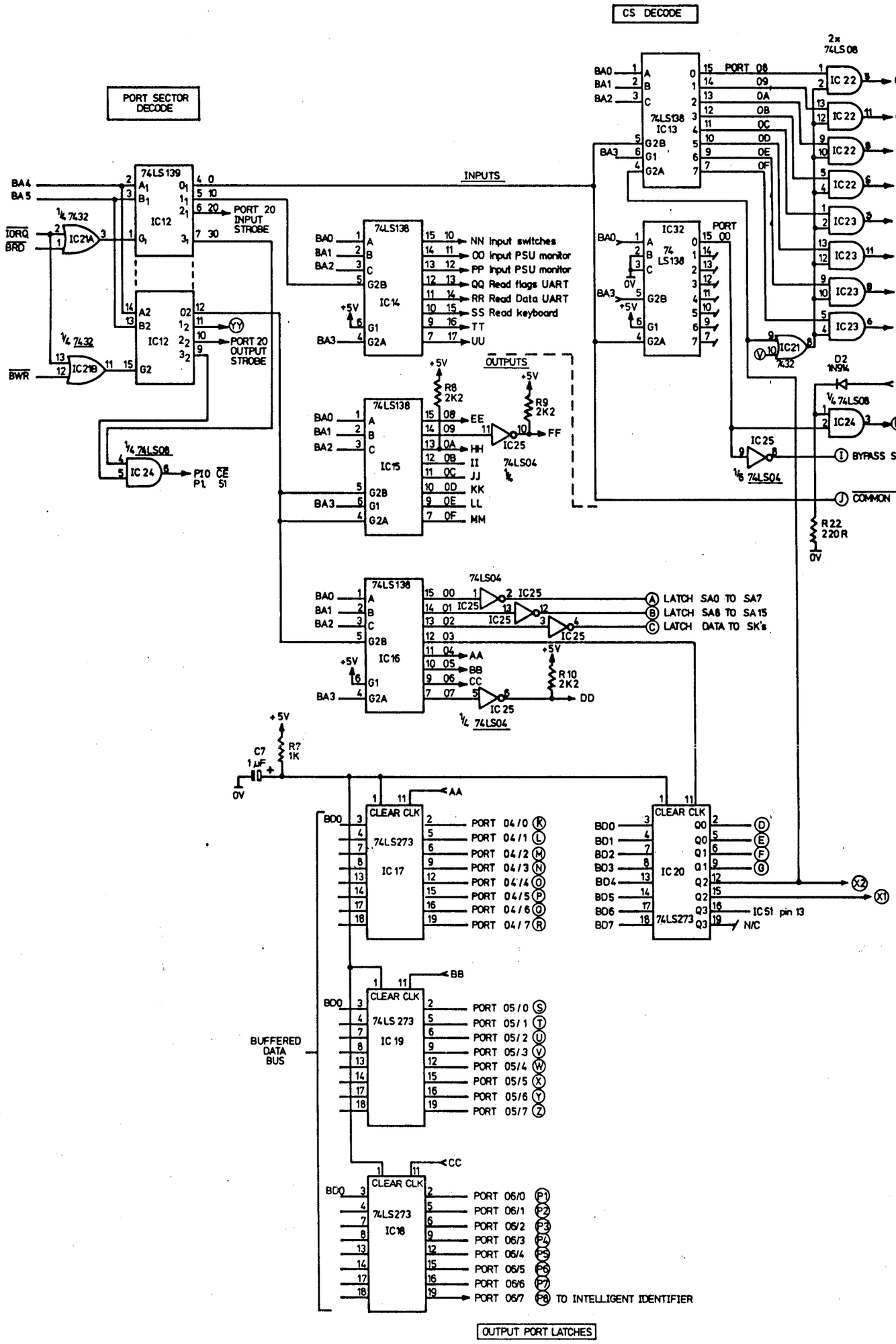
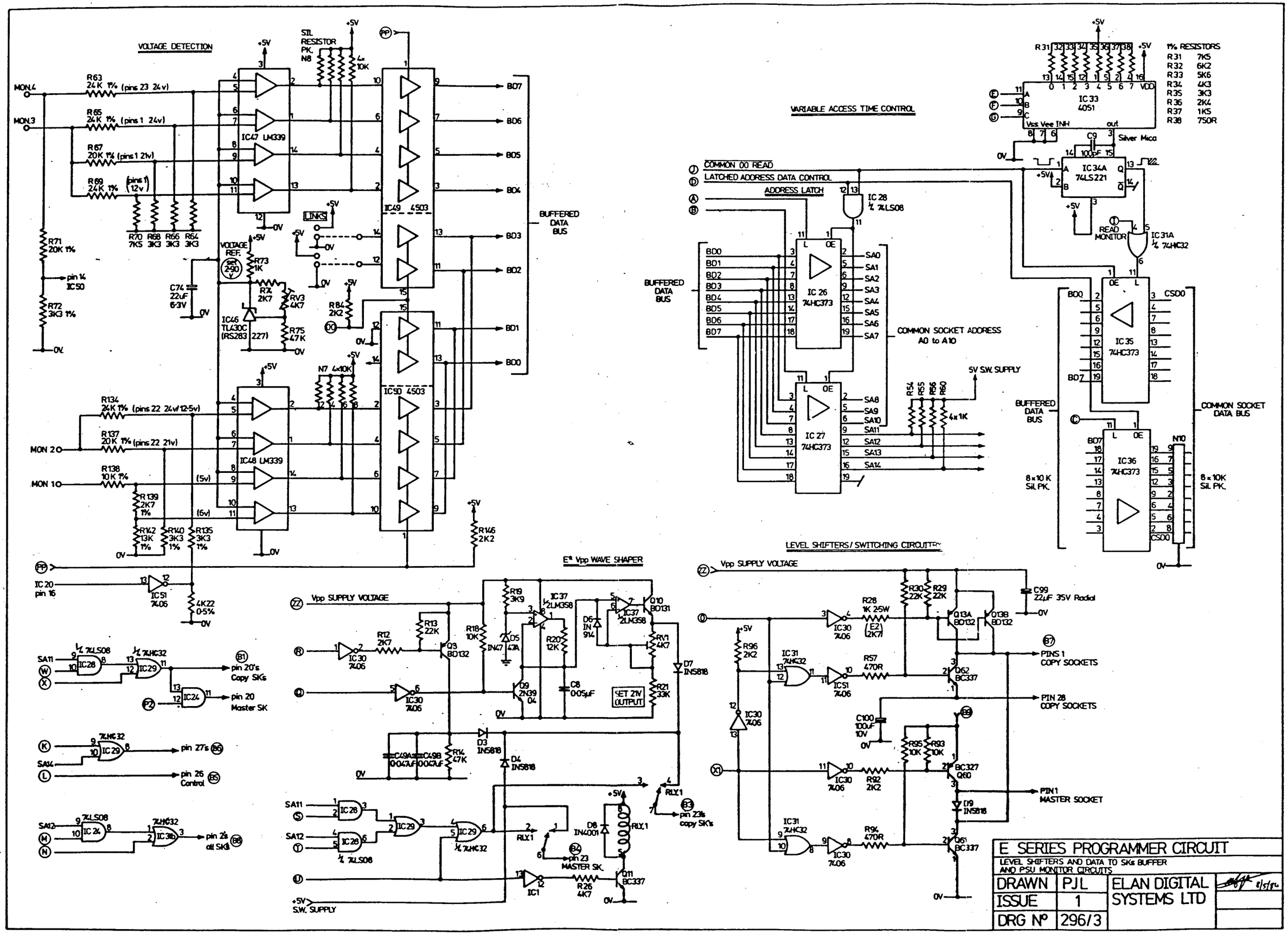


E SERIES PROGRAMMER CIRCUIT			
PORT & CS DECODE CIRCUITS			
DRAWN	P.J.L.	ELAN DIGITAL SYSTEMS LTD	MBB 8/5/84
ISSUE	1		
DRG. Nº.	296/2		


VOLTAGE DETECTION
VARIABLE ACCESS TIME CONTROL
E* Vpp WAVE SHAPER
LEVEL SHIFTERS/SWITCHING CIRCUITRY
BUFFERED DATA BUS
COMMON 00 READ
LATCHED ADDRESS DATA CONTROL
ADDRESS LATCH
COMMON SOCKET ADDRESS A0 to A10
COMMON SOCKET DATA BUS
5V S.W. SUPPLY
Vpp SUPPLY VOLTAGE
SET 21V OUTPUT
PINS 1 COPY SOCKETS
PIN 28 COPY SOCKETS
PIN 1 MASTER SOCKET
1% RESISTORS
R31 7K5
R32 6K2
R33 5K6
R34 4K3
R35 3K3
R36 2K4
R37 1K5
R38 750R
E SERIES PROGRAMMER CIRCUIT
LEVEL SHIFTERS AND DATA TO SKs BUFFER AND PSU MONITOR CIRCUITS
DRAWN PJL
ISSUE 1
DRG Nº 296/3
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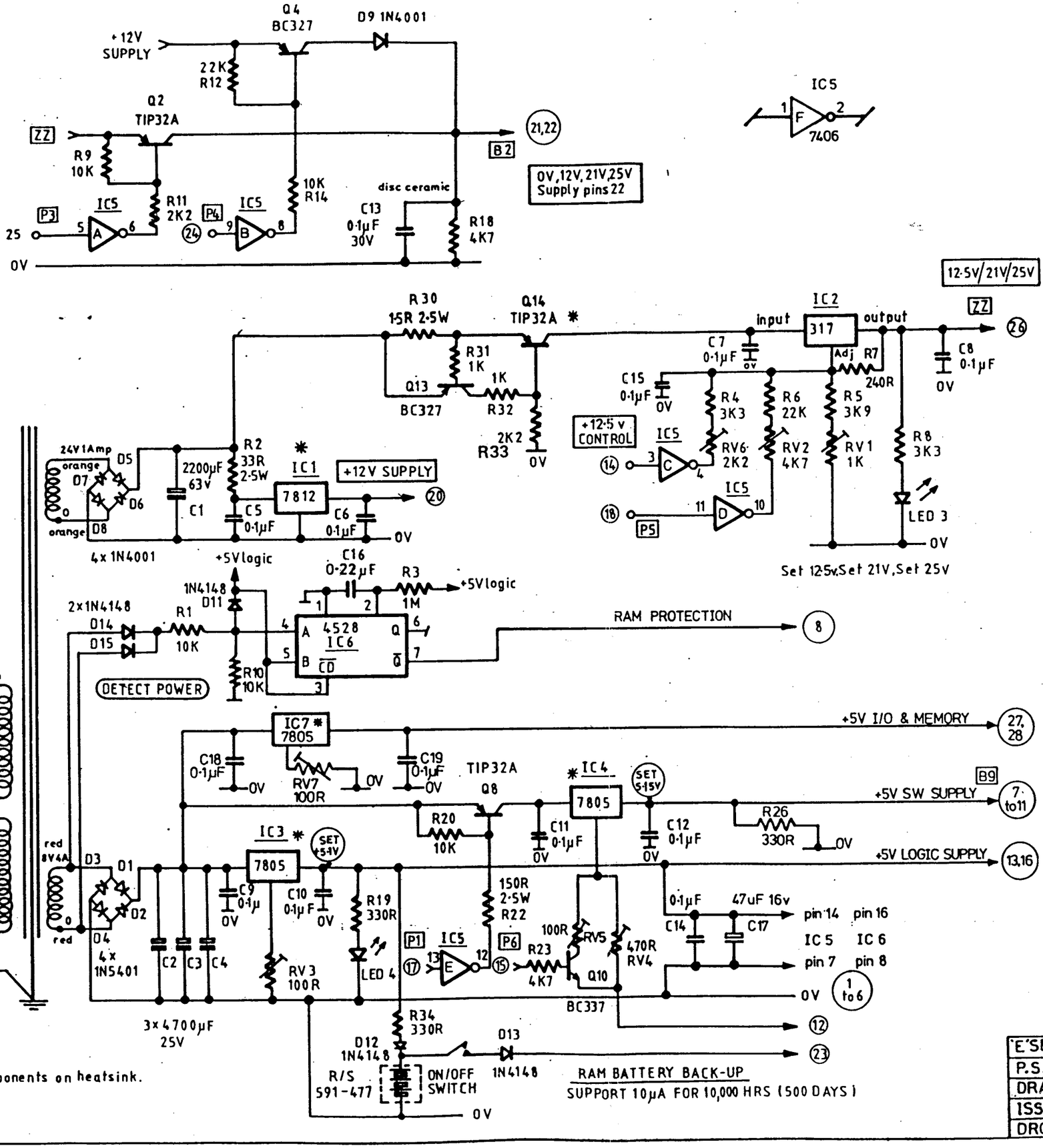
E A SERIES PROGRAMMER CIRCUITS

MASTER AND COPY SOCKET CIRCUITS
DISPLAY–KEYSWITCH–BUZZER CIRCUITS

DRAWN	P.J.L	ELAN DIGITAL SYSTEMS LTD
ISSUE	1	
DRG N°	296/4	



* Mount these components on heatsink.

IC5 = 7406
IC6 = 4528

34 WAY CONNECTOR		
FUNCTION	WAYS	PIN No.
N/C	1	34
N/C	1	33
N/C	1	32
N/C	1	31
N/C	1	30
N/C	1	29
+5V SUPPLY TO I/O & MEMORY	2	27. 28
0V COMMON	6	1 to 6
RAM PROTECTION	1	8
+5V SW Supply	4	7,9,10,11
0V return for IC4	1	12
+5V Logic	2	13 & 16
+13V Control	1	14
+5V/+6V Control P6	1	15
+5V SW Control P1	1	17
+21V Vpp Control P5	1	18
Piezo Sounder	1	19
+12V Supply	1	20
pin's 22 Supply	2	21,22
Ram Battery	1	23
+12V Control P4	1	24
High Voltage to pins 22 Control P3	1	25
Upp Supply	1	26

'E'SERIES PROGRAMMER CIRCUIT
P.S.U. CIRCUIT

DRAWN	JS
ISSUE	1
DRG No.	296/5

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PL2
50 PIN
CONNECTOR 2

+5V LOGIC SUPPLY	1	2	+5V LOGIC SUPPLY
MREQ	3	4	ZZ
BA0	5	6	BD0
BA1	7	8	BD1
BA2	9	10	BD2
BA3	11	12	BD3
BA4	13	14	BD4
BA5	15	16	BD5
BA6	17	18	BD6
BA7	19	20	BD7
BA8	21	22	RAM
BA9	23	24	BRD
BA10	25	26	BWR
BA11	27	28	CLK
BA12	29	30	QQ Read flag UART
BA13	31	32	RR Read data UART
BA14	33	34	FF Store format 1 UART
0V	35	36	HH Store format 2 UART
0V	37	38	II Store data UART
0V	39	40	SS Read keyboard
P10 CE	41	42	Spare
M1	43	44	Spare
IORQ	45	46	Spare
INT	47	48	RFSH
PORT 20 INPUT	49	50	PORT 20 OUTPUT

S3	S2	S1	S0	BAUD RATE
0	0	0	0	19,200 BAUD
0	0	0	1	19,200 "
0	0	1	0	50 "
0	0	1	1	75 "
0	1	0	0	134·5 "
0	1	0	1	200 "
0	1	1	0	600 "
0	1	1	1	2400 "
1	0	0	0	9600 "
1	0	0	1	4800 "
1	0	1	0	1800 "
1	0	1	1	1200 "
1	1	0	0	2400 "
1	1	0	1	300 "
1	1	1	0	150 "
1	1	1	1	110 "

E A SERIES PROGRAMMER CIRCUITS		
DRAM, KEYBOARD & INTERFACE		
DRAWN	P.J.L	ELAN DIGITAL SYSTEMS LTD
ISSUE	1	
DRG N°	296/6	