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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

Pb-free/Phase-out/Discontinued

MOS INTEGRATED CIRCUIT

μPD75P216A

4-BIT SINGLE-CHIP MICROCOMPUTER

The μPD75P216A is a One-Time PROM version of the μPD75216A. The μPD75P216A is suitable for small-scale production or experimental production in system development.

Also see documents for the μPD75216A.

FEATURES

- The μPD75216A compatible
- 16256 × 8 bits of on-chip one-time PROM
- Port 6 without pull-down resistor
- High voltage output for display
  S0 to S8, T0 to T9: On-chip load resistor
  S9, T10 to T15: Open drain
- Power-on reset circuit is not available
- Single power supply (5 V ± 10 %)

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD75P216ACW	64-pin plastic shrink DIP (750 mil)	Standard

Caution Pull-up resistor mask options are not available.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

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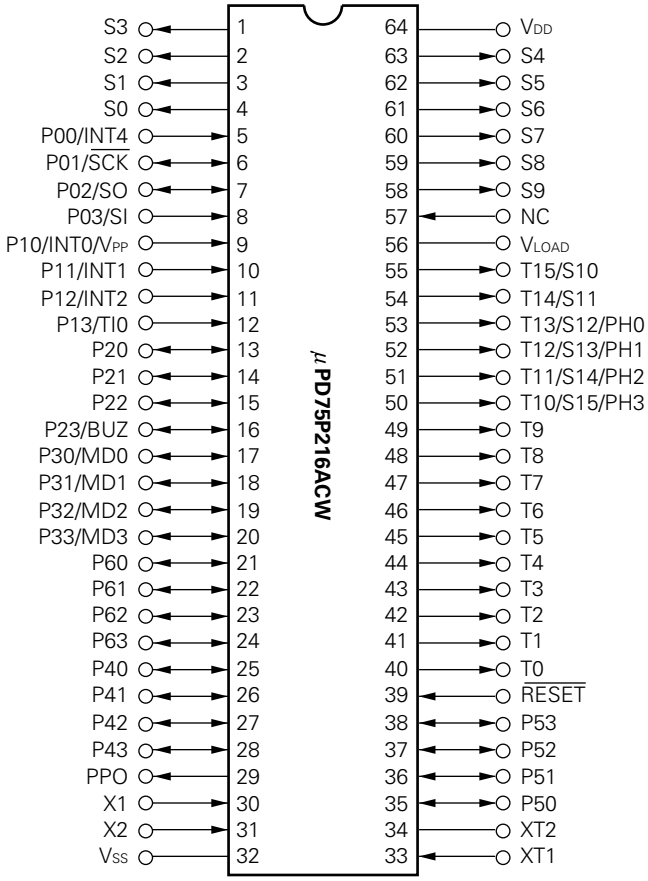
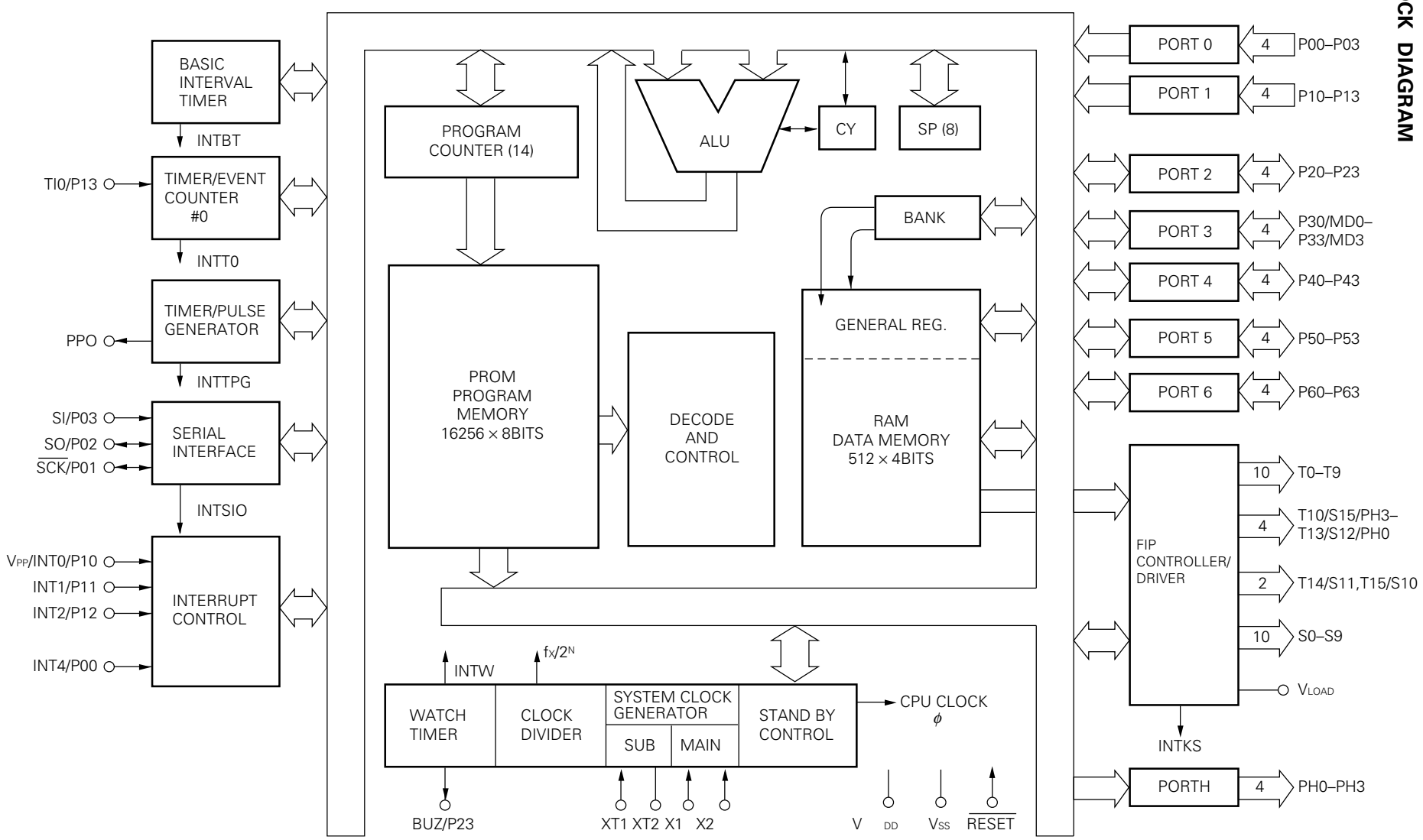
Date Published July 1993 P
Printed in Japan

The mark★ shows revised points.

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 PORT PINS

Pin name	Input/ output	Shared pin	Function	8-bit I/O	When reset	I/O circuit type Note
P00	Input	INT4	4-bit input port (PORT0).	×	Input	Ⓑ
P01	I/O	$\overline{SCK}$				Ⓕ
P02	I/O	SO				Ⓖ
P03	Input	SI				Ⓑ
P10	Input	INT0/V_{PP}	With noise elimination function	×	Input	Ⓑ
P11		INT1	With noise elimination function			
P12		INT2	4-bit input port (PORT1).			
P13		TI0				
P20	I/O	—	4-bit I/O port (PORT2).	×	Input	E
P21		—				
P22		—				
P23		BUZ				
P30 - P33	I/O	MD0 - MD3	Programmable 4-bit I/O port (PORT3). I/O can be specified bit by bit.	×	Input	E
P40 - P43	I/O	—	4-bit I/O port (PORT4). Can directly drive LEDs. Data input/output pins for the PROM write and verify (Four low-order bits).	○	Input	E
P50 - P53	I/O	—	4-bit I/O port (PORT5). Can directly drive LEDs. Data input/output pins for the PROM write and verify (Four high-order bits).	○	Input	E
P60 - P63	I/O	—	Programmable 4-bit I/O port (PORT6). I/O can be specified bit by bit. Suitable for keyboard input.	×	Input	E
PH0	Output	T13/S12	4-bit P-ch open-drain output port Can withstand high voltage and high current (PORTH)	×	High impedance	I-D
PH1		T12/S13				
PH2		T11/S14				
PH3		T10/S15				

Note The circle (○) indicates the Schmitt triggered input.

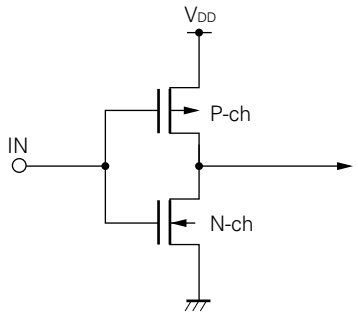
1.2 NON-PORT PINS

Pin name	Input/ output	Shared pin	Function		When reset	I/O circuit type Note 1
T0 - T9		—	Note 2	Used for digit output Can withstand high voltage and high current	Low level	I - E
T10/S15 - T13/S12	Output	PH3-PH0	Note 3	For digit/segment output Can withstand high voltage and high current Unused pin can be used as PORTH.	High impedance	I - D
T14/S11, T15/S10		—		For digit/segment output Can withstand high voltage and high current Static output is possible.		
S9				For segment output Can withstand high voltage Static output is possible		
S0 -S8			Note 2	For segment output Can withstand high voltage	Low level	I - E
PPO	Output	—	Pulse output by timer/pulse generator		High impedance	D
TI0	Input	P13	External event pulse input to timer event counter			Ⓑ
$\overline{SCK}$	I/O	P01	Input and output to serial clock		Input	Ⓕ
SO	I/O	P02	Serial data output or serial data input and output		Input	Ⓖ
SI	Input	P03	Serial data input or normal input		Input	Ⓑ
INT4	Input	P00	Edge detection vectored interrupt input (detected at both rising edge and falling edge)		—	Ⓑ
INT0	Input	P10/V_{PP}	Edge detection vectored interrupt input with noise elimination function (edge-detection selectable)		—	Ⓑ
INT1		P11				
INT2	Input	P12	Testable input for edge-detection (detected at rising edge)		—	Ⓑ
BUZ	I/O	P23	Fixed frequency output (For buzzer or system clock trimming)		Input	E
X1, X2	Input	—	Crystal/ceramic resonator connection for main system clock generation. When external clock signal is used, it is applied to X1, and its reverse phase signal is applied to X2.		—	—
XT1	Input	—	Crystal connection for subsystem clock generation. When external clock signal is used, it is applied to XT1 and XT2 is open.		—	—
XT2	—					
$\overline{RESET}$	Input	—	System reset input (low-level active)		—	Ⓑ
MD0 - MD3	I/O	P30 - P33	Operation mode selection during the PROM write/verify cycles.		—	E
V_{PP}		P10/INT0	+12.5 V is applied as the programming voltage during the PROM write/verify cycles		—	Ⓑ
V_{LOAD}		—	Pull-down resistor connection of FIP controller/driver		—	I - E
V_{DD}		—	Positive power supply +6 V is applied as the programming voltage during the PROM write/verify cycles		—	—
V_{SS}		—	GND potential		—	—
NC Note 4		—	No connection		—	—

Note 1. The circle (○) indicates the Schmitt triggered input.
2. Pull-down resistor is incorporated.
3. Open-drain output
4. NC pin should be connected to V_{PRE} when sharing print board with the μPD75216A.

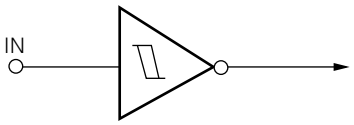
Fig. 1-1 Pin Input/Output Circuit

TYPE A



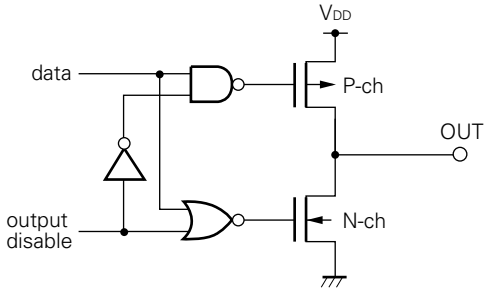
CMOS level input buffer

TYPE B



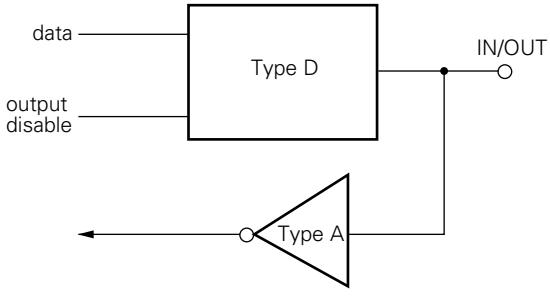
Schmitt-triggered input with hysteresis

TYPE D



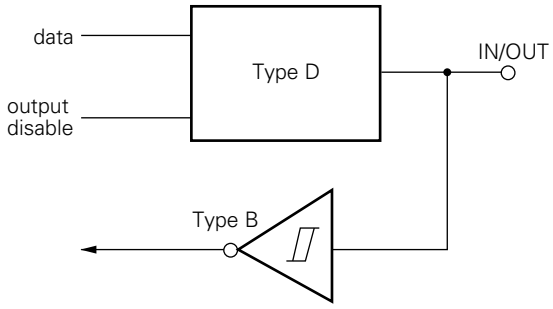
Push-pull output which can be set to high-impedance output (off for both P-ch and N-ch)

TYPE E



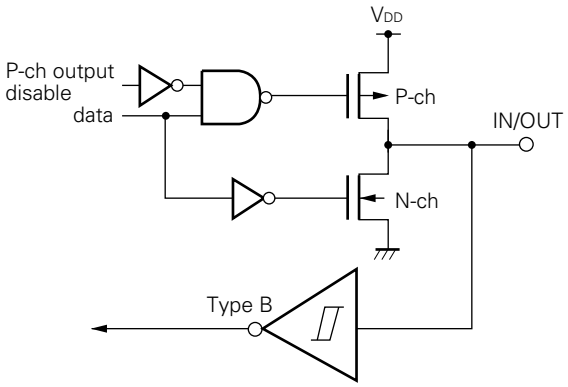
I/O circuit consisting of Type D push-pull output and Type A input buffer.

TYPE F



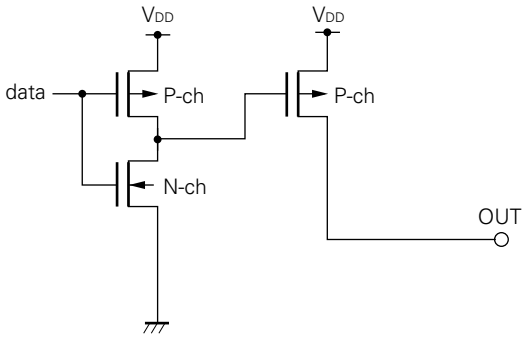
I/O circuit consisting of Type D push-pull output and Type B Schmitt-triggered input

TYPE G

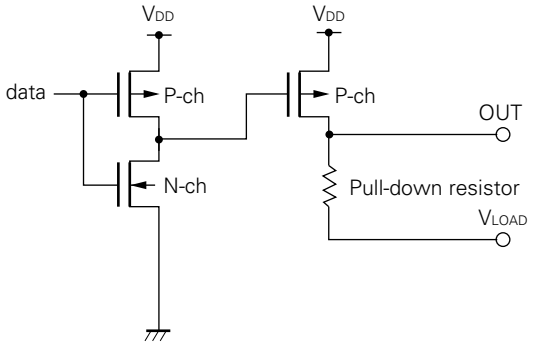


I/O circuit which can switch push-pull output or N-ch open-drain output (off for P-ch)

TYPE I-D



TYPE I-E



1.3 TREATMENT OF UNUSED PINS

Table 1-2 Recommended Connection for Unused Pins

Pin	Recommended connection
P00/INT4	Connect to V_{SS}
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD}
P02/SO	
P03/SI	
P10/INT0/V_{PP}	Connect to V_{SS}
P11/INT1, P12/INT2	
P13/T10	
P20 - P22	Input: Connect to V_{SS} or V_{DD} Output: Open
P23/BUZ	
P30/MD0 - P33/MD3	
P40 - P43	
P50 - P53	
P60 - P63	
PPO	Open
S0 - S9	
T15/S10, T14/S11	
T0 - T9	
T10/S15/PH3-T13/S12/PH0	
XT1	Connect to V_{SS} or V_{DD}
XT2	Open

2. DIFFERENCES BETWEEN THE μPD75P216A AND THE μPD75216A, μPD75208

Table 2-1 Differences between the μPD75P216A and the μPD75216A, μPD75208

Parameter		μPD75P216A	μPD75216A	μPD75208
ROM		One-time PROM	Mask ROM	
		16256 × 8 bits (0000H – 3F7FH)		8064 × 8 bits (0000H – 1F7FH)
RAM		512 × 4 bits		497 × 4 bits
FIP® Controller Driver		9 – 16 segments		9 – 12 segments
Pull-Down Registor	Port 6	N/A	Mask option	
	S0 – S8, T0 – T9	On-chip		
	S9, T10 – T15	N/A (Open-drain)		
Power-On Reset		N/A	Mask option	
Power-On Flag				
Pin Connection		P10/INT0/V_{PP}	P10/INT0	
		P30/MD0 – P33/MD3	P30 – P33	
		NC	V_{PRE}	
Operating Ambient Temperature		–10 to +70 °C	–40 to +85 °C	
Operating Supply Voltage		5 V ± 10 %	2.7 to 6.0 V	
Package		64-pin plastic shrink DIP (750 mil)	64-pin plastic shrink DIP (750 mil) 64-pin plastic QFP (14 × 20 mm)	

3. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY

The μPD75P216A contains 16256 × 8 bits of one-time PROM available of writing. The following table shows the pin functions during the write and verify cycles. Note that it is not necessary to enter an address, because the address is updated by pulsing the X1 clock pins.

Table 3-1 Used Pin at PROM Write and Verify

Pin name	Function
V_{PP}	Voltage application pin for write and verify (Normally V_{DD} potential)
X1, X2	Address-update clock input during write/verify. The inverted signal of the X1 should be input to the X2.
MD0 - MD3	Operation mode selection pins for write and verify
P40 - P43 (lower 4 bits) P50 - P53 (higher 4 bits)	8-bit data input/output pins for write and verify
V_{DD}	Supply voltage application pin Normally 5 V ± 10 %; 6 V is applied during write/verify

Caution 1. The pins which are not used during write or verify should be treated as follows

- **Port, XT1, $\overline{\text{RESET}}$ ... Connect to V_{SS} through pull-down resistors**
- **S0 to S9, T0 to T15, PPO, V_{LOAD} ... Connect to V_{DD} through pull-up resistors**
- **XT2 ... Open**

2. The μPD75P216A do not have a UV erase window, thus the PROM contents cannot be erased with ultra violet ray.

3.1 PROM WRITE AND VERIFY OPERATION

When +6 V and +12.5 V are applied to the V_{DD} and V_{PP} pins, respectively, the PROM is placed in the write/verify mode. The operation is selected by the MD0 to MD3 pins, as shown in the table.

Table 3-2 PROM Write and Verify Operation

Operation mode specification						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5	+6 V	H	L	H	L	Clear program memory address to 0
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

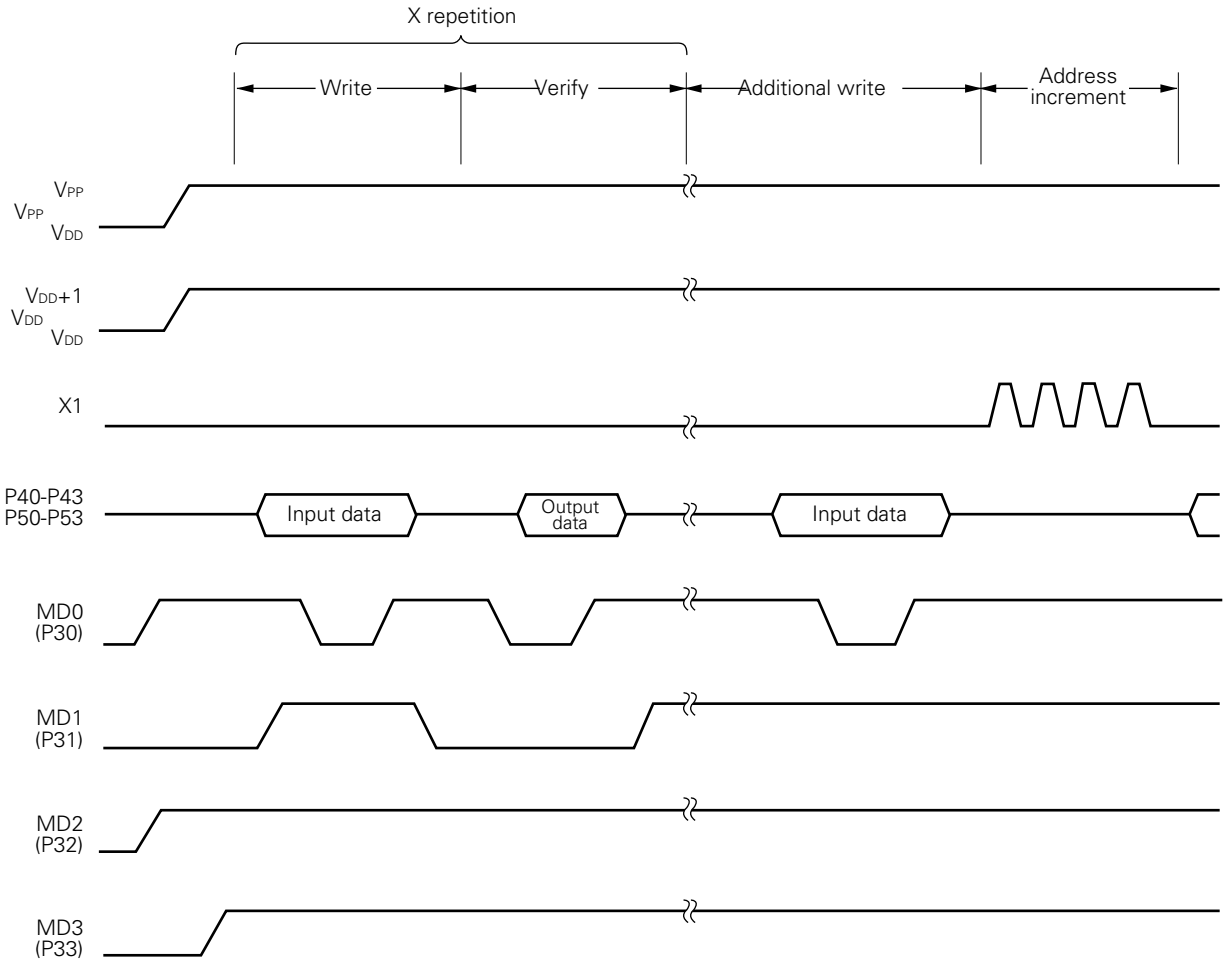
×: Don't care.

3.2 PROM WRITE PROCEDURE

PROM can be written at high speed using the following procedure: (see the following figure)

(1) Pull unused pins to V_{SS} through resistors. Set the X1 pin low.
(2) Supply 5 volts to the V_{DD} and V_{PP} pins.
(3) Wait for 10 μs.
(4) Select the zero clear program memory address mode.
(5) Supply 6 volts to the V_{DD} and 12.5 volts to the V_{PP} pins.
(6) Select the program inhibit mode.
(7) Write data in the 1 ms write mode.
(8) Select the program inhibit mode.
(9) Select the verify mode. If the data is correct, proceed to step (10). If not repeat steps (7), (8) and (9).
(10) Perform one additional write (duration of 1ms × number of writes at (7) to (9)).
(11) Select the program inhibit mode.
(12) Apply four pulses to the X1 pin to increment the program memory address by one.
(13) Repeat steps (7) to (12) until the end address is reached.
(14) Select the zero clear program memory address mode.
(15) Return the V_{DD} and V_{PP} pins back to + 5 volts.
(16) Turn off the power.

Fig. 3-1 Timing of Program Memory Write

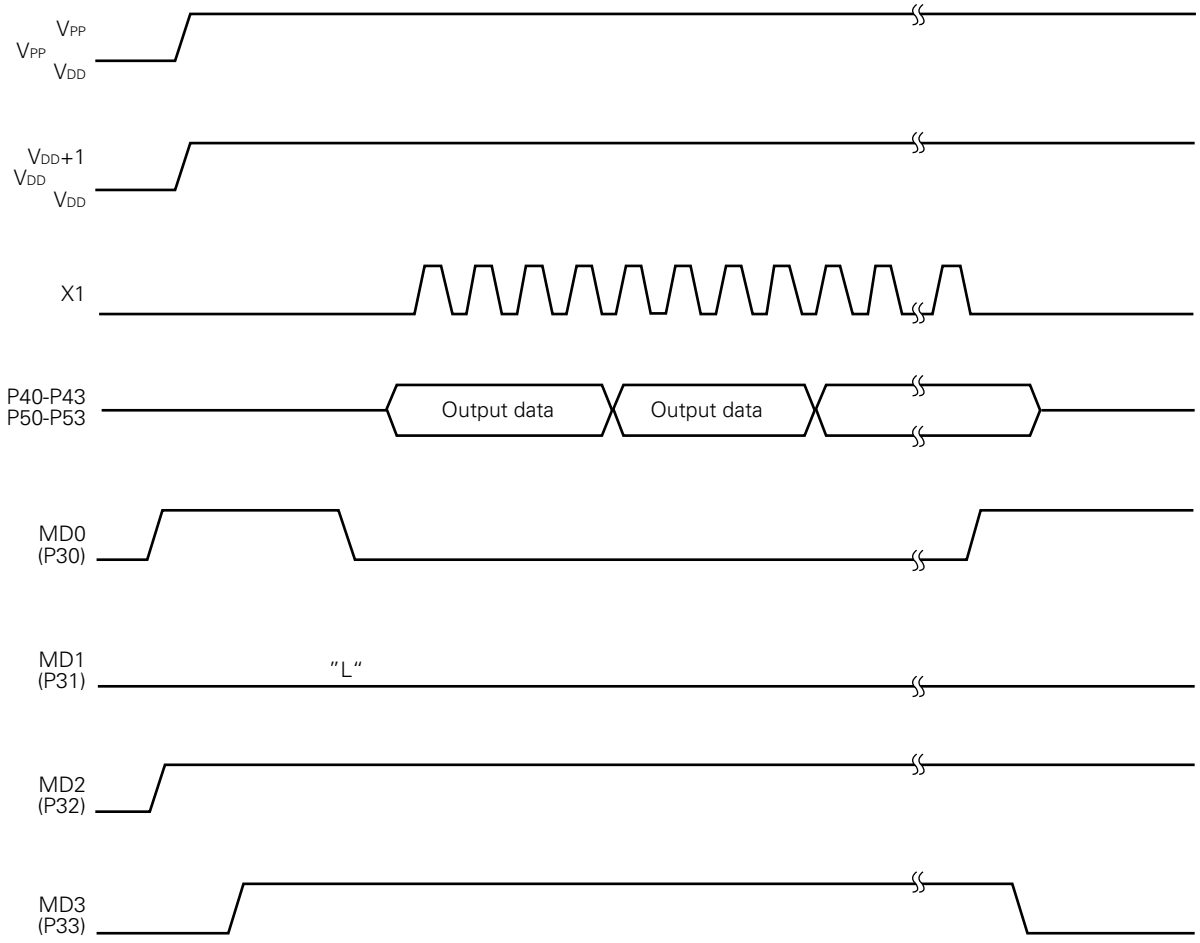


3.3 PROM READ PROCEDURE

The PROM contents can be read in the verify mode by using the following procedure: (see the following figure)

(1) Pull unused pins to V_{SS} through resistors. Set the X1 pin low.
(2) Supply 5 volts to the V_{DD} and V_{PP} pins.
(3) Wait for 10 μs.
(4) Select the zero clear program memory address mode.
(5) Supply 6 volts to the V_{DD} and 12.5 volts to the V_{PP} pins.
(6) Select the program inhibit mode.
(7) Select the verify mode. Apply four pulses to the X1 pin. Every four clock pulses will output the data stored in one address.
(8) Select the program inhibit mode.
(9) Select the zero clear program memory address mode.
(10) Return the V_{DD} and V_{PP} pins back to + 5 volts.
(11) Turn off the power.

Fig. 3-2 Timing of Program Memory Read



4. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_a = 25 °C)

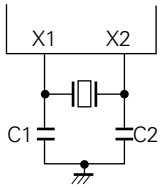
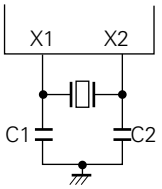
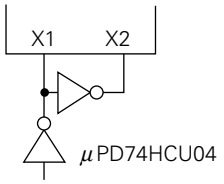
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +7.0	V
	V_{LOAD}		V_{DD} –40 to V_{DD} + 0.3	V
	V_{PP}		–0.3 to +13.5	V
Input voltage	V_I		–0.3 to V_{DD} +0.3	V
Output voltage	V_O	Other than display pins	–0.3 to V_{DD} +0.3	V
	V_{OD}	Display pins	V_{DD} –40 to V_{DD} + 0.3	V
High-level output current	I_{OH}	Single pin; other than display pins	–15	mA
		Single pin; S0 – S9	–15	mA
		Single pin; T0 – T15	–30	mA
		Total of all pins other than diplay	–20	mA
		Total of all display pins	–120	mA
Low level output current	I_{OL}	Single pin	17	mA
		Total of all pins	60	mA
Operating temperature	T_{opt}		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Operating Supply Voltage (T_a = –10 to + 70 °C)

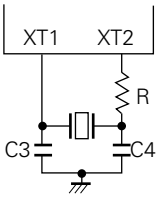
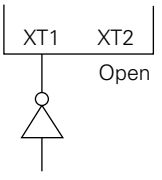
Parameter	Conditions	MIN.	MAX.	Unit
CPU Note		4.5	5.5	V
Display controller		4.5	5.5	V
Timer/pulse generator		4.5	5.5	V
Other hardwares Note		4.5	5.5	V

Note Except system clock oscillation circuit, display controller, timer/pulse generator.

Main System Clock Configurations (T_a = –10 to +70 °C, V_{DD} = 5 V ± 10 %)

Resonator	Recommended constants	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Note 1 Oscillation frequency (f_{XX})	V_{DD} = Oscillator operating voltage range	2.0		5.0 Note 3	MHz
		Note 2 Oscillation stabilization time	After V_{DD} reaches the minimum oscillator operating voltage range			4	ms
Crystal resonator		Note 1 Oscillation frequency (f_{XX})		2.0	4.19	5.0 Note 3	MHz
		Note 2 Oscillation stabilization time				10	ms
External clock		Note 1 X1 input frequency (f_X)		2.0		5.0 Note 3	MHz
		X1 input high- and low-level width (t_{XH}, t_{XL})		100		250	ns

Subsystem Clock Configurations (T_a = –10 to +70 °C, V_{DD} = 5 V ± 10 %)

Resonator	Recommended constants	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Note 1 Oscillation frequency (f_{XT})		32	32.768	35	kHz
		Note 2 Oscillation stabilization time			1	2	s
External clock		XT1 input frequency (f_{XT})		32		100	kHz
		X1 input high- and low-level width (t_{XTH}, t_{XTL})		10		32	μs

Note 1. The oscillation frequency and input frequency only indicate the characteristics of the oscillation circuit. Refer to the AC characteristics for the instruction execution time.

2. The oscillation stabilization time is the time until the oscillation enters a stable state after the application of V_{DD} or the release of STOP mode.

★ **3.** When the oscillation frequency is 4.19 < f_X ≤ 5.0 MHz, PCC = 0011 should not be selected as the instruction execution time. If PCC = 0011 is selected, 1 machine cycle is less than the specified minimum value, which is 0.95 μs.

Capacitance (T_a = 25 °C, V_{DD} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance		C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V			15	pF
Output capacitance	Other than display output	C_{OUT}				15	pF
	Display output					35	pF
Input/Output capacitance		C_{IO}				15	pF

DC Characteristics (T_a = –10 to +70 °C, V_{DD} = 5 V ± 10 %)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	All except ports 0, 1, 6, X1, X2, XT1, $\overline{RESET}$		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Port 0, 1 $\overline{RESET}$		0.75 V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2, XT1		V_{DD}–0.4		V_{DD}	V
	V_{IH4}	Port 6		0.65 V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL1}	All except ports 0, 1, 6, X1, X2, XT1, $\overline{RESET}$		0		0.3 V_{DD}	V
	V_{IL2}	Port 0, 1, 6 $\overline{RESET}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
High-level output voltage	V_{OH}	All outputs	I_{OH} = –1 mA	V_{DD}–1.0			V
			I_{OH} = –100 μA	V_{DD}–0.5			V
Low-level output voltage	V_{OL}	Port 4, 5	I_{OL} = 15 mA		0.4	2.0	V
		All outputs	I_{OL} = 1.6 mA			0.4	V
High-level input leakage current	I_{LIH1}	All except X1, X2, XT1	$V_I = V_{DD}$			3	μA
	I_{LIH2}	X1, X2, XT1				20	μA
Low-level input leakage current	I_{LIL1}	All except X1, X2, XT1	V_I = 0 V			–3	μA
	I_{LIL2}	X1, X2, XT1				–20	μA
High-level output leakage current	I_{LOH}	All outputs	$V_O = V_{DD}$			3	μA
Low-level output leakage current	I_{LOL1}	All except display output	V_O = 0 V			–3	μA
	I_{LOL2}	Display outputs	$V_O = V_{LOAD} = V_{DD}$ – 35 V			–10	μA
Display output current	I_{OD}	S0 - S9	$V_{OD} = V_{DD}$ – 2 V	–3	–5.5		mA
		T0 - T15		–15	–22		mA
On-chip pull-down resistor	R_L	Display outputs	$V_{OD} – V_{LOAD}$ = 35 V	25	70	135	kΩ
Power supply current Note 1	I_{DD1}	4.19 MHz Crystal oscillator C1 = C2 = 15 pF	Note 2		3.0	9.0	mA
	I_{DD2}		HALT mode		600	1 800	μA
	I_{DD3}	32.768 kHz Note 3 Crystal oscillator			100	300	μA
	I_{DD4}		HALT mode		40	100	μA
	I_{DD5}	XT1 = 0 V	STOP mode		0.5	20	μA

Note 1. Does not include the current for the on-chip pull-down resistor (output circuit to S0 to S8, T0 to T9).

2. When the processor clock control register (PCC) is set to 0011 and operated in high-speed mode.

3. When the system clock control register (SCC) is set to 1001 to stop the main system clock, and when the sub-system clock is used.

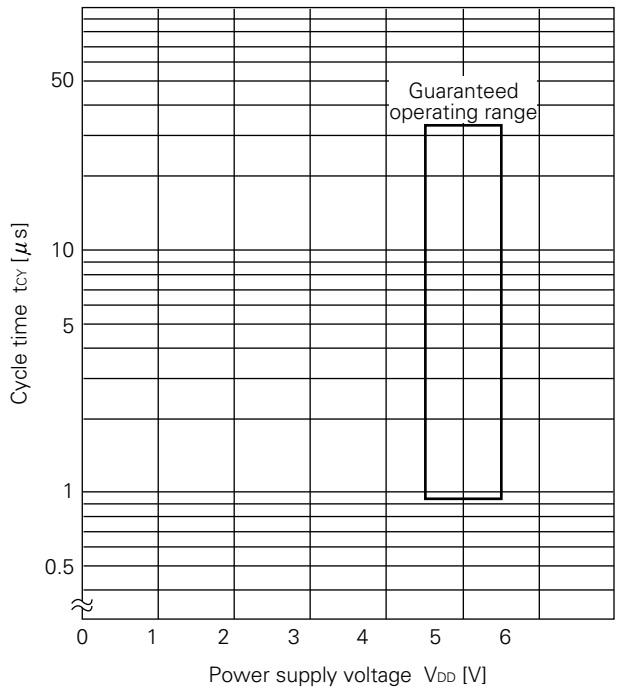
AC Characteristics (T_a = –10 to +70 °C, V_{DD} = +5 V ±10%)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU clock time Note 1 (minimum instruction execution time = 1 machine cycle)	t_{CY}	Main system clock		0.95		32	μs
		Subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}			0		0.6	MHz
TI0 input high- and low-level width	t_{TIH}, t_{TIL}			0.83			μs
$\overline{SCK}$ cycle time	t_{KCY}		Input	0.8			μs
			Output	0.95			μs
$\overline{SCK}$ high- and low-level width	t_{KH}, t_{KL}		Input	0.4			μs
			Output	t_{KCY}/2-50			ns
SI setup time (to $\overline{SCK}$ ↑)	t_{SIK}			100			ns
SI hold time (to $\overline{SCK}$ ↑)	t_{KSI}			400			ns
$\overline{SCK}$ ↓ → SO output delay time	t_{KSO}					300	ns
Interrupt inputs high- and low-level width	t_{INTH}, t_{INTL}		INT0	Note 2			μs
			INT1	$2t_{CY}$			μs
			INT2, 4	10			μs
$\overline{RESET}$ low-level width	t_{RSL}			10			μs

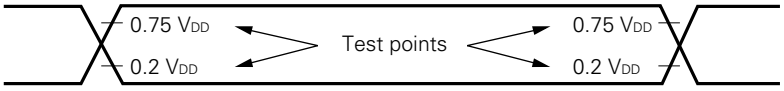
Note 1. The CPU clock (ø) cycle time is decided by the oscillation frequency of the resonator, system clock control register (SCC), and processor clock control register (PCC).
The figure to the right indicates cycle time (t_{CY}) characteristics for supply voltage V_{DD} when using the main system clock.

2. This is $2t_{CY}$ or $128/f_{XX}$ according to the interrupt mode register setting (IM0).

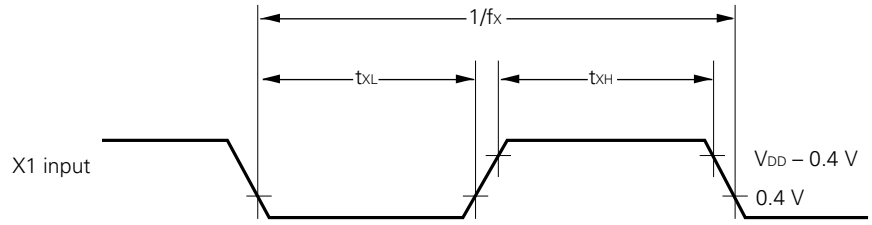
t_{CY} vs V_{DD} (Main system clock)

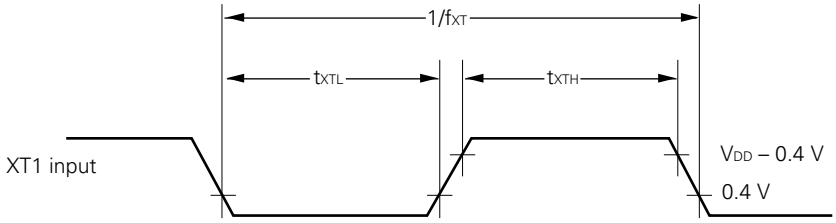


AC timing Test Point (Except X1, XT1)

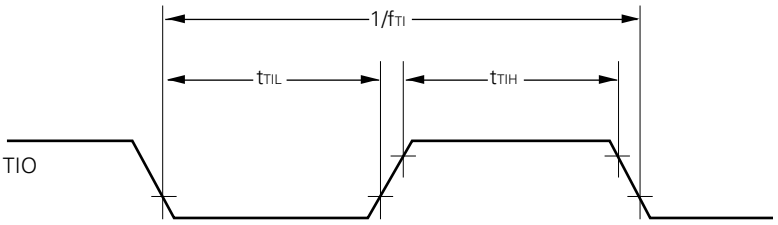


Clock Timing

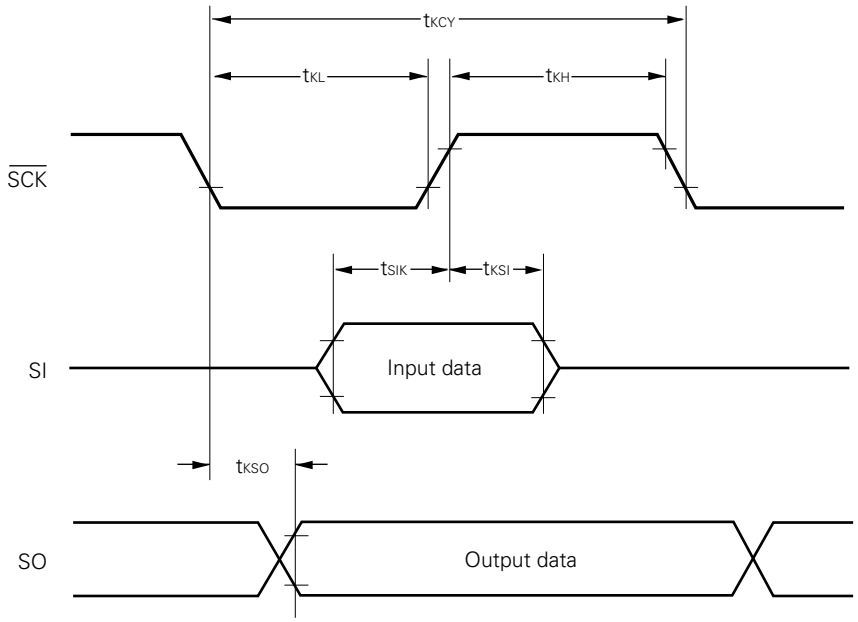




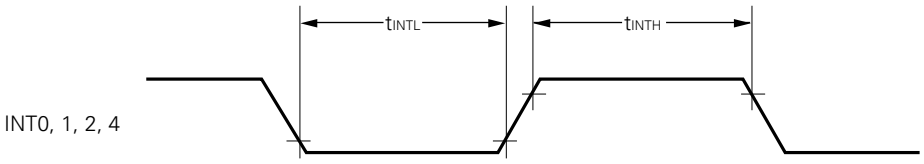
TIO Timing



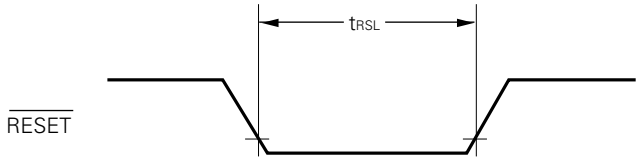
Serial Transfer Timing



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Data Memory STOP Mode Low Voltage Data Retention Characteristics (T_a = –10 to +70 °C)

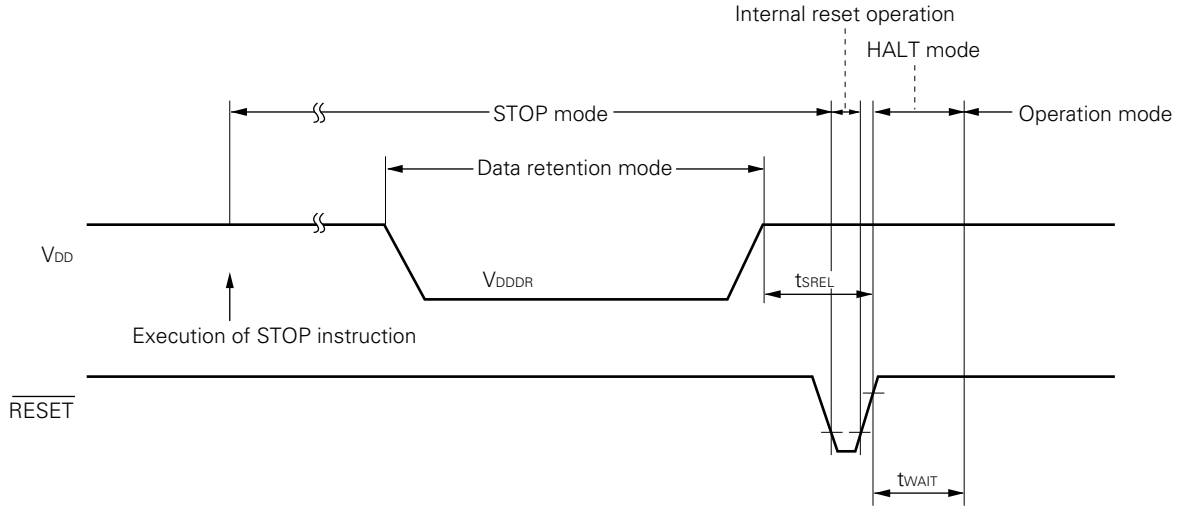
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}		2.0		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Released signal SET time	t_{SREL}		0			μs
Oscillation stabilization time Note 1	t_{WAIT}	Released by $\overline{RESET}$ input		$2^{17}/f_X$		ms
		Released by interrupt request		Note 2		ms

Note 1. The oscillation stabilization wait time is a period during which the CPU is kept inactive in order to avoid unstable operation at the start of oscillation.

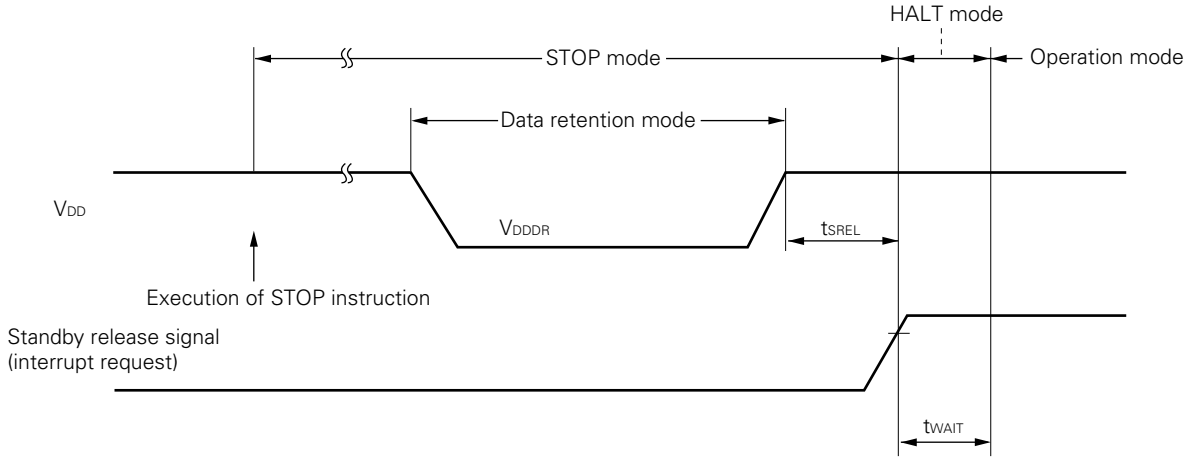
2. Depends on the setting of the basic interval time mode register (BTM) (see the following table).

BTM3	BTM2	BTM1	BTM0	Wait time ( ): f_{XX} = 4.19 MHz
—	0	0	0	$2^{20}/f_{XX}$ (approx. 250 ms)
—	0	1	1	$2^{17}/f_{XX}$ (approx. 31.3 ms)
—	1	0	1	$2^{15}/f_{XX}$ (approx. 7.82 ms)
—	1	1	1	$2^{13}/f_{XX}$ (approx. 1.95 ms)

Data Retention Timing (STOP mode is released by $\overline{RESET}$ input)



Data Retention Timing (Standby release signal: STOP mode is released by interrupt signal)



DC Programming Characteristics (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	All except X1, X2	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD}–0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	All except X1, X2	0		0.3 V_{DD}	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	I_{L1}	V_{IN} = V_{IL} or V_{IH}			10	μA
High-level output voltage	V_{OH}	I_{OH} = –1 mA	V_{DD}–1.0			V
Low-level output voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} power supply current	I_{DD}				30	mA
V_{PP} power supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Note 1. V_{PP} should not exceed +22 V (including overshoot).

2. V_{DD} should be applied before V_{PP} and turned off after V_{PP}.

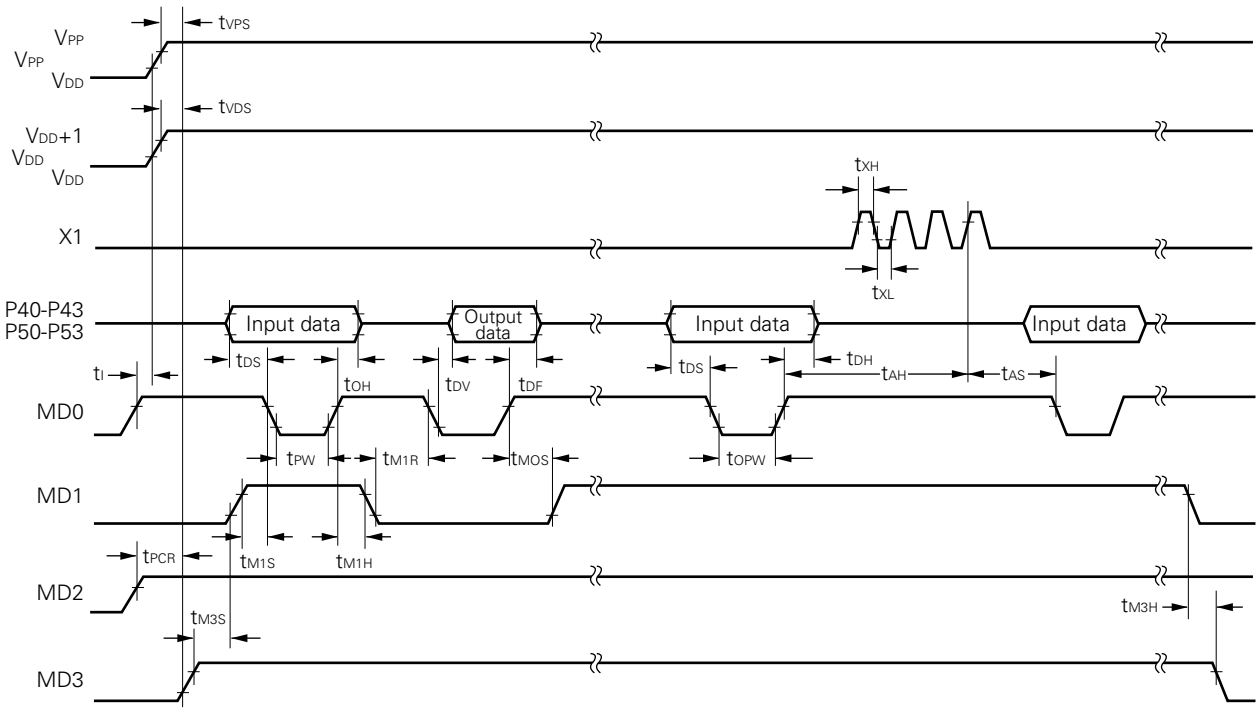
AC Programming Characteristics (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Note 1	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time Note 2 (toMD0↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (to MD0↓)	t_{MIS}	t_{OES}		2			μs
Data setup time (to MD0↓)	t_{DS}	t_{DS}		2			μs
Address hold time Note 2 (from MD0↑)	t_{AH}	t_{AH}		2			μs
Data hold time (from MD0↑)	t_{DH}	t_{DH}		2			μs
MD0 ↑ → data output float delay time	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (to MD3↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (to MD3↑)	t_{VDS}	t_{VCS}		2			μs
Initialized program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (to MD1↑)	t_{MOS}	t_{CES}		2			μs
MD0 ↓ → data output delay time	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (from MD0↑)	t_{MIH}	t_{OEH}	t_{MIH} + t_{MIR} ≥ 50 μs	2			μs
MD1 recovery time (to MD0↓)	t_{MIR}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	—		10			μs
X1 input high- and low-level width	t_{XH}, t_{XL}	—		0.125			μs
X1 input frequency	f_X	—				4.19	MHz
Initial mode set time	t_I	—		2			μs
MD3 setup time (to MD1↑)	t_{M3S}	—		2			μs
MD3 hold time (from MD1↓)	t_{M3H}	—		2			μs
MD3 setup time (to MD0↓)	t_{M3SR}	—	During program read cycle	2			μs
Address Note 2 → Data output delay time	t_{DAD}	t_{ACC}	During program read cycle	2			μs
Address Note 2 → Data output hold time	t_{HAD}	t_{OH}	During program resd cycle	0		130	ns
MD3 hold time (from MD0↑)	t_{M3HR}	—	During program read cycle	2			μs
MD3 ↓ → data output float delay time	t_{DFR}	—	During program read cycle	2			μs

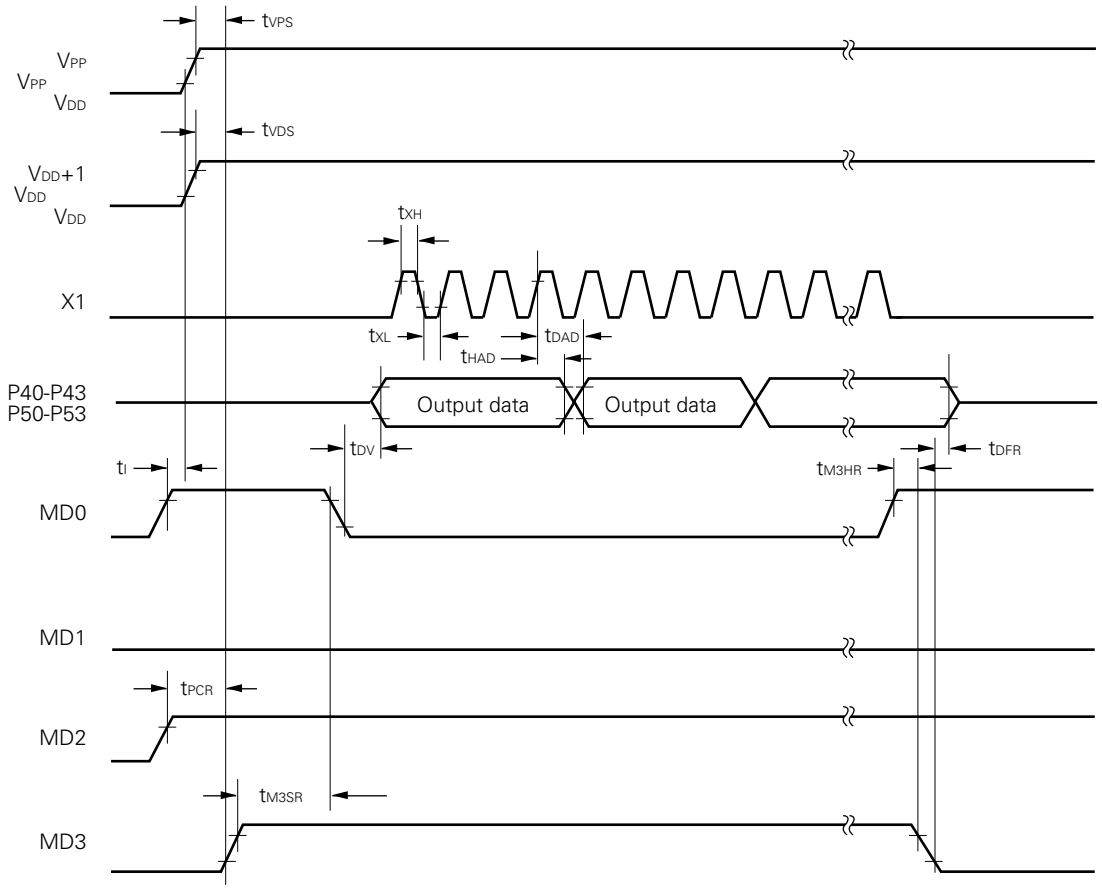
Note 1. Symbol of corresponding μPD27C256.

2. Internal address is incremented by 1 at the rising edge of the fourth X1 input. This address signal is not output to external pins.

Program Memory Write Timing

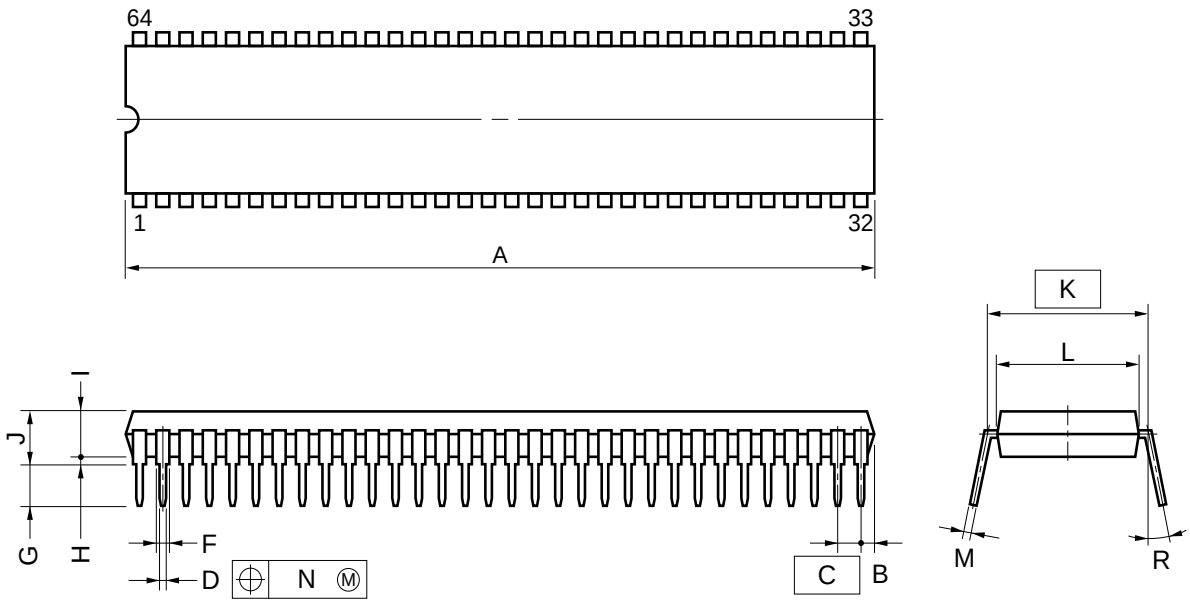


Program Memory Read Timing



5. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

6. RECOMMENDED SOLDERING CONDITIONS ★

The following conditions must be met when soldering this product.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207)**.

Please consult with our sales offices in case other soldering process is used, or in case other soldering is done under different conditions.

Table 6-1 Type of Through Hole Device

μPD75P216ACW: 64-pin plastic shrink DIP (750 mil)

Soldering process	Soldering conditions
Wave soldering (only lead part)	Solder temperature: 260 °C or lower, Flow time: 10 seconds or less
Partial heating method	Pin temperature: 260 °C or lower, Time: 10 seconds or less

Caution This wave soldering should be applied only to lead part, and don't jet molten solder on the surface of package.

★ APPENDIX DEVELOPMENT TOOLS

The following development tools are provided for the development of a system which employs the μPD75P216A.

Language processor

RA75X relocatable assembler	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS™ (Ver. 3.10 to Ver. 3.30C)	3.5-inch 2HD	μS5A13RA75X
			5-inch 2HD	μS5A10RA75X
	IBM PC series	PC DOS™ (Ver. 3.1)	5-inch 2HC	μS7B10RA75X

PROM programming tools

Hardware	PG-1500	The PG-1500 PROM programmer is used together with an accessory board and optional programmer adapter. It allows the user to program a single chip microcomputer containing PROM from a standalone terminal or a host machine. The PG-1500 can be used to program typical 256K-bit to 4M-bit PROMs.		
	PA-75P216ACW	PROM programmer adapter dedicated to μPD75P216ACW. Connect the programmer adapter to PG-1500 for use.		
	AF-9703 AF-9704	PROM programmer produced by Ando Electric Corp.		
	AF-9789	Programmer adapter dedicated to the μPD75P216ACW Connect to AF-9703, AF-9704 for use		
	UNISITE 2900 3900	PROM programmer produced by Data I/O Japan Corp.		
	PPI-0601	Programmer adapter dedicated to the μPD75P216ACW Connect to UNISITE, 2900, 3900 for use		
Software	PG-1500 controller	This program enables the host machine to control the PG-1500 through the serial and parallel interfaces.		
		Host machine / OS	Distribution media	Part number
		PC-9800 series / MS-DOS (Ver. 3.10 to Ver. 3.30C)	3.5-inch 2HD	μS5A13PG1500
			5-inch 2HD	μS5A10PG1500
		IBM PC series / PC DOS (Ver. 3.1)	5-inch 2HC	μS7B10PG1500

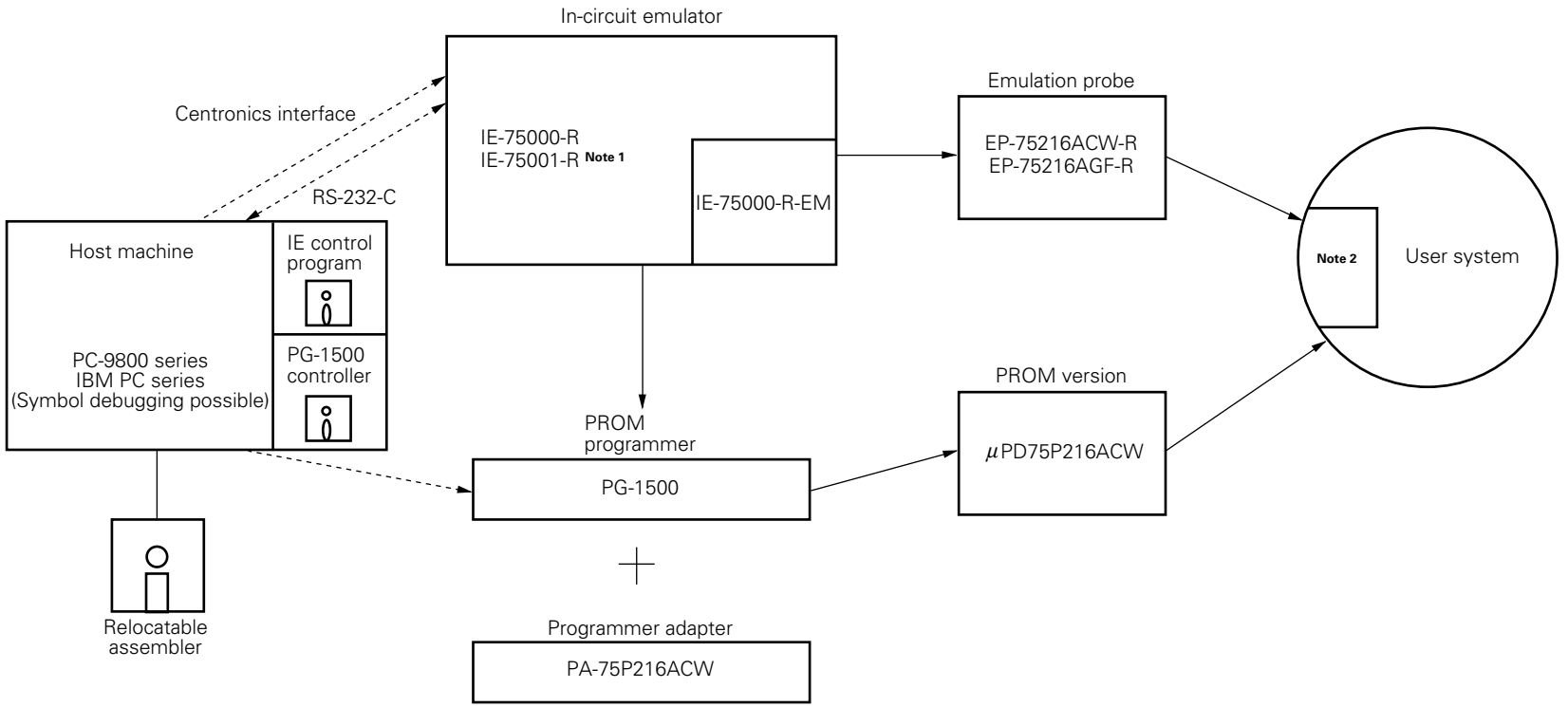
Debugging tools

Hardware	IE-75000-R [Note]	The IE-75000-R is an in-circuit emulator to debug the hardware and software at developing application system for 75X series. This emulator is used together with the emulation probe. For efficient debugging, the emulator is connected to the host machine and PROM programmer.		
	IE-75000-R-EM	The IE-75000-R-EM is an emulation board for the IE-75000-R and IE-75001-R. The IE-75000-R contains the emulation board. The emulation board is used together with the IE-75000-R or IE-75001-R to evaluate the μPD75P048.		
	IE-75001-R	The IE-75001-R is an in-circuit emulator to debug the hardware and software at developing application system for 75X series. This emulator is used together with the IE-75000-R-EM emulation board (option) and emulation probe. For efficient debugging, the emulator is connected to the host machine and PROM programmer.		
	EP-75216ACW-R	Emulation probe for the μPD75P216ACW. Connect this probe to the IE-75000-R or IE-75001-R and the IE-75000-R-EM for use.		
Software	IE control program	This program enables the host machine to control the IE-75000-R or IE-75001-R on the host machine through the RS-232-C interface.		
		Host machine		Part number
			OS	Distribution media	
		PC-9800 series	MS-DOS (Ver. 3.10 to Ver. 3.30C)	3.5-inch 2HD	μS5A13IE75X
				5-inch 2HD	μS5A10IE75X
		IBM PC series	PC DOS (Ver. 3.1)	5-inch 2HC	μS7B10IE75X

Notes Provided only for maintenance purposes.

Remark NEC is not responsible for the IE control program operation unless it runs on any host machine with the operation system listed above.

Configuration of Development Tools



Notes 1. IE-75001-R is not provided with IE-75000-R-EM (option)
2. EV-9200GC-64

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:
Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:
No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIAIZATION OF MOS DEVICES

Note:
Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

"μPD75216A USER'S MANUAL" (IEM-988F) is also prepared for this product (option).

M4 92.6