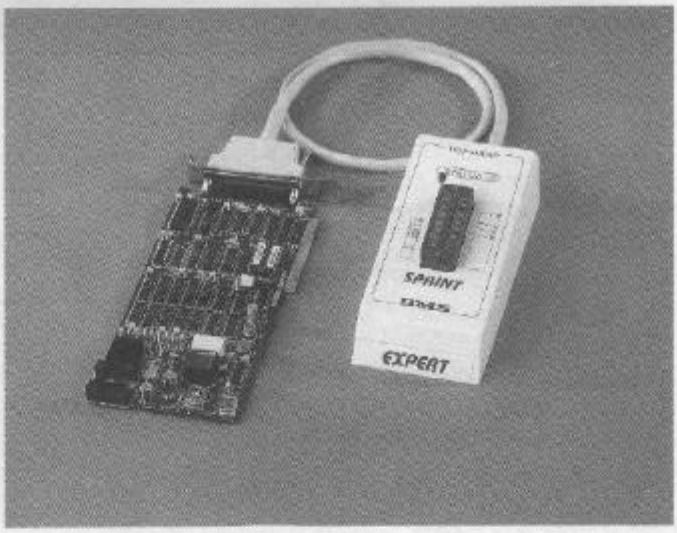
SMS SPRINT EXPERT, SPRINT TOP'S, SPRINT OPTIMA, SPRINT PLUS 48 BROCHURE

SPRINT EXPERT



Overview

The SPRINT EXPERT™ provides programming and vector testing for all of the latest in programmable device technologies. It supports thousands of PLDs, FPGAs, EPROMs, EEPROMs, and microcontrollers up to and beyond 84 pins; in a powerful universal programmer that fits on any desk or benchtop.

As a peripheral to your PC the SPRINT EXPERT utilizes the RAM, CPU and disk drives in the computer you already own. Simply install the SPRINT EXPERT controller card into any full sized slot on your PC, load the software and start programming. A key advantage to this approach is that you get high performance programming electronics that operate within your design environment. The lengthy download process that is associated with older generation programmers is virtually eliminated. The entire load/program/test cycle on the SPRINT EXPERT can be done in a fraction of the time it takes to download data through the RS232 port found on many programmers.

SPRINT EXPERT's full custom ASIC pindrivers make programming and testing the new high speed CMOS technologies a cinch. The compact design enables the pindriver output to be extremely close to the pin of the device, eliminating ground bounce problems experienced by many other programmers.

Standard Features

- TOP40DIP. Standard 40 pin DIP socket supports devices from 8-40 pins.
- Universal Pindrivers. Provide precise digital and analog signals on every pin.
- Device Support. PLDs, EPLDs, EEPLDs, PROMs, EPROMs, EEPROMs, GALs, FPLAs, and IFLs are supported regardless of package types.
- PC peripheral. Uses computer's existing RAM, disk, keyboard and display to provide maximum price/performance.
- Compact Design. Eliminates yield loss due to ground bounce.
- Full Screen Menus. The SPRINT EXPERT is easy to learn and operate.
- Batch Mode Operation. All key-stroke commands can be executed from a batch file.
- PLDASM. Assembly language for converting Boolean equations into JEDEC files for the popular PAL type architectures.
- 6 month warranty.

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Optional Features

- TOPIPLC. Universal TOP supports PLCC packages from 20 to 84 pins.
- Additional TOPs support other packages e.g., SOIC, PGA, QFP & SDIP.
- TOP432. Gang programming support for memory devices and PLDs.
- Handler Interface facilitates easy connection to a high speed device handler.
- Software Maintenance Plan (SMP). Affordable SMP keeps your programmer up-to-date with the latest algorithms and adds the following valuable software utilities to your programming system:

  UNASM. A reverse assembler for converting JEDEC files back to source files in the PLDASM format.
  Test Vector Editor. Tool for creating or editing test vectors.
  PLD Emulation. Cross programming tool for converting between PLD architectures.

Standard Accessories

- TOP40DIP
- 6 month warranty
- User manual
- System software

Specifications

General Architecture:
- Full custom ASIC's allow each programming pin to be universal.
- Internal hardware controls timing and waveform generation independent of other CPU operations.
- Relays switch power and ground to the proper pins.

User Ram:
- Virtual Memory Control. User RAM is only limited by the PC hardware and/or DOS version in use.

Devices Programmed:
- Memory: PROMs, EPROMs, EEPROMs.
- Logic: FPGAs, PLDs, PALs, IFLs, FPLAs.
- Other: microcontrollers and sequencers.

Device Operations: Read, blank check, program, verify, sumcheck, ID test. Automatically does illegal bit and continuity check during program.

System Operation: Set address, change device, execute DOS, input file, edit data, list memory, multiple device programming, write file.

Translation Formats: Binary, Ascii Hex, Intel 8/16/32 bit, 286/386 OMF, Mos Tech, Motorola 8/16/32 bit, Tek Hex, extended Tek Hex, JEDEC, POF

PC Requirements

DOS-based PC, AT, PS/2, 286, 386, 486 with open full sized slot. 640K RAM (minimum). Hard disk with 1 MB of available space. CGA, EGA, VGA, or LCD.

Environmental/ Physical Specifications

Temperature:
Operating - 50 F to 104 F (10 to 40 C)
Storage - 40 F to 122 F (4 to 50 C)

Humidity:
5 to 90% (noncondensing)

Operational Altitude:
0 to 10,000 ft (0 to 3048 m)

Dimensions:
2.5 x 3.375 x 8.125 in (6.35 x 8.57 x 20.63 cm)

Weight:
Operational - 3.5 lbs (1.59kg)
Shipping - 5.75 lbs (2.61 kg)
(Includes manual and shipping carton)

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SPRINT TOP's

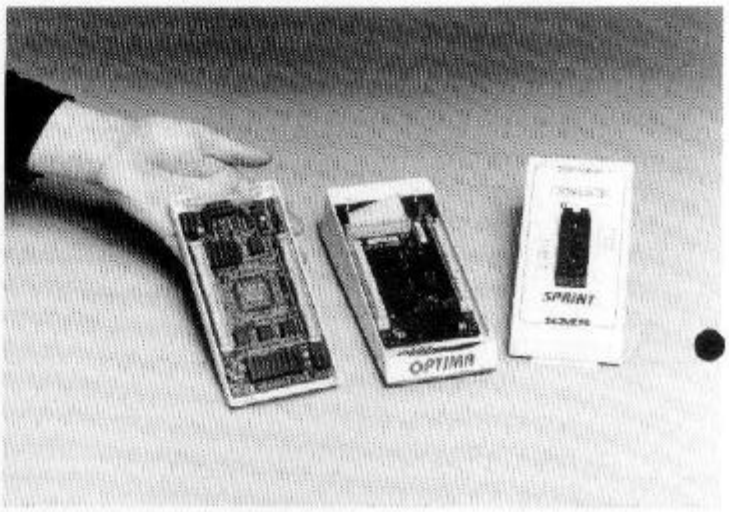
Description

TOP is the name for the socket-top of the new-generation of universal SPRINT programmers: SPRINT EXPERT, SPRINT OPTIMA and the SPRINT MULTISYTE series - DUAL, QUAD and OCTAL.

SPRINT programmer consist of two or three parts:
The SPRINT EXPERT and the MULTISYTE programmers include a PC plug-in card, a programming base and one (or several) TOP's. The SPRINT OPTIMA consists of two parts - the programming base and the TOP.

The TOP's are an active component of the SPRINT programmers. They help in making the absolutely shortest connection between the pindrivers and the socket pins possible (less than 2 inches). The universal ASIC pindrivers and these shortest connections guarantee fastest programming and test algorithms.

As you can see on the photo, part of the SPRINT electronics is in the TOP. Additional ASIC pindrivers and relais in the TOP allow different pinconfigurations including GND- and Vcc-connections for devices up to 84 pins. The concept of "TOP ON BASE" can support devices exceeding 200 pins.



When the programmer is moved, the TOP can be locked to the base. Under normal operating conditions this is not required and allows a quick exchange of the TOP's: A guidance helps in the installation. The SPRINT software initializes the TOP and reports after an extensive soft- and hardwaretest "ready to use". The screen shows the TOP-specific list of supported devices. A LED informs about the status of the socket.

The SPRINT software performs on all TOP's before programming a reverse- and continuity-check on all pins (a few special devices are exempted).

When an operation like programming or testing is finished, the TOP can be exchanged. The programmer or the PC need not be turned off.

Depending on the markets needs, new TOP's can be developed quickly in a "SPRINT" to new devices. The direct connection of the SPRINT soft- and hardware to the PC guarantee flexibility and universality for the future developments on the semiconductor market.

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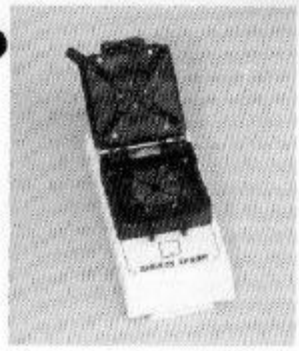
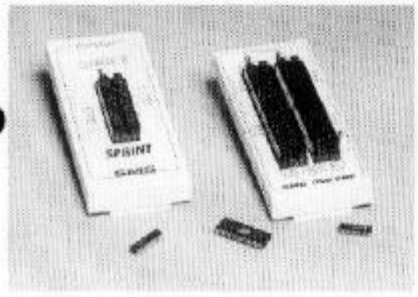
Specifications:



The TOP1PLC is a universal socket TOP for PLCC components with up to 84 pins. 84 special gold-contacts allow insertion of devices with 20, 28, 32, 44, 52, 68 or 84 pins. This includes the rectangular 32-pin PLCC package for programming and testing. The devices are put into the lid of the socket and are positioned and held by a special mechanism. When the lid is closed, the pins of the device are securely and precisely contacted. 84 universal ASIC pindrivers support many pinouts including Vcc and GND standards. JEDEC and non-JEDEC, 16 bit, microcontrollers, EPLD's, FPGA's, MACH's, MAX's and many more pinouts are supported.



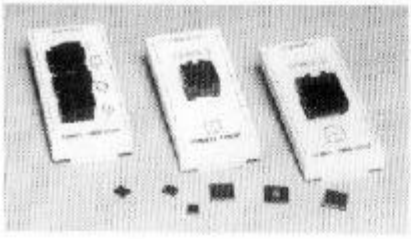
The TOP40DIP is included in the base package of SPRINT EXPERT and SPRINT OPTIMA. The TOP40DIP is for memory- and logic-devices with 8 to 40 pins in DIL packages. 40 universal ASIC pindrivers allow many pinouts and also vectortesting.

The TOP432DIP is designed for the programming of 4 memory devices in 8 bit JEDEC format. Four operating modes (one GANG-mode and three SET-modes) allow the user to handle different data formats. In GANG-mode 4 devices with up to 32 pins DIP can be programmed in parallel. Failing devices are ignored and LED's show the status of the individual sockets. With one socket (MASTER) data can be read. The three SET-modes allow processing of different data formats: 8 Bit SET, 16 Bit SET and 32 Bit SET. In the 8 Bit SET mode, large datafiles are distributed into smaller PROM's.

An example: 1 Megabit of data can be programmed into four 256 kBit EPROM's. The first 256 kBit go into the first EPROM, the second 256 kBit into the second EPROM and so on . The 16 Bit SET-mode divides 16 Bit data into two or four 8 Bit devices. The 16 Bit file is read in and can immediately be programmed into two or four PROM's. The 32 Bit SET mode distributes 32 Bit data into 4 PROM's. The first byte goes into the first PROM, the second byte into the second PROM, the third into the third, the fourth into the fourth and the fifth byte into the first PROM again, and so on. The SPRINT software formats the data memory automatically for this. When the TOP432DIP is used with the SPRINT MULTISYTE programmers, then programming speed can be quadrupled compared to the use of the TOP40DIP.

The TOP68 PGA supports 68-pin memory and logic devices in PGA-packages. 68 universal ASIC pindrivers allow testing with testvectors.

The TOP4M programs up to four memory-cards in JEIDA/PCMCIA format with 68 pins.



The photo shows (from the left) the TOP3PLC, the TOP44PLC and the TOP68PLC. The TOP3PLC supports PLCC/LCC memory and logic parts with 20, 28 and 32 pins. The TOP44PLC is for PROM's and PLD's in a PLCC/LCC package and the TOP68PLC for such devices with 68 pins. The additional universal pindrivers are located in the TOP. Lowinductance miniaturerelais allow pinouts with many Vcc and GND standards. The SPRINT software automatically displays the list of supported devices according to the installed TOP.

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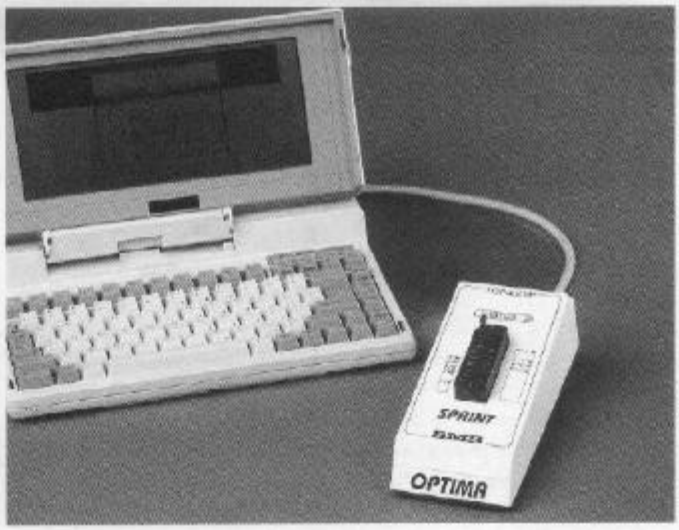
SPRINT OPTIMA



Overview

The SPRINT OPTIMA™ establishes a new standard in Professional Device Programmers. The SPRINT OPTIMA provides programming and vector testing for all of the latest in programmable device technologies. It supports thousands of PLDs, FPGAs, EPROMs, EEPROMs, and microcontrollers up to and beyond 84 pins, in a powerful universal programmer that fits in the palm of your hand.

As a peripheral to your PC, the SPRINT OPTIMA utilizes the RAM, CPU and disk drives in the computer you already own. Simply connect the SPRINT OPTIMA to any parallel port, load the software and start programming. A key advantage to this approach is that you get high performance programming electronics that operate within your design environment. The lengthy download process that is associated with older generation programmers is virtually eliminated. The entire load/program/test cycle on the SPRINT OPTIMA can be done in a fraction of the time it takes to download data through the RS232 port.

Full custom ASIC pindrivers make programming and testing the new high speed CMOS technologies a cinch. The compact design enables the pindriver output to be extremely close to the pin of the device, eliminating the ground bounce problems experienced by other programmers.

Any DOS computer with a standard Centronics printer port can control the SPRINT OPTIMA. Combine the compact design of the SPRINT OPTIMA with your favorite notebook and you have a portable programmer that is ready to go wherever your travels take you.

Standard Features

- TOP40DIP. Standard 40 pin DIP socket supports devices from 8-40 pins.
- Universal Pindrivers. Provide precise digital and analog signals on every pin.
- Device Support. PLDs, EPLDs, EEPLDs, PROMs, EPROMs, EEPROMs, GALs, FPLAs, and IFLs are supported regardless of package types.
- PC Peripheral. Uses computer's existing RAM, disk, keyboard and display to provide optimum price/performance.
- Compact Design. Eliminates yield loss due to ground bounce.
- Portable. Connects to any standard PC parallel port (LPT) providing complete portability between PCs.
- State Machine Waveform Generation. Internal crystal controlled state-machine insures accurate programming wave forms; not dependent on PC.
- Full Screen Menus. The SPRINT OPTIMA is easy to learn and operate.
- Batch Mode Operation. All keystroke commands can be executed from a batch file.
- PLDASM. Assembly language for converting Boolean equations into JEDEC files for the popular PAL type architectures.

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Optional Features

- TOPIPLC. Universal TOP supports PLCC packages from 20 to 84 pins.
- Additional TOPs support other packages e.g.: SOIC, PGA, QFP & SDIP.
- TOP432. Gang programming support for memory devices and PLDs.
- Handler Interface facilitates easy connection to a high speed device handler.
- Software Maintenance Plan (SMP). Affordable SMP keeps your programmer up-to-date with the latest algorithms and adds the following valuable software utilities to your programming system:

  UNASM. A reverse assembler for converting JEDEC files back to source files in the PLDASM format.
  Test Vector Editor. Tool for creating or editing test vectors.
  PLD Emulation. Cross programming tool for converting between PLD architectures.

Standard Accessoies

- TOP40DIP
- 6 month warranty
- User manual
- System software
- Power supply & line cord

Specifications

General Architecture:

- Full custom ASIC pindrivers, complex PLD, and a crystal oscillator control timing and waveform generation.
- Independent power supply insures accurate voltage levels independent of the host PC.
- LPT port provides programmer control and databus interface.

User Ram:

- Virtual Memory Control. User RAM is only limited by the PC hardware and/or DOS version in use.

Devices Programmed:

- Memory: PROMs, EPROMs, EEPROMs.
- Logic: FPGAs, PLDs, PALs, IFLs, FPLAs.
- Other: microcontrollers and sequencers.

Device Operations: Read, blank check, program, verify, sumcheck, ID test. Automatically does illegal bit and continuity check during program.

System Operation: Set address, change device, execute DOS, input file, edit data, list memory, multiple device programming, write file.

Translation Formats: Binary, Ascii, Hex Intel 8/16/32 bit, 286/386 OMF, Mos Tech, Motorola 8/16/32 bit, Tek Hex, extended Tek Hex, JEDEC, POE.

PC Requirements

DOS-based PC, AT, PS/2, 286, 386, 486 Desktop, Laptop or Notebook. 640K RAM (minimum). Hard disk with 1 MB of available space. CGA, EGA, VGA, or LCD. Centronics parallel port (8 data, 4 control, 5 status, ground).

Electrical Requirements

Operation Voltages:
100 VAC to 250 VAC
Frequency Range: 47 to 63 Hz
Power Consumption: 25 VA max.

Environmental/ Physical specifications

Temperature:
Operating
50 F to 104 F (10 C to 40 C)
Storage
40 F to 122 F (4 C to 50 C)

Humidity:
5 to 90% (noncondensing)

Operational Altitude:
0 to 10,000 ft (0 to 3048 m)

Dimensions:
2.5 x 3.375 x 8.125 in
(6.35 x 8.57 x 20.63 cm)

Weight:
Operational - 3.5 lbs (1.59 kg)
Shipping - 5.75 lbs (2.61 kg)
(includes power supply, manual and shipping carton)

Safety Standards:
UL CSA GS

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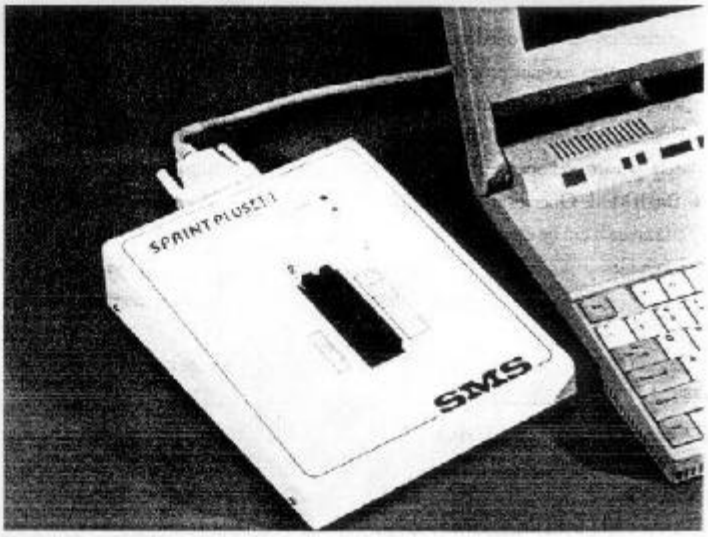
SPRINT PLUS48

Universal Device Programmer



General Description

The PLUS48 is the newest entry in the Sprint family of Universal Device Programmers. The PLUS48 comes complete with 48 universal pin drivers, setting a new standard in low cost Universal Device Programmers. The PLUS48 provides support for all of the most popular FPGAs, CPLDs, PLDs, Microcontrollers, EPROMs, and EEPROMs. Software libraries allow you to purchase the device support you need today, then you may purchase an additional library when your needs change.

Full custom ASIC pin drivers have been developed which enable the programming and testing of new high speed CMOS devices. A compact design is made possible through the use of these analog/digital ASICs. This allows the pin drivers, VCC and GRN relays to be placed as close to the pin of the device as possible, thus virtually eliminating ground bounce.

The PLUS48 is a PC peripheral that utilizes the RAM, CPU and Disk drive of the computer you already own. A key advantage to this approach is that you pay less for your computer electronics and you can choose the actual price/performance level you desire. It also eliminates file download times required by older standalone programmers.

Interface to the PC is through the standard parallel port. When the software is installed, it will automatically interrogate the LPT ports to determine where the programmer is attached and then configure itself.

Any DOS computer with a printer port can control the PLUS48. Combine the compact design of the PLUS48 with your favorite Notebook and you have a portable programmer that is ready to go wherever your travels take you.

The PLUS48 comes standard with 48 fully universal pin drivers and a 48 pin DIP socket that accepts devices from 8 to 48 pins. Affordable adapters are available for larger DIP, PLCC and other SMD packages.

Specifications

Standard features

- Standard 48 pin DIP/ZIF socket supports devices from 8-48 pins.
- Larger pin count and non DIP devices supported via adapters.
- Simple Device Libraries provide affordable entry level.
- Universal Pin Drivers provide precise digital and analog signals on every pin.
- Device Support: FPGAs, CPLDs, PLDs, Microcontrollers, EPROMs, and EEPROMs.
- PC peripheral. Uses computer's existing RAM, Disk, Keyboard and Display to provide maximum price/performance.
- Portable. Connects to any standard PC parallel port (LPT) providing complete portability between PCs.
- Compact Design eliminates yield loss due to ground bounce.

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Service means satisfaction

- State Machine Waveform Generation. Internal crystal controlled statemachine insures accurate programming waveforms; not dependent on PC.
- Full Screen Menus make the PLUS48 easy to learn and operate.
- Batch Mode Operation. All keystroke commands can be executed from a batch file.

Versions:
Version 1
FPGAs, CPLDs, PLDs, micros, EEPROMs, EPROMs with up to 32 pins

Version 2
FPGAs, CPLDs, PLDs, micros, EPROMs, EEPROMs with up to 48 pins. Larger pin count supported via adapter.

Can easily be upgraded from level 1 to level 2 with keyfax.

PC requirements
DOS based PC, AT, PS/2, 286, 386, 486, Laptop or Notebook.
640K RAM (minimum).
Hard disk with 1 Megabyte of space available.
CGA, EGA, VGA, or LCD.
Centronics Parallel Port (8 data, 4 control, 5 status, ground).

General architecture
- Full custom ASIC pin drivers and a complex PLD control timing and waveform generation.
- On board crystal and independent power supply insure critical timing and voltage levels independent of the PC.
- LPT port provides programmer control and databus interface.

Devices programmed
- Memory: PROMs, EPROMs, EEPROMs.
- Logic: FPGAs, CPLDs, PLDs, PALs, IFLs, FPLAs
- Other: Microcontrollers and Sequencers.

Device operations
Read, blank check, program, verify, sum check, ID test. Automatically does illegal bit and continuity check during program.

System operation
Set address, change device, execute DOS, input file, edit data, list memory, multiple device programming, write file.

Translation formats
JEDEC, POF, Binary, Intel 8/16/32 bit, Motorola 8/16/62 bit, 286/386 OMF, Tek Hex, ASCII Hex, MOS Tech

Standard accessories
48 pin DIP/ZIF socket
User manual
System software
Power supply & line cord

Electrical requirements
Operation Voltages: 100 to 250 VAC
Frequency Range: 47 to 63 Hz
PowerConsumption: 25w

Environmental/physical specifications
Temperature: Operating - 50 F to 104 F (10 C to 40 C)
Storage - 40Fto122F (4Cto50C)

Humidity: 5 to 90 % (noncondensing)

Operational Altitude:
0 to 10,000 ft (0 to 3048 m)

Dimensions:
1 x 7 x 8 in. (2.56 x 17.9 x 20.5 cm)

Weight: Operational - 3.5 lbs (1.59 kg)
Shipping 5.75 lbs (2.61 kg)
(includes power supply, manual and shipping carton)

Safety Standards: UL CSA GS

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