Operating Manual for RS PP40 and RS PP41 Gang Programmers

Manual Revision 2

This product is supplied by : RS Components Limited, P.O. Box 99, Corby, Northants NNI7 9RS

Tel: 0536 201234

Fax: 0536 201501

Tlx: 342512

Addendum

Note: These additions will be incorporated into the PP40 series manual at the next revisional reprint.

Additions to Existing Manual (PP40, PP41 and PP42 Rev.1)

Additional 'Set' Commands - pages 1.5-01 and 1.5-03

Set Verify: This allows selection of 'Normal' verify and 'Margin' verify. Normal verification is carried out with Vcc at a steady 5V (typical). Margin verification is carried out with Vcc being taken 5% higher and 5% lower than normal. Press Set followed by Verify. Interchange between Normal and Margin is made by pressing the vertical cursor keys. Press Exit to confirm.

Set Program: Allows the selection of pre-program checks. The options are: illegal bit; empty and none. Press Set followed by Program. Interchange between the options is made by pressing the vertical cursor keys. Press Exit to confirm.

I/O Formats

Please disregard Section 6.8.1 of the manual - Binary. The two binary formats available on the PP41 and PP42 are DEC Binary and binary rubout. DEC binary is described in the existing manual.

Binary Rubout

The programmer display for binary rubout is BINR.

Binary rubout is similar to binary in that it is devoid of address, stop code and checksum. The data is however preceded by the rubout (delete) character 7F.

Remote Commands for Filling the PP41/PP42 RAM

The commands are:

FF^ - to fill with FFs

00 ^ - to fill with 00s

Remote Commands for Setting the PP42 Set Configuration

The set configuration command takes the form:

ABCDD22]

where:

A - can be I or D for Identical or Different data.

B - is the number of devices per set (in decimal).

C - number of sets (in decimal).

DD - bit mode (expressed in hexadecimal e.g. 08,10 or 20).

22] - command.

For example:

1160822] - 8-bit gang mode with 6 devices.

D221022] - 16-bit mode with two different sets of two devices each.

New Modules

40M101, 41M101 and 42M101

Description

These three modules program MOS PROMs, EPROMs and EEPROMs in 24,28 and 32-pin DIL packages.

Operation

These modules function in a similar manner to the 40M100, 41M100 and 42M100 modules respectively as detailed in the manual apart from one function.

Set DE - to erase Seeq 48128 devices.

Press Set followed by D and E. If the wrong device type is selected, the message 'NOT APPLICABLE' will be returned. If the correct device type is selected, erasure will take place.

Warning: Extreme care should be taken to ensure that only Seeq 48128 devices are socketed when the Device Erase function is used. Failure to comply may result in damaged devices for which Stag and the semiconductor manufacturers can take no responsibility.

40M102 and 41M102

Description

These modules program 40-pin DIL EPROMs and EEPROMs from most major manufacturers.

Operation

These modules function in essentially the same way as the 40M100 and 41M100 as detailed in the manual apart from one major difference. The 'M100 modules handle 8-bit data but the 'M102 modules handle 16-bit data. In the case of the 41M102 where there is a RAM editor present, the data displayed in functions such as List, Edit, Delete etc. will be in the form of a double byte (4 hex. digits) for any given address.

41M200 - compatible with PP41 and PP42 mainframes.

Description

The 41M200 module will gang program 40-pin DIL, single chip microcomputers with data loaded into RAM from a master micro, a master EPROM, direct keyboard entry or via one of the dual RS232C ports.

Operation

The 41M200 operates in almost the same way as the 41M100 but for the following exceptions:

Loading of Data from a Master Device

Data can be loaded from a master micro or from a master EPROM. To select between the two master sockets, press Set followed by Load. This will display the default state 'MASTER MICRO', which indicates that the 40-pin micro socket is to be used. To interchange between either of the sockets, use the vertical cursor keys. Press Exit to confirm. A green LED will illuminate adjacent to Pin 1 of the relevant socket. To load the data, insert the master device and press Load. Data will be loaded from addresses corresponding to the size of the selected micro to be programmed. The address limits can however be altered see Section 3.9 of the manual.

Note: When loading data from a master EPROM, only 2764 and 27128 devices should be used. The master EPROM should be the only device socketed during loading.

Electronic Identifier

There is no Electronic Identifier function on the 41M200.

Margin Verify

There is no margin verify function on the 41M200

Security Bit Status

Certain devices such as the 8751H have a security bit. If this bit (bit 1) is blown, the device will function but the data cannot be read and no further programming of the device can be carried out. For devices with two security bits such as the 87C51, operation is slightly different. Blowing bit 1 will allow the device data to be read but will inhibit further programming and blowing bit 2 will not allow the device data to be read. To select the security bit status option, press Set F3. To interchange between bit 1 and bit 2, press the vertical cursor keys. To interchange between 'blown' and 'intact', press the horizontal cursor keys. Press Exit to confirm. The selected security bits will be blown after the device has verified following programming. The display will return the message 'VERIFIED/SECURED'.

CONTENTS

PP40, PP41 and PP42

Section	1 1.1 1.2 1.3 1.4 1.5	GENERAL INTRODUCTION Introduction Mainframe and Modules The Keyboard Initial Setting-up procedure List of 'SET' Commands
Section	2. 2.1 2.2	SELECTING A DEVICE Device Type Selection Electronic Identifier
Section	3. 3.1 3.2 3.3 3.4 3.5 3.6 3.7 3.8 3.9	DEVICE FUNCTIONS Error Detection Load (PP41 and PP42 only) Checksum Empty Test Pre-Program Bit Test Programming In-Program Verify Device Address Limits—PP40 Device Address Limits—PP41 and PP42
		PP41 and PP42 only
	4. 4.1 4.2 4.3 4.4 4.5 4.6 4.7	RAM FUNCTIONS List Edit Insert Delete Block Move Filling The RAM String Search
Section	5. 5.1 5.2 5.3	INTERFACE Setting the Input/Output Interface Parameters Input and Output Parameters Error Reporting on Input/Output
Section	6. 6.1 6.2 6.3 6.4 6.5 6.6 6.7 6.8 6.8.1 6.8.2 6.9	FORMAT DESCRIPTIONS Interface Formats Intellec Hex ASCII Motorola S-Record Tek Hex Extended Tek Hex Stag Hex Binary and DEC Binary Binary DEC Binary MOS Technology

PP40, PP41 and PP42





SECTION 1

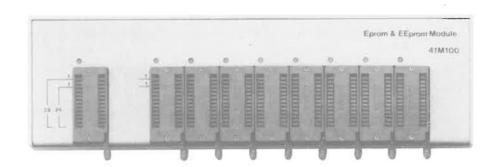
stag

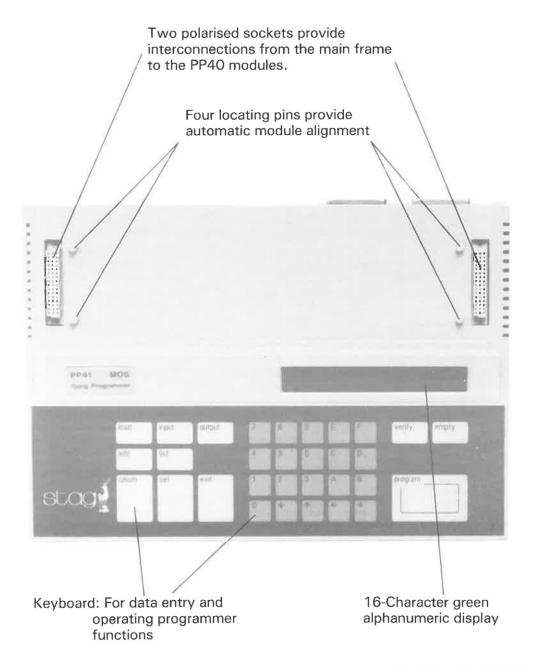
1.1 INTRODUCTION

The PP40, PP41 and PP42 are high-speed gang programmers, capable of supporting EPROMs and EEPROMs in CMOS and NMOS technology.

The programmers are software controlled using a single level module approach and have no need of adaptor modules. This ensures flexibility and ease of upgrade for future devices. The modules support NMOS and CMOS EPROM and EEPROM devices in both 24 and 28 pin DIL packages. They feature algorithms for fast programming and support Electronic Identifier technology for automatic device identification. The sockets all have bi-coloured LEDs to enhance socket status indication and error reporting. An auto-recall feature is incorporated whereby pre-set parameters are recalled from a non-volatile memory on power-up. These are the device and the I/O parameters.

PP41 MAINFRAME





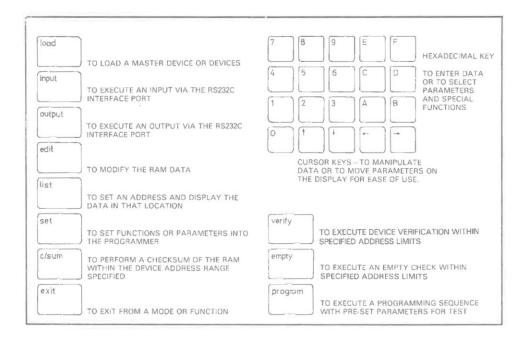
1.3 The Keyboard

For data entry and operating programmer functions.

PP40

set		7	8	9	E	F	
	TO SET FUNCTIONS OR PARAMETERS INTO THE PROGRAMMER				J		HEXADECIMAL KEY
c/sum	TO PERFORM A CHECKSUM NITHIN THE DEVICE ADDRESS RANGE	4	5	6	C	D	TO ENTER DATA OR TO SELECT PARAMETERS
exit	J SPECIFIED	1	2][3	A	В	AND SPECIAL FUNCTIONS
	TO EXIT FROM A MODE OR FUNCTION	0	1	1	7-	-	
verify	TO EXECUTE DEVICE VERIFICATION WITHIN SPECIFIED ADDRESS LIMITS		DATA	OR TO	MOVE PA	ANIPULAT ARAMETER	RS ON
empty	TO EXECUTE AN EMPTY CHECK WITHIN SPECIFIED ADDRESS LIMITS		THE D	DISPLAY	FOR EAS	SE OF USE	
program							
	TO EXECUTE A PROGRAMMING SEQUENCE WITH PRE-SET PARAMETERS FOR TEST						

PP41/PP42

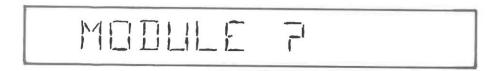


1.4 INITIAL SETTING UP PROCEDURE

Before attempting to apply power to your programmer ensure that it is set to the correct operating voltage for your power source. The voltage setting will be printed on the rear panel.

- 1. Plug the supplied power cable into the back panel socket.
- 2. Apply power to the machine from the power source.
- 3. Switch on the machine using the ON/OFF switch on the rear panel.

After "POWER ON" and without a Module inserted the display will read:



The main frame software revision can now be ascertained prior to the module being inserted simply by pressing the key marked 'SET' followed by the key marked '6', eg:



In order to make this manual as straightforward as possible the action of pressing the key marked 'SET' followed by another key or keys will be abbreviated to a single instruction, eg. 'SET 6', 'SET F6'.

Note

To ensure correct initialization, power down before inserting a module. Always wait two seconds before applying power again.

1.5 PP40 LIST OF 'SET' COMMANDS

set 0	Allows user to scan and select various manufacturers and device types.
set6	Displays module software revision if module is plugged in, or main frame software revision, if no module is plugged in.
set 8	Calculates and displays CRC (Cyclic Redundancy Check)
setEI	Allows the user to enter the two-key operation of the Electronic Identifier mode. The device signature is read and the manufacturer and device type are displayed. To execute the function the specified device function key must be pressed again, eg. Prog.
Set E2	Allows the user to enter the single-key operation of the Electronic Identifier mode. The device signature is read and the PP40 continues straight on to execute the selected function.
set F1	Audible Alarm: To indicate end of program, test, or as a warning using a combination of bleeps and tones. SET F1 can either enable or disable this function.
setF6	Defines device address range.

PP41/PP42 LIST OF 'SET' COMMANDS—Continued

setFI	Audible alarm: To indicate end of program, test, or as a warning using a combination of bleeps and tones. SET F1 both enables and disables this function.
set F2	
	Fills RAM with arbitrary variable across an arbitrary address range.
setF4	Re-locate RAM data. A block of data with pre- selected address limits can be copied and then re-located at another address within the RAM.
setF6	
	Defines RAM and device address ranges for all functions which operate on the device.
set input	
	Enters input address offset, start and stop addresses and port selection.
set out put	
	Enters output address offset, start address and stop address and port selection.

SECTION 2



stag

2.1 DEVICE TYPE SELECTION

Selecting the device using a 4 digit code

The complete range of devices supported by the programmer's module is stored in the EPROM. Each individual device has its own four digit code. (See device code list).

SET 0-Allows code selection

SEQUENCE: Prior to SET '0' the display will show the last entered configuration.

For example:



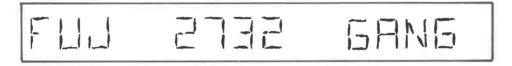
By pressing SET '0' the device code of this configuration will be displayed:



When the new device code to be entered is already known, (for example AF44 is the code for a Fujitsu 2732 EPROM device), then the AF44 can be entered directly onto the display from the keyboard replacing the old code.



The selection sequence can be completed by pressing EXIT whereupon the new manufacturer and device type are displayed.



2.2 ELECTRONIC IDENTIFIER

Important Note:

Devices which do not contain an Electronic Identifier can be irreparably damaged if they are used in the Electronic Identifier mode.

Electronic Identifier is a term used to describe a code mask programmed into a PROM which identifies the device type and manufacturer. The code is stored outside the normal memory array and is accessed by applying 12 Volts to address line A9. This allows the programmers directly to identify any devices containing an Electronic Identifier and thus eliminates the need for the user to select the device type.

The programmers presently uses two modes of Electronic Identifier operation both of which only work with 28 pin devices.

Mode (i): Two Key Operation

On pressing SET E1 the display will show:

ELECT IDENT GANG

If any device function key such as 'Program' is pressed, the programmer will first attempt to read the signature of any devices present. If no code can be read or the code is not found in the programmer's list of valid codes the display will show:



If any devices are successfully recognised but are incompatable ie. they use different programming algorithms the display will show:



If neither of the above two fault conditions occurs then the manufacturer and the device type will be displayed.

To execute the function the specified 'device function key' must be pressed again eg. Prog

To exit from the Electronic Identifier mode select a device using SET 0 in the usual manner.



stag

3.1 ERROR DETECTION

Connect Errors

The programmers have the ability to detect connect errors but the selected operation will not be interrupted unless the master socket or all the slave sockets have connect errors. In such a case the display will show:



Red LEDs indicate the failing socket(s).

Reversed or Faulty Device

If just one reversed or faulty device is detected, the selected operation stops immediately with the message:



Device Address Bus Check

If a fault such as a shorted address line is detected the selected operation will stop with the message:



3.2 PP41 and PP42 only

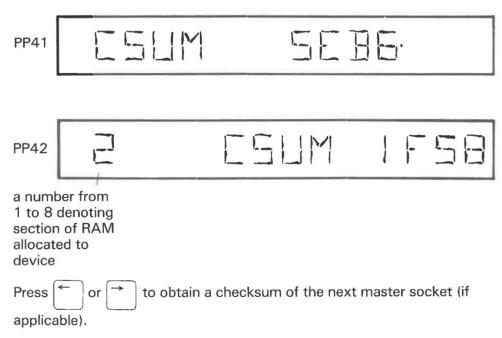
Note: For a full explanation of Bit mode configuration on the PP42 the user is advised to turn to section 10.

LOAD

Loading the RAM from a 'master' PROM

Insert the master devices into the master sockets. Press the load key.

The checksum will be displayed:

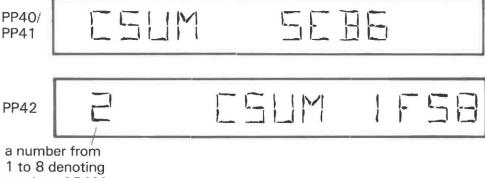


3.3 CHECKSUM

Press C/sum

to perform a checksum of the master device (PP40) or RAM (PP41, PP42)

The display will show:



1 to 8 denoting section of RAM allocated to device

Press to obtain a checksum of the next master socket if applicable.

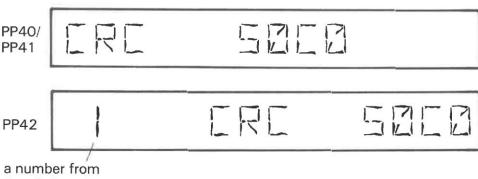
CYCLIC REDUNDANCY CHECK (CRC)

The Cyclic Redundancy check applies a continuous process of shifting and addition to the PROM data. This yields a coded representation of the data which is sensitive to the ordering of the data bytes, unlike the checksum which only considers their values.

Press SET 8

to perform a Cyclic Redundancy check on the master device (PP40) or RAM (PP41, PP42)

The display will show:



a number from 1 to 8 denoting section of RAM allocated to device

Press to obtain a Cyclic Redundancy check of the next master socket if applicable.

(D · · · 4) 0004

3.4 PROGRAMMING SEQUENCE

Empty Test

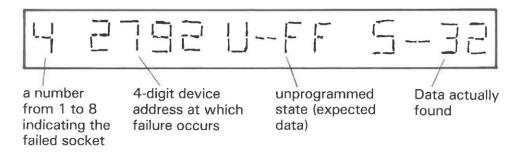
If required an 'empty test' can be applied to the device or devices in the slave sockets prior to programming. This can be done by pressing the 'empty' key. The device or devices will be examined for the unprogrammed state and if they are entirely empty the display will show thus:



Should a device fail the 'empty test' the display will show:



Red LEDs indicate the failed device(s). The cursor keys can be used to move to each in turn, and the display will change to give information of the format below:



s = slave device

While the failed device data is displayed the red LED flashes, but stops flashing when -> or <- is pressed to move to the next failed device.

Press EXIT

to skip to the next failing addresses.

Press EXIT

to return to Select Device mode.

If the empty test passes or is unnecessary the programming can begin.

Pressing the program key will automatically execute the 'program' sequence to the manufacturers' specifications with pre-program (Bit Test) and in-program (Verify) device tests.

3.5 PRE-PROGRAM BIT TEST

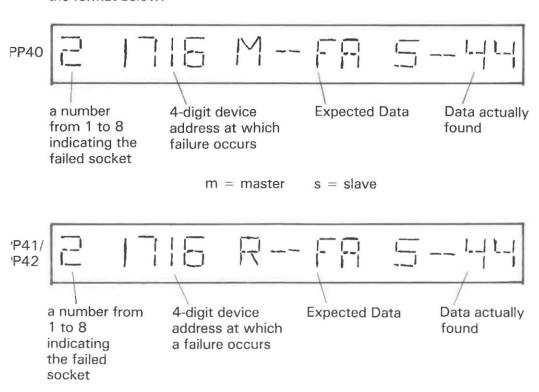
The programmers automatically check that the pattern already within the slave device is able to be programmed with the intended data from the master device (PP40), or RAM (PP41, PP42).

If a device passes the bit test, programming begins automatically.

Should a device fail the bit test, the display will show:



Red LEDs indicate the failed device(s). The cursor keys can be used to move to each in turn, and the display will change to give information of the format below:



When the failed device data is displayed the red LED flashes, but stops flashing when -> or <- is pressed to move to the next failed device.

S = slave

R = RAM

Press set to skip to the next failing addresses.

3.6 PROGRAMMING

Once the device has passed the bit test, programming of that device will start.

To provide an indication of how far programming has progressed at any given time the address being programmed is displayed; for example:

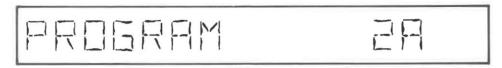
COUNTER



FOUR DIGIT ADDRESS

In the case of the larger devices which use a fast algorithm only the two most significant digits of the address are displayed.

COUNTER



TWO MOST SIGNIFICANT DIGITS OF THE ADDRESS

If the data to be programmed into a particular location is the same as the unblown state of that device, the programming sequence will automatically skip to the next location. This function speeds up programming considerably where large sections of the device are to remain empty.

3.7 IN-PROGRAM VERIFY

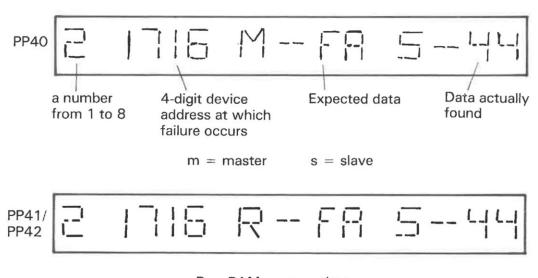
The algorithms of certain devices are such that an in-program verify is performed. This is a feature whereby each location is checked to see that its data is identical to the corresponding data in the master device (PP40) or the RAM (PP41, PP42).

If a device passes the in-program verify at all locations an automatic verify is performed.

Should a device fail the in-program verify, the display will show:



Red LEDs indicate the failed device(s). The cursor keys can be used to move to each in turn, and the display will change to give information of the format below:



R = RAM s = slave

While the failed device data is displayed the red LED flashes but stops flashing when -> or <- is pressed to move to the next failed device.

Press Set to skip to the next failing addresses.

3.8 DEVICE ADDRESS LIMITS (SET F6)-PP40

All device-related functions on the PP40 are defined by two parameters: the address limits. These are Address High and Address Low.

Press SET F6

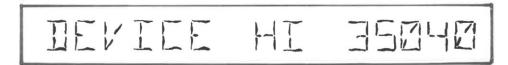
to set the address limits. The display will show:



A new address limit can be entered using the hexadecimal keyboard.

Press ↓ or ↑

to display:



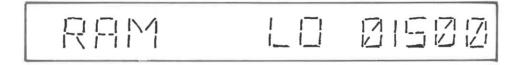
A new address limit can be entered using the hexadecimal keyboard.

3.9 DEVICE ADDRESS LIMITS (SET F6) — PP41 and PP42

All device-related functions on the PP41 and PP42 are defined by three parameters: the address limits. These are Address High, Address Low and RAM Low.

Press SET F6

to set the address limits. The display will show:



A new address limit can be entered using the hexadecimal keypad.

Press

to display:



A new address limit can be entered using the hexadecimal keypad.

Press 1

to display:



The upper limit defaults to the size of the device but a new limit can be entered using the hexadecimal keypad.

Pressing displays the address limits in the reverse order.

PP41 and PP42 ONLY

stag

SECTION 4

stag

4.1 KEYBOARD EDIT ROUTINES

The comprehensive editor on the PP41 and PP42 enables the following functions:

LIST

This is a feature enabling the data content of the RAM to be scanned on the display, without the danger of changing the RAM data.

It can be selected by pressing the list key: the first address will be displayed with the data within the first address.

For example:



The address can be scanned in two ways:

1. By use of the cursor keys:



- (a) By using the right/left cursor keys the address can be incremented or decremented a single location at a time.
- (b) By using the up/down cursor keys the address can be incremented or decremented 16, locations at a time.
- Any address with RAM limits can be directly entered by use of the hexadecimal keypad.

For example:

SELECTED ADDRESS	DATA	
CIFFO	29	

^{*}Note: if 16 or 32 bit configurations are selected on the PP42 the address shown will be the true address and the data will be four or eight digits in size.

4.2 **EDIT**

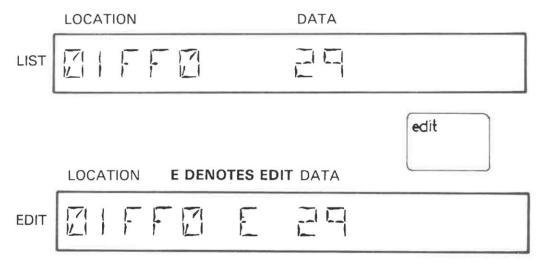
This is a feature whereby the actual content of the RAM can be directly modified by using the keyboard.

The edit mode can be selected in two ways.

- (a) By pressing the edit key when the machine is in the normal operating mode.
- (b) By pressing the edit key when the machine is in the list mode. (The list mode can be reselected in the same manner).

When switching from the list to the edit mode or visa versa the address and data being displayed will be unaffected.

For example:



The data '29' at location '01FF0' can now be changed by use of the hexadecimal keypad into A3, for example.



As with 'list' the data can be scanned by use of the cursor keys; when selection of address is made the information can again be changed by use of the hexadecimal keypad.

Alternatively and usually more quickly an address can be directly entered by switching back to the 'List mode' and using the hexadecimal keypad to select the location. Switching back to the edit mode will not corrupt this information.

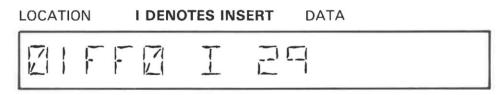
Note: if 16 or 32 bit configurations are selected the address shown will be the true address and the data will be four or eight digits in size.

4.3 INSERT

Insert is part of the edit mode and can be selected by pressing the edit key once, when the machine is in the edit mode.

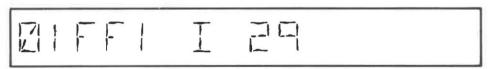
Information can be inserted into a particular location within the RAM. The existing data content in and above the selected address is repositioned one location higher. Apart from this shift in location the existing data remains the same.

For example:



By pressing the SET key all data inclusive of location 01FF0 and above is repositioned one location higher:

NEXT LOCATION UP



Having pressed the set key, '00' will be inserted into the selected address.



By use of the hexadecimal keypad the chosen data can now be inserted for instance A6:



Other than the use of the set key, operation in the Insert mode remains the same as when in the ordinary edit mode. For graphic example see next page.

Note: if 16 or 32 bit configurations are selected on the PP42 the address shown will be the true address and the data will be four or eight digits in size.

4.4 DELETE

Delete is also part of the edit mode and can be selected by pressing the edit key twice when the machine is in the edit mode. Delete is the opposite function to insert whereby data is removed 'from' a particular location.

The data above the selection address is repositioned one location lower.

For example: 5B is the data to be deleted.

LOCATION D DENOTES DELETE DATA

By pressing the SET key all data above but not inclusive of location 00200 is automatically brought down one location. The information previously at address 00201 replaces 'Data 5B' at location 00200.

For example:



Other than the use of the set key, operation in the delete mode remains the same as when in the ordinary edit mode.

For graphic example see next page.

^{*}Note: if 16 or 32 bit configurations are selected on the PP42 the address shown will be the true address and the data will be four or eight digits in size.

4.5 BLOCK MOVE (SET F4)

SETTING ADDRESS LIMITS

This is a feature enabling a block of data with pre-selected address limits to be relocated at another address within the RAM, without destroying the original data.

Selection of this function is made by pressing SET F4.

The display will show:

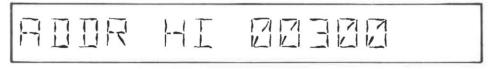
ADDRESS LOV	V	ZERO			
FIIIR					
This defines the lower (Defaults to 0000)	limit of the b	lock in RAM	to be re-located.		
The new lower RAM limit can be entered using the hex-keyboard					
For example 00100:		NEW LOWE	ER RAM LIMIT		
HIIR					
If is pressed the display will show: ADDRESS HIGH SIZE OF SELECTED DEVICE					
HIIR	HI	BEF	FF		

This defines the upper limit of the block in RAM to be relocated. (Defaults to selected device size).

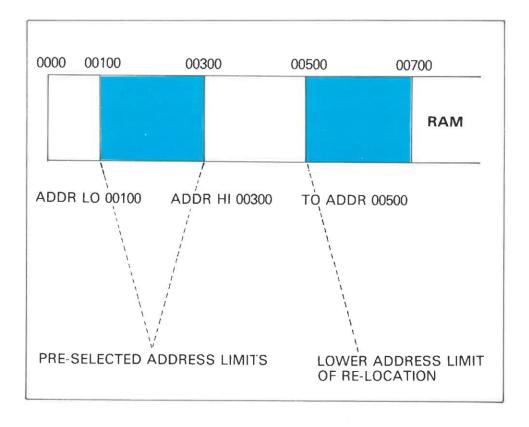
A new value for the upper RAM limit can be entered using the hexadecimal keypad.

For example 00300:

NEW UPPER RAM LIMIT



A GRAPHIC EXAMPLE OF HOW THE BLOCK MOVE FUNCTION WORKS IS SHOWN BELOW:



4.6 FILLING THE RAM

ADDRESS LOW

By pressing SET FF the RAM will be entirely filled with Fs.

By pressing SET FO the RAM will be entirely filled with Os (Zeros).

By pressing SET 5 the RAM data will be complemented. (1's complement).

FILLING THE RAM WITH AN ARBITRARY VARIABLE*. (SET F2)

This function enables the user to fill the RAM with an arbitrary variable of his own choosing.

LOCATION ZERO

The variable will be identically repeated at every word within address limits specified by the user. Pressing SET F2 will display the lower address limit which defaults to zero:

ADDR				
The new lower address limit can be selected by using the hexadecimal keypad, for example 00600:				
		LOCATION		
FIIR				
The upper address limit can be shown by pressing and this also defaults to the device size.				
ADDRESS HIGH		LOCATION ZERO		
FIIR	HI			
The new upper limit can be selected using the hexadecimal keypad, for example 01000:				
		LOCATION		

4.7 STRING SEARCH

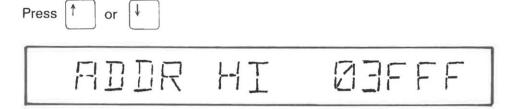
This function allows the RAM data to be searched for a particular string of data.

Press SET 9 to display:



The lower address limit of the area of RAM to be searched is now displayed defaulted to zero. It can be altered using values input from the keypad.

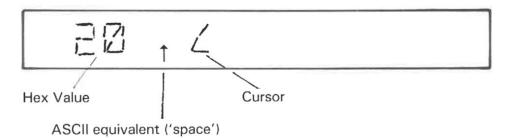
To display the upper limit:



The upper address limit is shown defaulted to the size of the pre-selected device, and like the lower limit it can be altered using values input from the keypad.

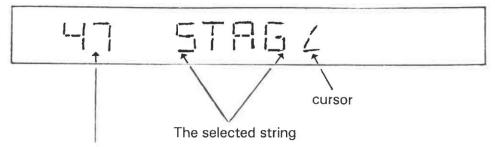
Once the address limits have been set:

Press SET to display:



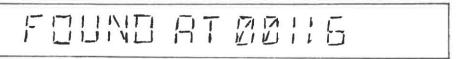
To the extreme left of the display is the hex equivalent of the ASCII character displayed on the immediate left of the cursor. In this case the space character is displayed.

For instance:



The ASCII value of the character to the immediate left of the cursor. (In this case 'G')

The above string was searched for and the display showed the following message:



This means that the first occurrence of the string was found at location 00116.

If the string had not been found within the specified area of RAM the display would have shown:



If a string has been entered and only part of it is to be used, then movifng the cursor to the left will restrict the string to the desired length. The original string will be retained however in its entirety, and moving the cursor to the right will display it again.

Any entered string will be retained until the programmer is powered down.

To abort the String Search at any time.

Press EXIT.

SECTION 5

stag

INPUT/OUTPUT

5.1 SETTING THE I/O INTERFACE PARAMETERS

It is possible to initiate an input or output without setting any of the associated parameters. Simply press the input or output key. The offset defaults to the offset last set; the start address defaults to zero, the input stop address defaults to the maximum RAM size and the output stop address defaults to the device size.

Hardware Parameters

Pressing SET 1 displays the hardware parameters for Port 1:

PORT NUMBER	BAUD RATE	WORD LENGTH	NO. OF STOP BITS	PARITY
PRTI.	9600	8	2	EP

To display the hardware parameters for Port 2:

Press SET 1

followed by Key 2 or just key 2 if SET has already been pressed.

The parameters for both ports can be changed. This is done by use of the horizontal cursor keys.

Press (

to move the chosen parameter field until it is immediately to the right of PRT 1 or PRT 2.

Press or U

to modify the parameter.

Software Parameters

Pressing SET 1 followed by Key 3 displays the software parameters:

SOFTWARE PARAMETER	FORMAT	PASS-THROUGH OPTION	CONTROL Z OPTION
되 사 문.	INT	TRSP	CZ
Press ↑ or ↓	16		

to select the required format.

Press

to enable selection of Pass-Through.

Press or or

to select Transparent (Pass-Through mode) or Normal (non-Pass-Through mode)

The selection available in each category is shown in this table.

WORD LENGTH 8 7

6

FORMAT	BAUD RATE
INT HASC XOR TEK XTEK PPX BIN DBIN MOST	38K4 19K2 9600 4800 2400 2000 1800 1200 600 300 150
	75 50
	30

NUMBER OF STOP BITS	PARITY
2	
1	EP
	OP OP

FORM	ΑT	-
Key to	Abb	reviations
INT	=	INTELLEC
HASC	=	HEX ASCII
XOR	=	EXORCISOR
TEK	=	TEK HEX
XTEK	=	EXTENDED TEK
PPX	=	STAG HEX
BIN	=	BINARY
DBIN	=	DEC BINARY
MOST	=	MOS TECHNOLOGY

PARIT	ΓΥ	
Key to	Abbi	reviations
	=	NO PARITY CHECK
EP	=	EVEN PARITY
OP	=	ODD PARITY

5.2 Setting the I/O Address Parameters

The pre-settable address parameters are:

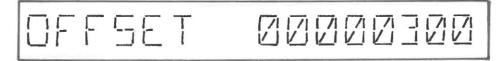
INPUT ADDRESS OFFSET
INPUT START ADDRESS
INPUT STOP ADDRESS

OUTPUT ADDRESS OFFSET
OUTPUT START ADDRESS
OUTPUT STOP ADDRESS

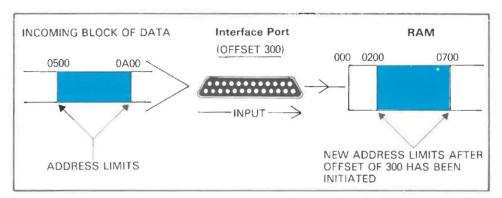
Input Parameters

An incoming block of data originating from peripheral equipment can be re-located at a lower address within the RAM, using an Input Offset.

Pressing 'Set Input' displays the last-entered offset Address, for example:



An offset of 300 would look like this:



The offset address can be changed using the hexadecimal keypad. 00000000 = No Offset

Press followed by Key 1

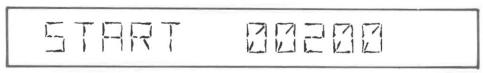
to select Port 1 for the data input.

or Press ↓ followed by Key 2

to select Port 2 for the data input.

Press 🗸

to display the Input start address.



Press again

to display the Input stop address. Both addresses can be changed using the hexadecimal keypad.

Pressing the input key initiates the input operation.

FORMAT OFFSET TYPES

FORMAT	DISPLAY ABBREVIATION	NO. OF RELEVANT DIGITS IN ADDRESS FRAME
INTELLEC	INT	5 Digits
HEX ASCII	HASC	0 Digits
MOTOROLA S-RECORD	XOR	8 Digits
TEK-HEX	TEK	4 Digits
EXTENDED TEK	XTEK	17 Digits
STAG HEX	PPX	4 Digits
BINARY	BIN	0 Digits
DEC BINARY	DBIN	4 Digits
MOS TECHNOLOGY	MOST	4 Digits

Eight characters are always displayed even when only 4 digits are required. Pressing the output key initiates the output operation.

5.3 ERROR REPORTING ON INPUT/OUTPUT

The following table shows the 12 possible error messages that will be displayed instead of the checksum on completion of either input or output or when 'exit' is pressed.

Reported at the end of data transfer

- (1) PARITY ERROR A parity error was detected.
- (2) FRAMING ERROR A pulse on the serial signal was not of an acceptable size.
- (3) PTY/FMG ERROR Parity/Framing: A combined parity and framing error was detected.
- (4) OVERRUN ERROR Data was lost due to overwriting of secondary information in UART.
- (5) PTY/OVN ERROR Parity/Overrun: A combined parity and overrun error was detected.
- (6) FMG/OVN ERROR Framing/Overrun: A combined framing overrun error was detected.
- (7) PY/FR/O/ERROR Parity/Framing/Overrun: A combined parity, framing and overrun error was detected.
- (8) L CSUM ERROR Line Checksum Error: A checksum failure in a record (line) was detected.
- (9) NON-HEX ERROR A non-hex character was received where a hex character was expected.

SECTION 6



stag

6.1 TRANSLATION FORMATS (INTRODUCTION)

There are nine formats available on the PP41 and PP42:

INT = INTELLEC HASC = HEX ASCII XOR = MOTOROLA S-RECORD MOST = MOS TECHNOLOGY TEK **TEK HEX** XTEK = EXTENDED TEK PPX = STAG HEX BIN = BINARY = DEC BINARY DBIN

STANDARD FORMATS

There are four standard manufacturer formats these are: INTELLEC, EXORCISOR, TEK HEX and MOS TECHNOLOGY which are used on most development systems.

EXTENDED FORMATS

There is one protracted version of the standard formats: EXTENDED TEK. The extended format can be used when a larger address field is required.

HEX ASCII

The Hex ASCII format is the original base version of the standard formats. It lacks the facility of an address field and a checksum.

PPX (Stag Hex)

The PPX format differs from the HEX ASCII in that it has an address field and terminates with a checksum of total bytes.

BINARY

The Binary format is the most fundamental of all formats and can be used where fast data transfers are required. It has no facility for address, byte count or checksum.

DEC BINARY

This is an improvement of binary in that it has a single address and a single checksum for the entire block of data.

6.2 INTELLEC

The intellec format when displayed consists of:

- a. A start code, i.e. (a colon):
- b. The sum of the number of bytes in an individual record, e.g. 1A.
- c. The address of the first byte of data in an individual record, e.g. 0000.
- d. The record types, i.e. 00-Data Record 01-End Record.
- e. Data in bytes, e.g. 12 34 56 78.
- f. Checksum of an individual record, e.g. 28.

For example:

START ADDRESS:	0000
STOP ADDRESS:	008F
OFFSET:	0000

ADDRESS OF FIRST START CODE BYTE IN EACH RECORD.

: 1A000000123456781234

NO. OF DATA BYTES IN EACH RECORD

RECORD TYPE

CHECKSUM OF EACH RECORD

CALCULATION OF THE INTELLEC* CHECKSUM

Example: THE SECOND 'DATA RECORD' OF THE ABOVE FORMAT.

(i) This is: :01 00 1A 00 56 8F

(ii) The start code and the

checksum are removed: :8F

(iii) Five Bytes remain: 01 00 1A 00 56

(iv) These are added together: 01 + 00 + 1A + 00 + 56 = 71

(v) The total '71' is converted into 7 1 Binary: 0111 0001

(vi) The Binary figure is reversed. 8 E
This is known as a complement: 1000 1110

(vii) A one is added to this 8 F compliment. This addition 1000 1111 forms a "2's complement":

(viii) 8F is the checksum as above: :01 00 1A 00 56 8F

When addition of information occurs in longer records the checksum may consist of more than one byte. When this occurs the least significant byte is always selected to undergo the above calculation.

^{*}This calculation also applies to the extended version.

6.3 HEX ASCII

The Hex ASCII format when displayed consists of:

DATA ALONE

However, invisible instructions are necessary for operation. These are:

(A hidden start character known as Control B.

(02: ASCII Code, STX ASCII character).

A hidden stop character known as Control C.

(03: ASCII Code, ETX ASCII character)

A hidden 'space' character between data bytes

(20: ASCII Code, SP, ASCII character)

For example:

START ADDRESS	0000
STOP ADDRESS:	008F

OFFSET: NONE REQUIRED AS HEX ASCII ALWAYS LOADS AT ZERO

HIDDEN START CHARACTER (Control B)

HIDDEN SPACE CHARACTERS

O12 34 56 78 12 34 56 78

HIDDEN STOP CHARACTER (Control C)

16 bytes per line on output

- 30 49 0004

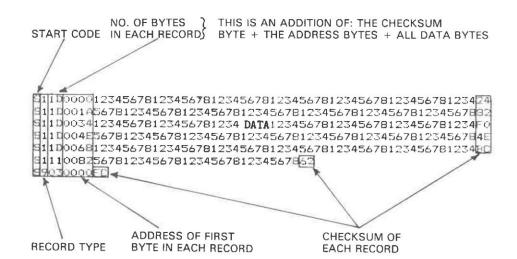
6.4 MOTOROLA S-RECORD

The Motorola S-Record when displayed consists of:

- a. A start code, i.e. S
- b. The record types, i.e. 1 Data Record 9 - End Record
- c. The sum of the number of bytes in an individual record, e.g. 1D
- d. The address of the first byte of data in an individual record, e.g. 0000
- e. Data in bytes, e.g. 12 34 56 78
- f. Checksum of an individual record, e.g. A4

For example:

START ADDRESS:	0000
STOP ADDRESS:	008F
OFFSET:	0000



CALCULATION OF THE EXORCISOR* CHECKSUM

\$1100000123456781234567812345678123456781234567812345678123424 <u>\$10400145688</u> \$9030000FC

Example: THE SECOND 'DATA RECORD' OF THE ABOVE FORMAT.

(i) This is: S1 04 00 1A 56 8B

(ii) The start code, the record type and the checksum are removed: S1 8B

(iii) Four Bytes remain:

(vii) 8B corresponds to the

(iv) These are added together: 04 + 00 + 1A + 56 = 74

04 00 1A 56

(v) The total '74' is converted into 7 4 Binary: 0111 0100

(vi) The Binary figure is reversed. 8
This is known as a complement: 1000 1011

checksum as above: S1 04 00

(8B)

56

1A

When no additional figures are added to this calculation it is called a 1's (One's) complement.

When addition of information occurs in longer records the checksum may consist of more than one byte. When this occurs the least significant byte is always selected to undergo the above calculation.

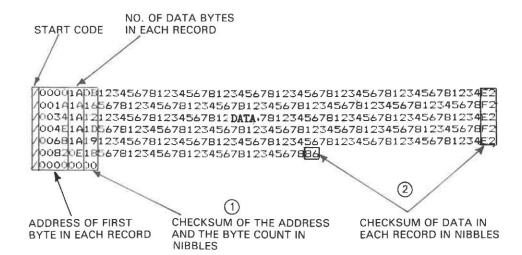
^{*}This calculation also applies to the extended version.

6.5 TEK HEX

The Tek Hex format when displayed consists of:

- a. A start code, i.e.
- b. The address of the first byte of data in an individual record, e.g. 0000
- c. The sum of the number of data bytes in an individual record, e.g. 1A
- d. Checksum 1 which is a nibble addition of the address (4 characters) and the byte count (2 characters), e.g. 0B
- e. Data in bytes, e.g. 12 34 56 78
- f. Checksum 2 which is a nibble addition of all data.
- g. An end record which automatically stops the operation when 00 is specified in the byte count (c).

For example:	START ADDRESS:	0000
	STOP ADDRESS:	008F
	OFFSET:	0000



CALCULATION OF TEK HEX CHECKSUMS

Unlike the other PP39 formats, the Tek Hex has two checksums which are both the result of nibble additions, as opposed to byte additions.

Checksum 1 is a nibble addition of the 'address' and the 'byte count' which make 6 characters in total.

Checksum 2 is a nibble addition of data alone.

Example: THE THIRD "DATA RECORD" OF THE ABOVE FORMAT

CHECKSUM 1

(i) This is: /10034030A

The start code and the checksum are removed: /0A

(iii) Six nibbles remain: 003403

(iv) They are added together: 0+0+3+4+0+3 = A

(v) 0A is the checksum which is displayed in byte form as above: /1003403

CHECKSUM 2

(i) This is: 12345615

(ii) The checksum is removed: 15

(iii) Six nibbles remain: 123456

(iv) These are added together: 1+2+3+4+5+6=15

(v) 15 is the checksum as above: 123456

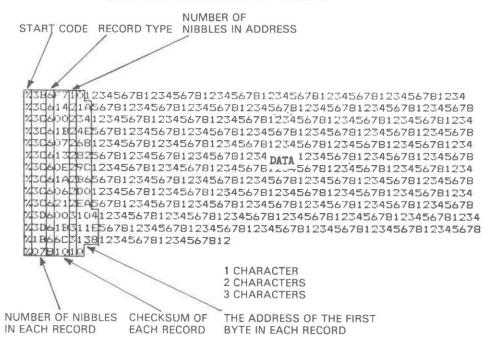
When addition of nibble information occurs in longer records the checksum may consist of more than one byte. When this occurs the least significant byte is always selected to undergo the above calculation.

6.6 EXTENDED TEK HEX

The Extended Tek Hex when displayed consists of:

- a. A start code: % (percentage)
- b. A count of the nibbles in an individual record, e.g. 3B
- c. The record types, i.e. 6—Data Record 8—End Record
- d. A checksum of the whole of an individual record excluding the %, e.g. F7
- e. *The number of nibbles comprising—"the address of the first byte in each record", e.g. 1, 2, 3 etc.
- The address of the first byte of data in an individual record, e.g. 0, 1A, 104

For example:	START ADDRESS:	0000
	STOP ADDRESS:	0140
	OFFSET:	0000 0000



CALCULATION OF THE EXTENDED TEK HEX CHECKSUM

Unlike the standard version the Extended Tek Hex has only one checksum.

X3B6F7101234567812345678123456781234567812345678123456781234 X3C61421A5678123456781234567812345678123456781234567812345678 Z0A6IC234I2 X0781010

Example: THE THIRD LINE OF THE ABOVE FORMAT.

(i) This is:

% 0A61C23412

(ii) The start code and the checksum are removed:

% 1C

(iii) Eight nibbles remain:

0A623412

(iv) These are added together:

0 + A + 6 + 2 + 3 + 4 + 1 + 2 = 1C

(v) 1C is the checksum as above;

% 0A6 (1C) 23412

When addition of nibble information occurs in longer records the checksum may consist of more than one byte. When this occurs the least significant byte is always selected to undergo the above calculation.

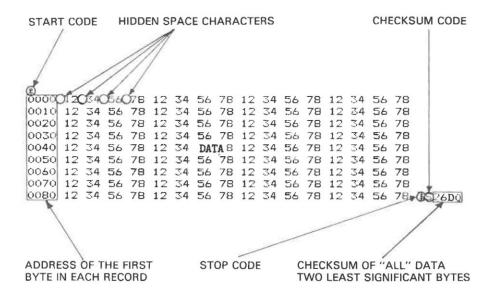
6.7 PPX or (STAG HEX)

The PPX format when displayed consists of:

- a. A start code, i.e. * (an asterisk, 2A-ASCII Code)
- b. The address of the first byte of data in an individual record, e.g. 0000
- c. Data in bytes, e.g. 12 34 56 78
- d. A stop code, i.e. \$ (a dollar sign, 24-ASCII Code)
- e. A checksum start code: S
- f. A checksum of all data over the entire address range. (The displayed checksum is the two least significant bytes.)
- g. An invisible space character between data bytes (20-ASCII Code)

For example:

START ADDRESS:	0000
STOP ADDRESS:	008F
OFFSET:	0000



CALCULATION OF THE PPX CHECKSUM

"Data alone", in bytes over the entire address range (as opposed to individual records) is added together to give the checksum. The address is not included in this calculation.

* 0000 12 34 56 78 \$S0114

Example: THE SEGMENT OF DATA ABOVE

(i) This is: *0000 1 34 56 78 \$S0114

(ii) The start code, the address, the stop code, the checksum code and the checksum are removed: *0000 \$S0114

(iii) Four bytes remain: 12 34 56 78

(iv) These are added together: 12 + 34 + 56 + 78 = 114

(v) 114 is the checksum which is displayed in two byte form as above:

*0000 12 34 56 78 \$\$ 0114

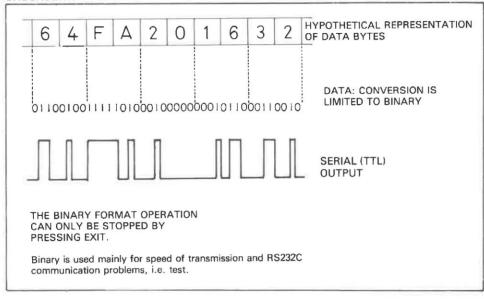
As the PPX checksum is an addition of all data the total will invariably constitute more than two bytes. When this occurs the least significant 'two' bytes are always selected to undergo the above calculation.

6.8 BINARY AND DEC BINARY

Binary and DEC Binary are the most fundamental of all formats. ASCII code conversion never occurs. Information is therefore limited to the interpretation of pulses via the RS232C interface port into either ONE'S or ZERO's. Hence 'Binary'. A visual display is not possible.

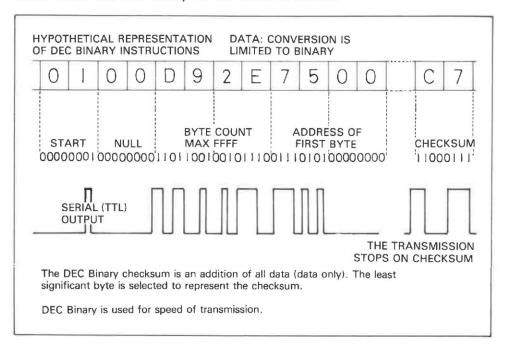
6.8.1 **BINARY**

Binary is data only. It is devoid of a start code, address, stop code and checksum.



6.8.2 DEC BINARY

DEC Binary is an improvement of Binary. It has a start code, a null prior to transmission, a byte count, a single address and a single checksum of all data. It also has the facility for an offset to be set.

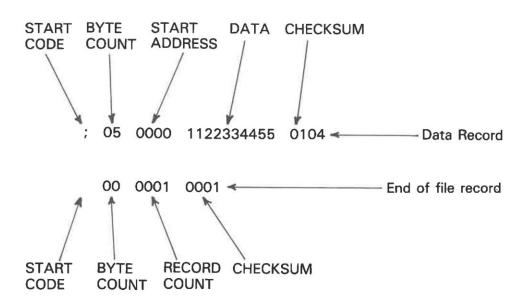


6.9 MOS-TECHNOLOGY

The MOS-TECHNOLOGY format consists of:

- i. a start code, ie: ; (semi-colon)
- ii a byte count—that is the sum of the number of data bytes in an individual record, eg: 05
- iii the address of the first byte of data in an individual record, eg: 0000
- iv data in bytes, eg: 11 22 33 44 55. (The data bytes must consist of valid hexadecimal digits).
- a checksum which is displayed as two hexadecimal bytes. It is the addition of the preceding data bytes in the record including the address and byte count in hexadecimal form.

For example:



SECTION 7



stag

7.1 RS232C INTERFACE PORT CONNECTIONS

The PP41 and PP42 are linked to peripheral equipment via their two RS232C interface ports.

LINK-UP TO PERIPHERAL EQUIPMENT

There are two distinct types of machine:

- (i) Data Terminal Equipment (DTE)
- (ii) Data Communication Equipment (DCE)

The PP41 and PP42 fall into both categories: Port 1 is configured as DTE, Port 2 is configured as DCE.

On the male connector only 9 of the 25 available pins play an active role in data transfer. These are numbers 1, 2, 3, 4, 5, 6, 7, 8 and 20.

1.*	PG	PROTECTIVE GROUND	
2.	TXD	TRANSMITTED DATA	
3.	RXD	RECEIVED DATA	
4.	RTS	REQUEST TO SEND	
5.	CTS	CLEAR TO SEND	
6.	DSR	DATA SET READY	
7.	SG	SIGNAL GROUND	
8.	DCD X	DATA CARRIER DETECT	
20. D.T.R.		DATA TERMINAL READY	

^{*}Pin Number 1 is present in all connections, it represents the Protective Ground surrounding all the other cables.

(Day :: :: -- 4) 7 4 04

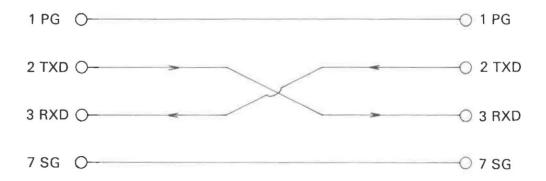
7.2 CONNECTION TYPES

The programmers support the two most popular types of connection, these are:

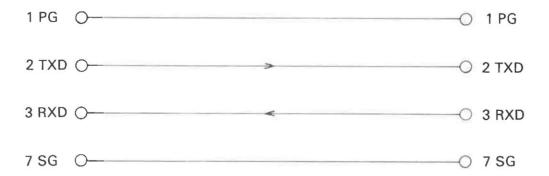
XON/XOFF (3 wire cable-form connection) and (7/8 wire cable form) hardware handshake. The most straightforward of these two is the XON/XOFF.

XON/XOFF (3 wire cable-form connection)

a. For connection of two alike machines a 'cross over' is required.
 DCE to DCE and DTE to DTE:



b. For connection of two unalike machines 'no' cross over is required.
 DCE to DTE and DTE to DCE: Straight



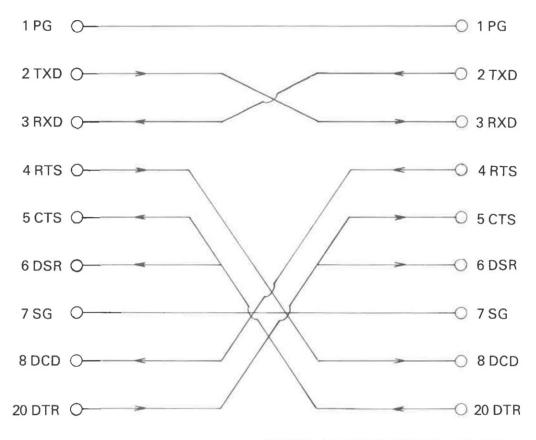
NOTE: Some machines do not have internal pull-ups and require extra connections within the cable form. Pull-ups may be required on pins 5, 6 and 8 of the external device if it is DTE or pins 4, 6 and 20 if it is DCE.

/D ** 41 7004

7.3 HARDWARE HANDSHAKE (7 OR 8 WIRE CABLE-FORM)

DCE TO DCE AND DTE TO DTE CROSSOVER 8 WIRE CABLE-FORM
DCE TO DTE AND DTE TO DCE STRAIGHT 7 WIRE CABLE-FORM

a. For connection of two alike machines a 'cross over' is required. DCE to DCE and DTE to DTE:



EXISTS AS STAG PART No. 10-0250

7.4 NON-STANDARD CONNECTIONS

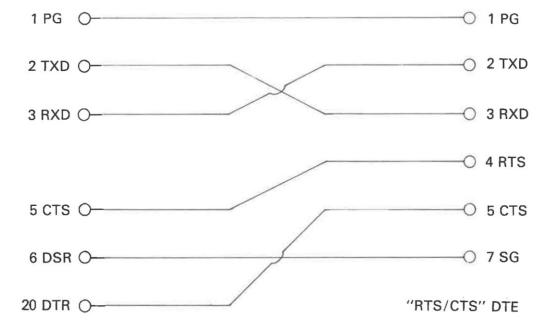
HARDWARE HANDSHAKE (5 WIRE CABLE-FORM)

This is a link-up to an unalike connector using "CTS-RTS" handshaking, it is made possible by the fabrication of a non standard cable-form.

RTS is a signal normally made active, but it remains inactive to inhibit data transmission to it, from external devices.

CTS is a pin kept inactive, to prevent signal transmission from it.

For DTE to DTE the following cable-form will be required.



SECTION 8

stag

8.1 SELECTION OF 'LOCAL' OR 'REMOTE' MODE

To select Local Mode

If the machine is in remote mode on power-up, one of two sequences can be performed:

- (i) If the programmer is connected via the remote I/O port to a computer or terminal keyboard then the sequence of pressing Key 'Z' followed by the 'RETURN' key will bring control back to 'local' on the programmer's keyboard.
- (ii) If the programmer is in stand-alone mode on power-up, but still under the 'remote' setting, the operator must power down, wait two seconds and then power up again with the 'EXIT' key simultaneously depressed to read 'local' mode.

When either sequence (i) or (ii) is performed the display will show manufacturer, device type and bit mode. A typical 'local' mode setting might be:



In local mode all functions of the programmer are controlled from its own keyboard.

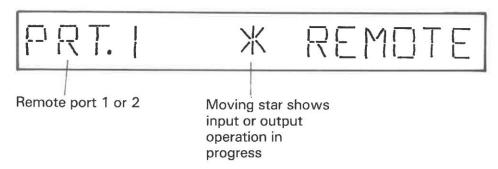
8.2 REMOTE CONTROL

To select remote control Press Set 2

The display will show:



By pressisng set again, the display will show:



In remote mode the programmer is operated remotely from a computer or terminal. The programmer's keyboard is inoperative at this time.

Note: If Pass-through has been selected then pressing Set 2 gives the display:



A full description of Pass-through and its remote mode of operation is found in Section 9.

REMOTE CONTROL COMMANDS

h = one hex digit

RETURN Executes a command for instance G RETURN, A6AF< RETURN, [RETURN, 11A RETURN etc.

G Software revision number. This command issues a 4-digit hex number representing the software configuration in the programmer.

Z Exits from remote control.

H No operation. This is a null command and always returns a prompt character (>)

SET UP FOR DEVICE/RAM FUNCTIONS

hhhh@ *A four digit code sets up programming for a particular device. (The first two digits represent the manufacturer code and the second two represent the pin out code).

*The programmer sends a four digit hex code of the device in use. (The first two digits represent the manufacturer code and the second two represent the pin out code).

T Test for illegal bit in the device.

B Blank check, sees that no bits are programmed in the device.

R Respond indicates device status for instance: 00FFF/8/0>:
The first 5 digits reflect the working RAM limit relevant to the device. The 6th digit is the byte size measured in bits.
The 7th digit reflects the unprogrammed state of the device selected. The 7th digit can be either 1 or 0.

0 = Unprogrammed state 00.1 = Unprogrammed state FF.

SET UP FOR INPUT AND OUTPUT

Selection of Translation Formats A.

10A	BINARY	
11A	DEC BINARY	
50A	HEX-ASCII (Space)	
51A	HEX-ASCII (Percent)	
52A	HEX-ASCII (Apostrophe)	
53A	HEX-ASCII (Comma)	
59A	STAG HEX	
82A	MOTOROLA S-RECORD	
83A	INTELLEC 86	
86A	TEK HEX	
96A	EXTENDED TEK HEX	
81A	MOS TECHNOLOGY	

All covered by standard HEX-ASCII

Input/Output Address Limits

h hhhh< Sets a five digit figure defining the lower address limit.

h hhhh; Sets the number of bytes of data to be transferred, which in effect defines the upper address limit.

hhhh hhhhW Sets the offset required for data transference for both INPUT and OUTPUT.

I INPUTS data from the computer/terminal to the programmer's RAM

O OUTPUTS data from the programmer to the computer/terminal.

By initiating either the INPUT or the OUTPUT operation data transfer will commence, inclusive of any pre-selected parameters specified above.

To select Port 1 or Port 2 preceed I or O with a '1' or a '2'. If the port number is not specified the programmer defaults to the last selected port.

ERROR RESPONSES

F Error-status inquiry returns a 32-bit word that codes errors accumulated. Error-status word resists to zero after interrogation. (See remote error words).

X Error-code inquiry. Programmer outputs error codes stored in scratch-RAM and then clears them from memory. (See remote error codes).

H No operation. This is a null command and always returns a prompt character (>).

PROGRAMMER RESPONSES

> CR Prompt character. Informs the computer that the programmer has successfully executed a command.

F CR Fail character. Informs the computer that the programmer has failed to execute the last-entered command.

? CR Question mark. Informs the computer that the programmer does not understand a command.

CR = Carriage return.

8.4 Remote Error Codes

Code	Name	Description
20	Blank check Error	Device not blank
21	Illegal bit Error	
22	Programming Error	The device selected could not be programmed
23	Verify Error	
26	Device Faulty	Either faulty part or reversed part
48	Buffer Overflow	
82	Checksum	
84	Invalid Data	

/D · · · 41 0 4 0 4

INTERPRETATION OF THE ERROR STATUS WORD

EXAMPLE: 80C80084

- 8 —The word contains error information
- 0 -No receive errors
- C -(=8+4); 8 = Device error 4 = Start line not set high
- 8 Device is not blank
- 0 -No input errors
- 0 —No input errors
- 8 -RAM error
- 4 Insufficient RAM resident

SECTION 9

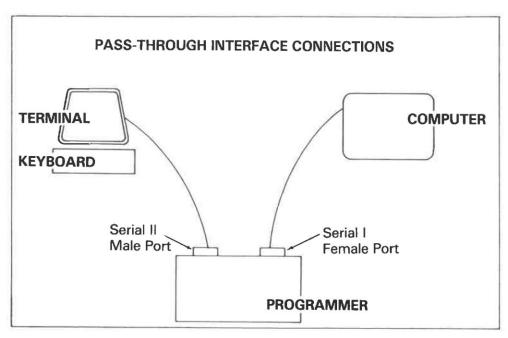


stag

PASS-THROUGH

The PASS-THROUGH mode allows communication between a terminal, the programmer and a computer by utilizing only one connection on the terminal and the computer.

Note: In order for PASS-THROUGH to work the computer must be connected to the programmer via the RS232(1) female port (configured as DTE) and the terminal must be connected via the RS232(2) male port (configured as DCE).



Pass-Through mode is selected by pressing Set 1 followed by Key 3, and from or from or

There are two modes of operation for Pass-Through:

- (i) Normal Mode
- (ii) Remote Mode

9.1 (i) Normal Mode

The programmer appears to be transparent in data transfer between the terminal and the computer. Pass-Through continues until the input or output key is pressed on the programmer, causing it to display the message 'Stand By'. Nothing further is transmitted until either the programmer receives a 'Control O' sequence from the computer or its own 'Set' Key is depressed. The input or output function is then implemented.

When the input or output is finished or the exit key is used to abort the function, the programmer goes back to Pass-Through.

PP42 ONLY



stag

SECTION 10

stag

BIT MODES AND SET PROGRAMMING

The PP42 can be configured to 8, 16 or 32 bit mode using Stag's "Interlace" concept. A wide range of set programming options are available, selected by pressing:

SET 3

The display will show the last-entered bit mode configuration. To change configuration press \downarrow or \uparrow

10.1 8-BIT MODE

There are four options available.

0 8-BIT 8 0F 1

In this gang mode the devices all receive the same data from the RAM and are therefore identical.

This configuration is abbreviated when displayed with other information, for example:

INTL 27256 8.8/1

··· B-BIT 4 CF 2

This mode consists of four identical sets of two devices. The two devices within the set differ from each other in the data which they receive from the RAM.

 $\begin{bmatrix} A \\ MS \end{bmatrix} \begin{bmatrix} B \\ S \end{bmatrix} \begin{bmatrix} A \\ S \end{bmatrix} \begin{bmatrix} B \\ S \end{bmatrix} \begin{bmatrix} A \\ S \end{bmatrix} \begin{bmatrix} B \\ S \end{bmatrix} \begin{bmatrix} A \\ S \end{bmatrix} \begin{bmatrix} B \\ S \end{bmatrix} \begin{bmatrix} M = master, \\ S = slave \end{bmatrix}$

This configuration is abbreviated when displayed with other information, for example:

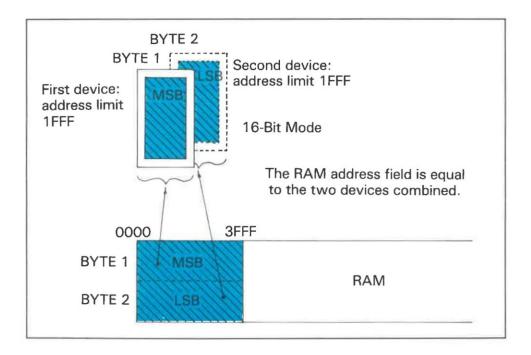
INTL 27255 0.4/2

10.2 16-BIT MODE

In this mode 16 data bits are split between two eight-bit devices.

A graphic example of how the 16-Bit Mode works on both LOAD and PROGRAM is shown below:

For clarity the following example will show a fixed device size: 1FFF (2764 EPROM)



In the first operation: PROGRAM or LOAD is made to and from a single 8-Bit device with only the most significant byte "MSB" of a 16-Bit Word undergoing data transfer.

In the second operation: PROGRAM or LOAD is made to and from a single 8-Bit device with only the least significant byte "LSB" of a 16-Bit word undergoing data transfer.

/n 11 41 40 0 0 0

There are two options available:

15 BIT IDENTICAL

The two devices function interactively, although they differ from each other in the data which they receive from the RAM. Together they form a set. Four such identical sets are possible.

This configuration is abbreviated when displayed with other information, for example:

INTL 27256 16.I

IS-BIT DIFFERENT

The two devices function interactively, although they differ from each other in the data which they receive from the RAM. Together they form a set. Four such sets are possible, each unique.

 $\begin{bmatrix} \mathsf{A} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{B} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{P} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{Q} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{C} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{D} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{R} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{S} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{M} = \mathsf{Master} \\ \mathsf{S} = \mathsf{Slave} \end{bmatrix}$

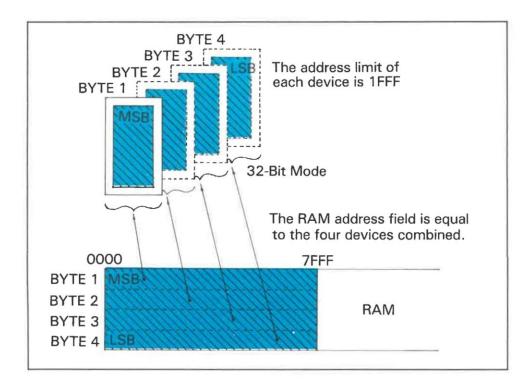
This configuration is abbreviated when displayed with other information, for example:

INTL 27256 15.D

10.3 32-BIT MODE

In this mode 32 bit data bits are split between four eight-bit devices.

A graphic example of how the 32-Bit Mode works on both LOAD and PROGRAM is shown below:



In the first operation: PROGRAM or LOAD is made to and from a single 8-Bit device with only BYTE 1 the "most significant byte" of a 32-Bit Word undergoing data transfer.

This sequence is repeated for the next three devices with bytes 2, 3 and 4 respectively undergoing data transfer.

There are two options available:

O 32-BIT IDENTICAL

The four devices function interactively, although they differ from each other in the data which they receive from the RAM. Together they form a set. Two such identical sets are possible.

A B C D A B C S S M = Master S = Slave

This configuration is abbreviated when displayed with other information, for example:

INTL 27256 32.I

(ii) 32-BIT DIFFERENT

The four devices function interactively, although they differ from each other in the data which they receive from the RAM. Together they form a set. Two such sets are possible, each unique.

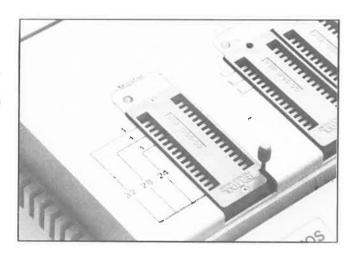
 $\begin{bmatrix} \mathsf{A} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{B} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{C} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{D} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{P} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{Q} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{R} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{S} \\ \mathsf{MS} \end{bmatrix} \begin{bmatrix} \mathsf{M} = \mathsf{Master} \\ \mathsf{S} = \mathsf{Slave} \end{bmatrix}$

This configuration is abbreviated when displayed with other information, for example:

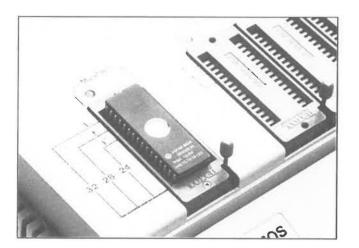
INTL 27256 32.D

Correct Operation of ZIF Sockets.

Empty ZIF socket.
 Lever in open (up) position.



Device inserted.Socket open.



 Device inserted.
 Lever in closed (down) position.

